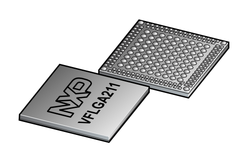

SOT1868-1

VFLGA211, plastic, very thin fine-pitch land grid array package; 211 balls; 0.5 mm pitch; 9.6 mm x 9.6 mm x 0.805 mm body

11 January 2019 Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	VFLGA211
Package style descriptive code	VFLGA (very thin fine-pitch land grid array package)
Package body material type	P (plastic)
Mounting method type	S (surface mount)
Issue date	06-12-2018
Manufacturer package code	98ASA00988D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	9.6	-	mm
package width	-	9.6	-	mm
package height	-	0.85	-	mm
nominal pitch	-	0.5	-	mm
actual quantity of termination	-	211	-	

2 Package outline

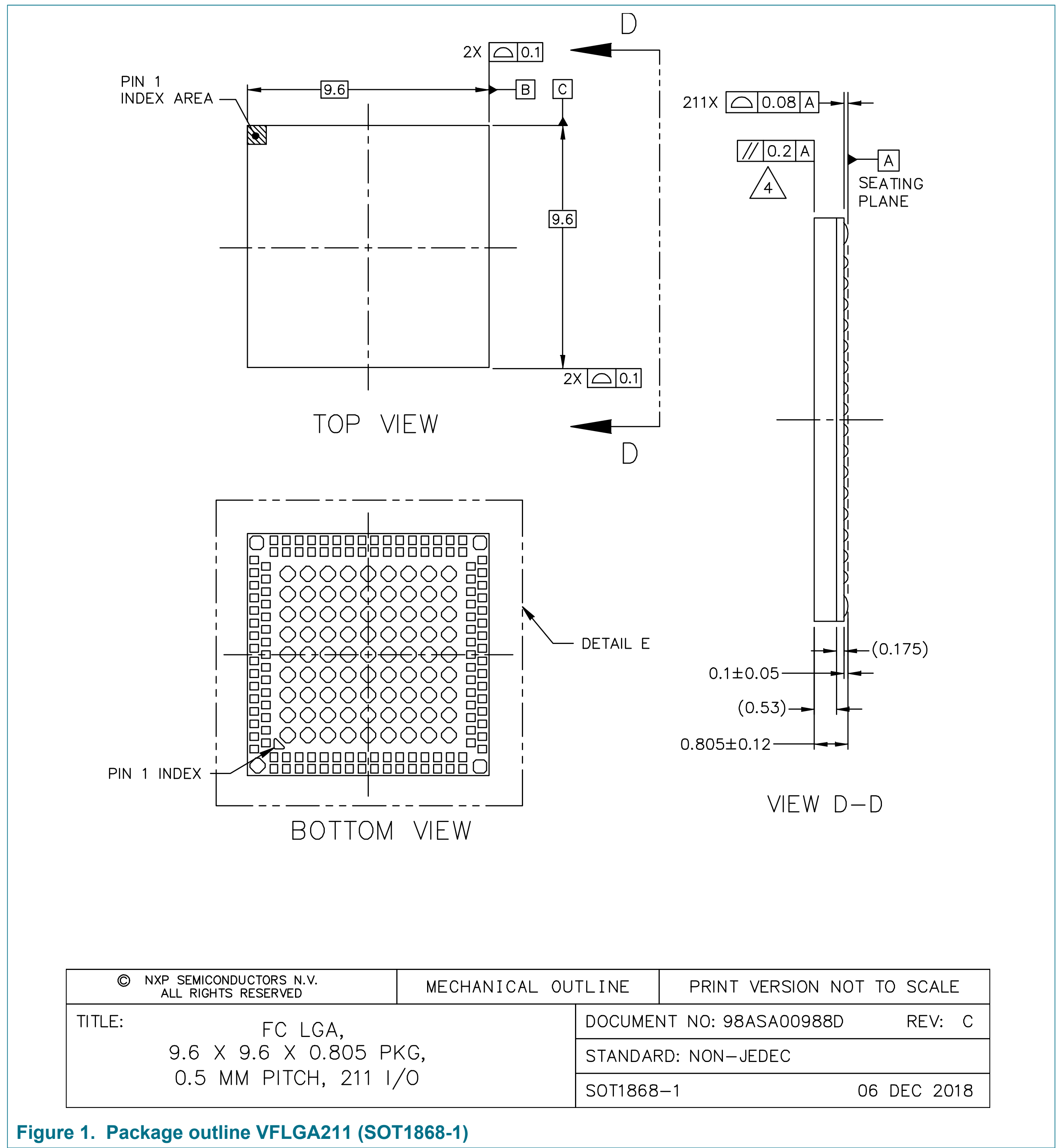

Figure 1. Package outline VFLGA211 (SOT1868-1)

 © NXP B.V. 2019. All rights reserved.

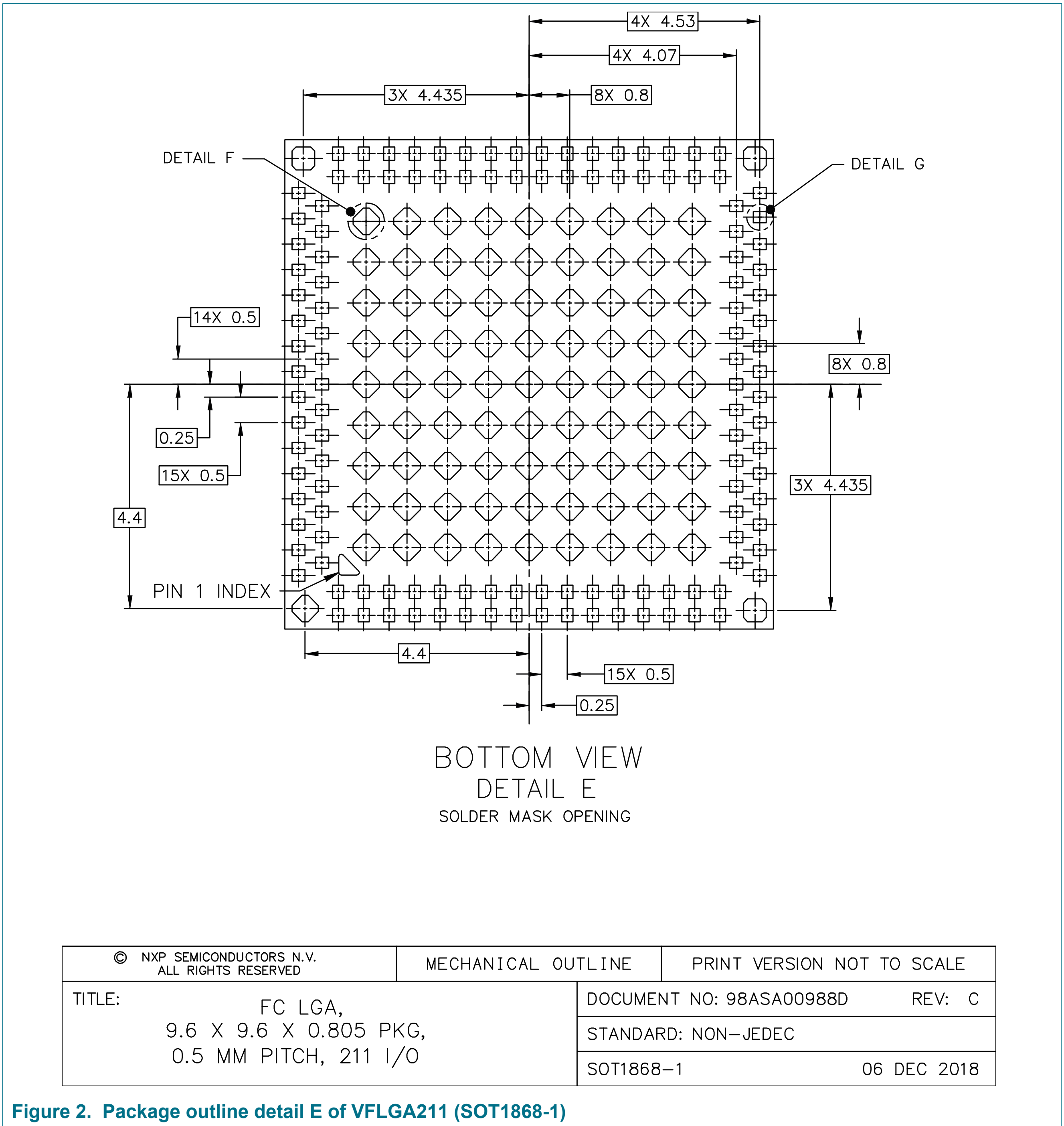

Figure 2. Package outline detail E of VFLGA211 (SOT1868-1)

 © NXP B.V. 2019. All rights reserved.

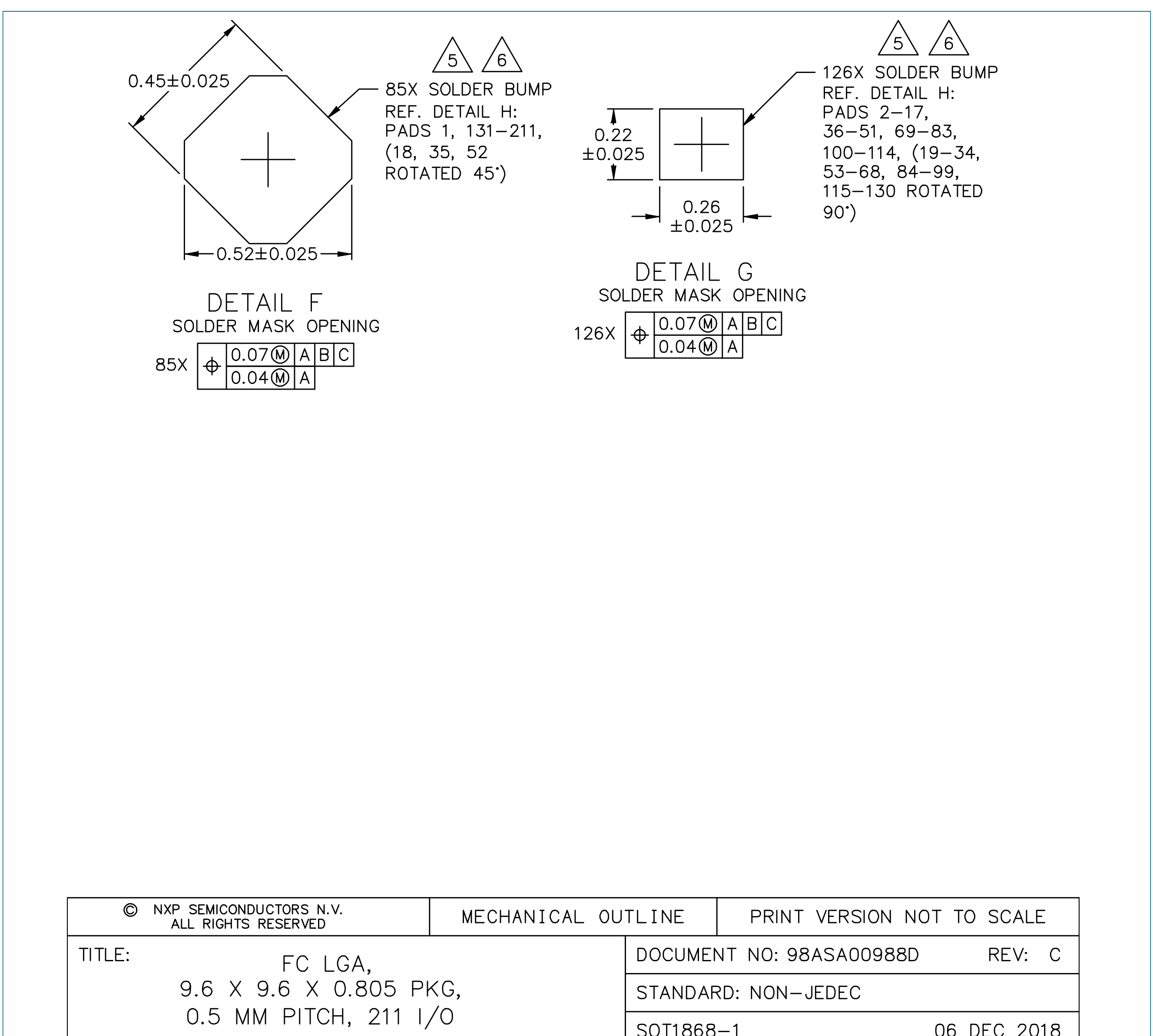

Figure 3. Package outline detail F/G of VFLGA211 (SOT1868-1)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2019. All rights reserved.

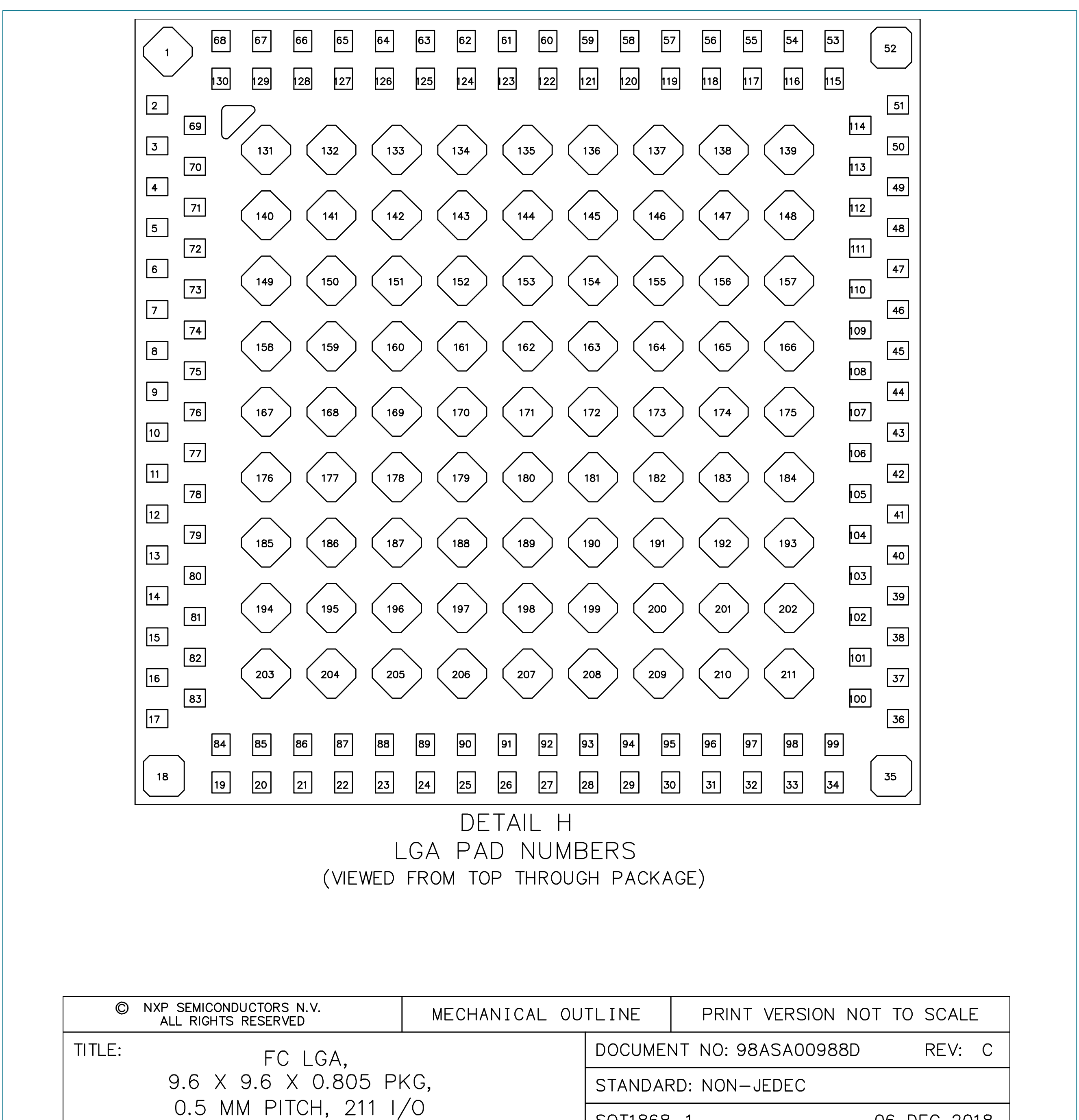

Figure 4. Package outline detail H of VFLGA211 (SOT1868-1)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2019. All rights reserved.

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

3. ALL DIMENSIONS ARE SYMMETRIC ACROSS THE PACKAGE CENTER LINES, UNLESS DIMENSIONED OTHERWISE.

4. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

5. MAXIMUM SOLDER BUMP SHAPE MEASURED PARALLEL TO DATUM A.

6. EXPOSED COPPER IS NOT ALLOWED ON THE LGA PAD.

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: FC LGA, 9.6 X 9.6 X 0.805 PKG, 0.5 MM PITCH, 211 I/O	DOCUMENT NO: 98ASA00988D	REV: C
	STANDARD: NON−JEDEC	
	SOT1868−1	06 DEC 2018

Figure 5. Package outline note VFLGA211 (SOT1868-1)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2019. All rights reserved.

3 Legal information

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

© NXP B.V. 2019. All rights reserved.

Contents

1 Package summary 1
2 Package outline 2
3 Legal information 7

© NXP B.V. 2019. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 11 January 2019