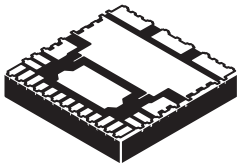
Document Number: MC10XS3412PNATAD
Rev 2.0, 05/2012

Quad High Side Switch (Dual 10 mOhm, Dual 12 mOhm)

10XS3412

24-PIN PQFN



98ARL10596D
24-PIN PQFN (12 x 12)

Note For package dimensions, refer to 98ARL10596D.

Thermal Addendum

Introduction

This thermal addendum is provided as a supplement to the 10XS3412 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application and packaging information is provided in the data sheet.

Package and Thermal Considerations

This 10XS3412 is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R_{\theta JAmn}$.

For *m*, *n* = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 1. Thermal Performance Comparison

Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$ (1)(2)	26.04	18.18	35.49
$R_{\theta JBmn}$ (2)(3)	13.21	6.40	23.94
$R_{\theta JAmn}$ (1)(4)	46.42	37.03	53.82
$R_{\theta JCmn}$ (5)	0.67	0.95	0.00

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.

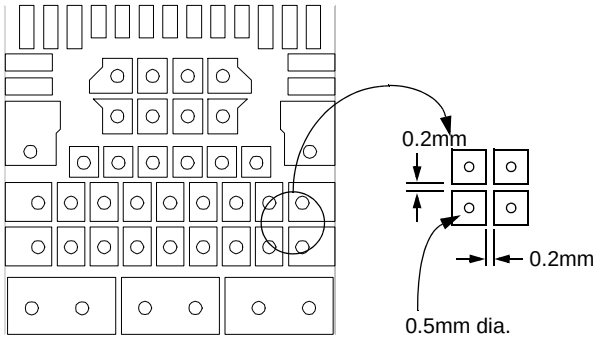


Figure 1. Detail of Copper Traces Under Device with Thermal Vias

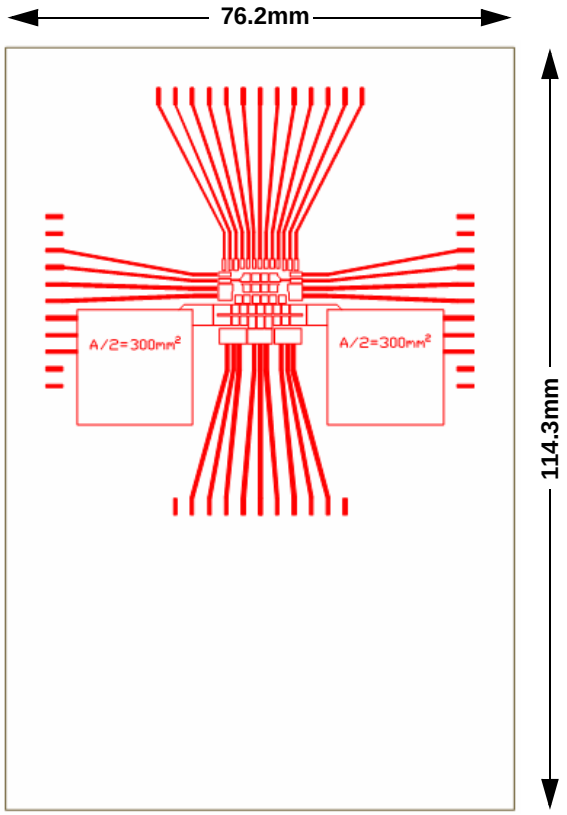


Figure 2. 1s JEDEC Thermal Test Board Layout

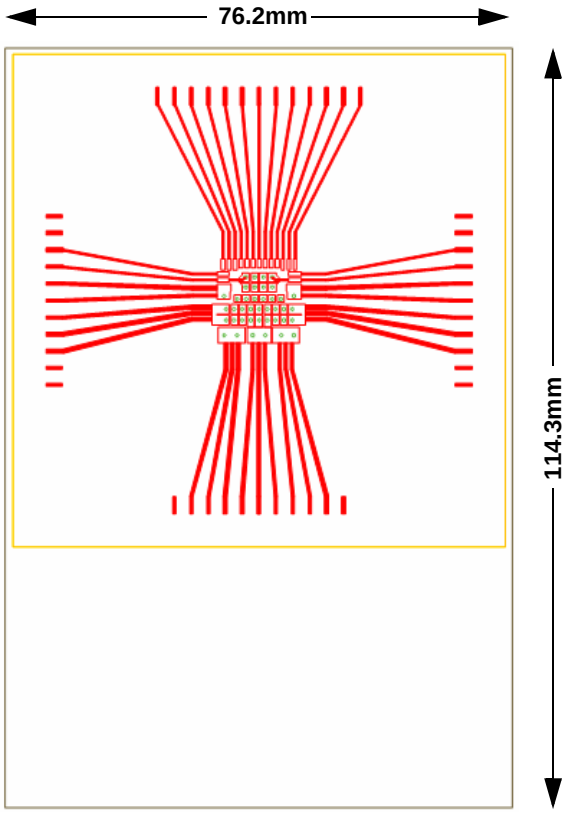
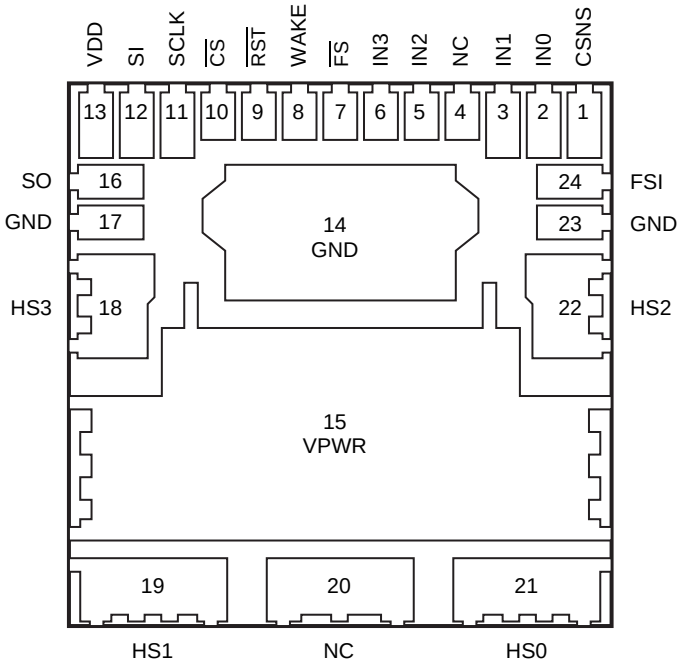


Figure 3. 2s2p JDEC Thermal Test Board (Red - Top Layer, Yellow - Two Buried Layers)

Transparent Top View



MC10XS3412 Pin Connections
24-PIN PQFN (12 x 12)
0.9 mm Pitch
12.0mm 12.0mm Body

Figure 4. Pin Connections

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness Cu buried traces thickness 0.035mm
Outline:	76.2mm x 114.3mm board area, including edge connector for thermal testing, 74mm x 74mm buried layers area
Area **A**:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 2. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$	0	46.42	37.03	53.82
	150	41.60	32.90	51.27
	300	40.02	31.63	55.05
	450	38.86	30.68	49.47
	600	38.04	29.99	48.63

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

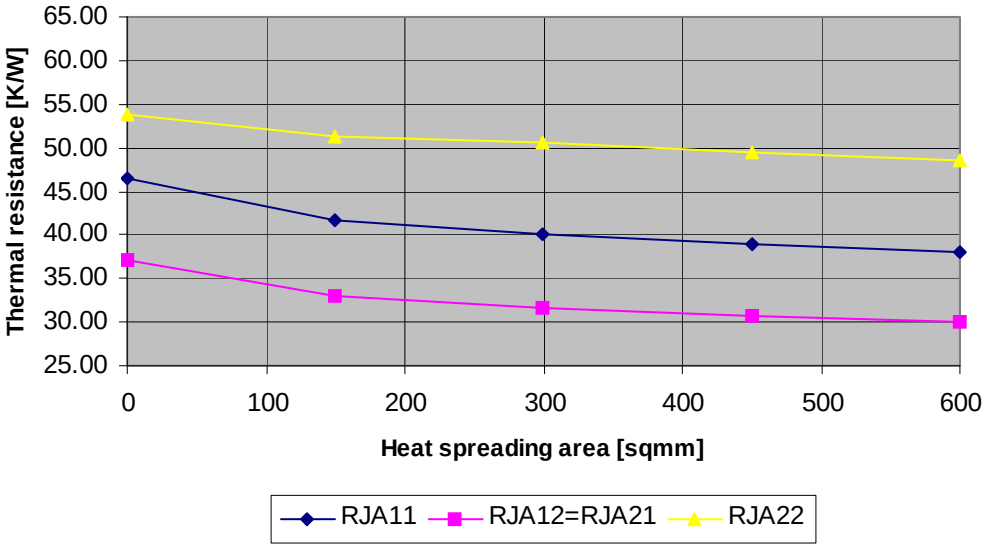


Figure 5. Steady State Thermal Resistance in Dependance on Heat Streading Area; 1s JEDEC Thermal Test Board with Spreading Areas

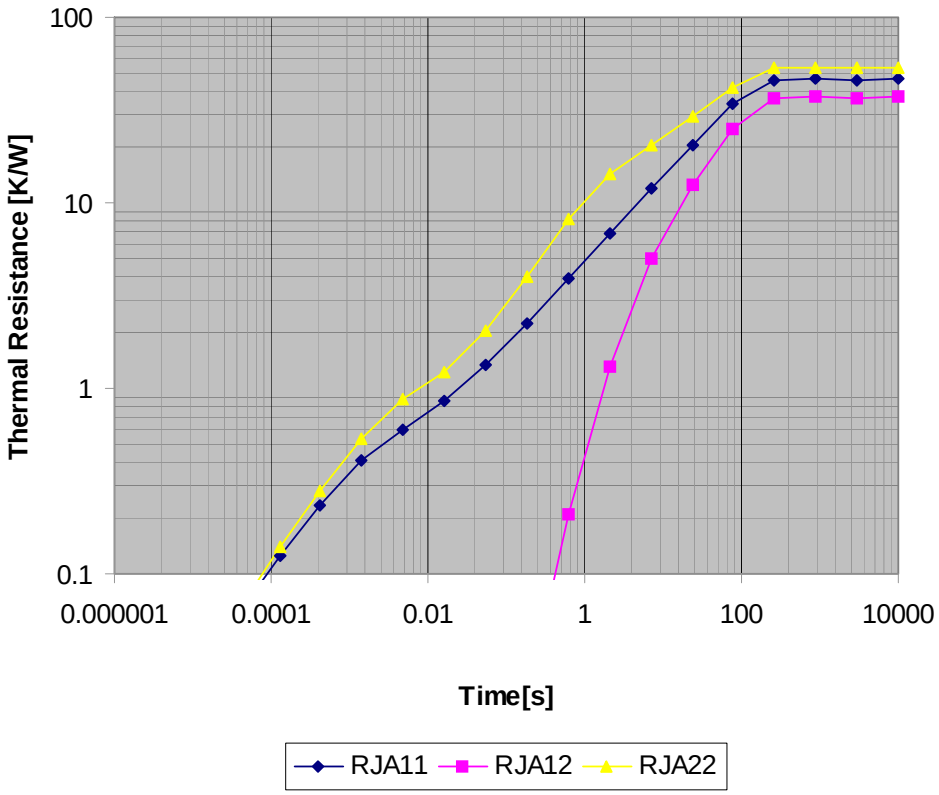


Figure 6. Transient Thermal 1W Step Response; Device on 1s JEDEC Standard Thermal Test Board with Heat Spreading Areas 600 Sq. mm

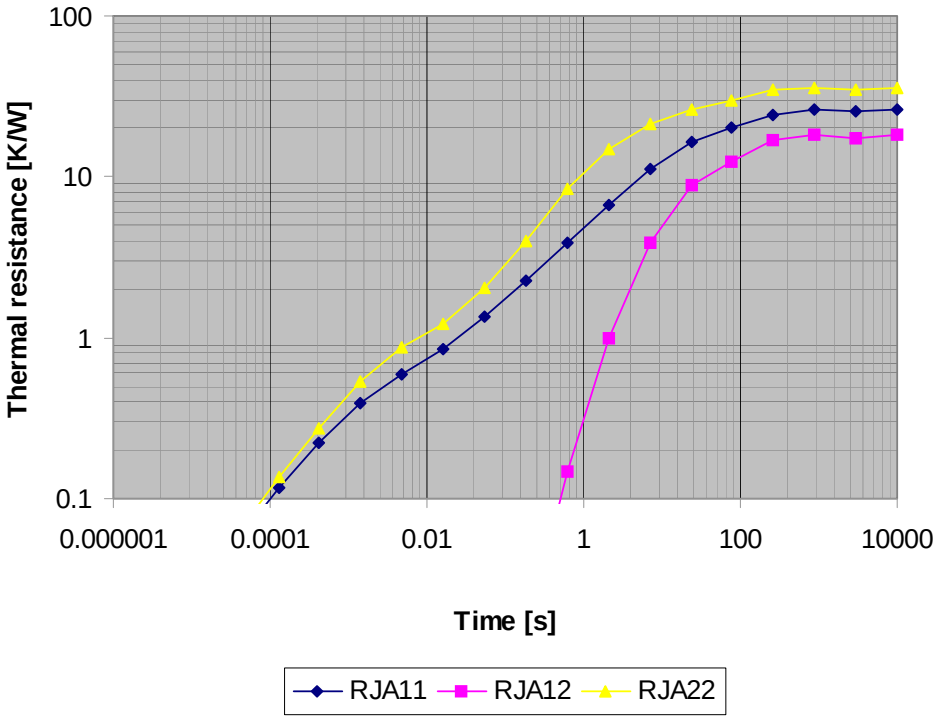


Figure 7. Transient Thermal 1W Step Response; Device on 2s2p JEDEC Standard Thermal Test Board

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer’s technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: http://www.reg.net/v2/webservices/Freescale/Docs/TermsandConditions.htm

Document Number: MC10XS3412PNATAD
Rev 2.0
05/2012