1. Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP16
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	9-2-2018
Manufacturer package code	98ASA01190D

Table 1. Package summary

Parameter		Min	Nom	Max	Unit
package length		-	1.84	-	mm
package width		-	1.84	-	mm
seated height		-	0.5	0.54	mm
nominal pitch		-	0.4	-	mm
actual quantity of termination		-	16	-	A/A

WLCSP16, wafer level chip-scale package; 16 bumps; 1.84 mm x 1.84 mm x 0.5 mm body

2. Package outline

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DATE: 24 MAY 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01190D	REVISION: A	
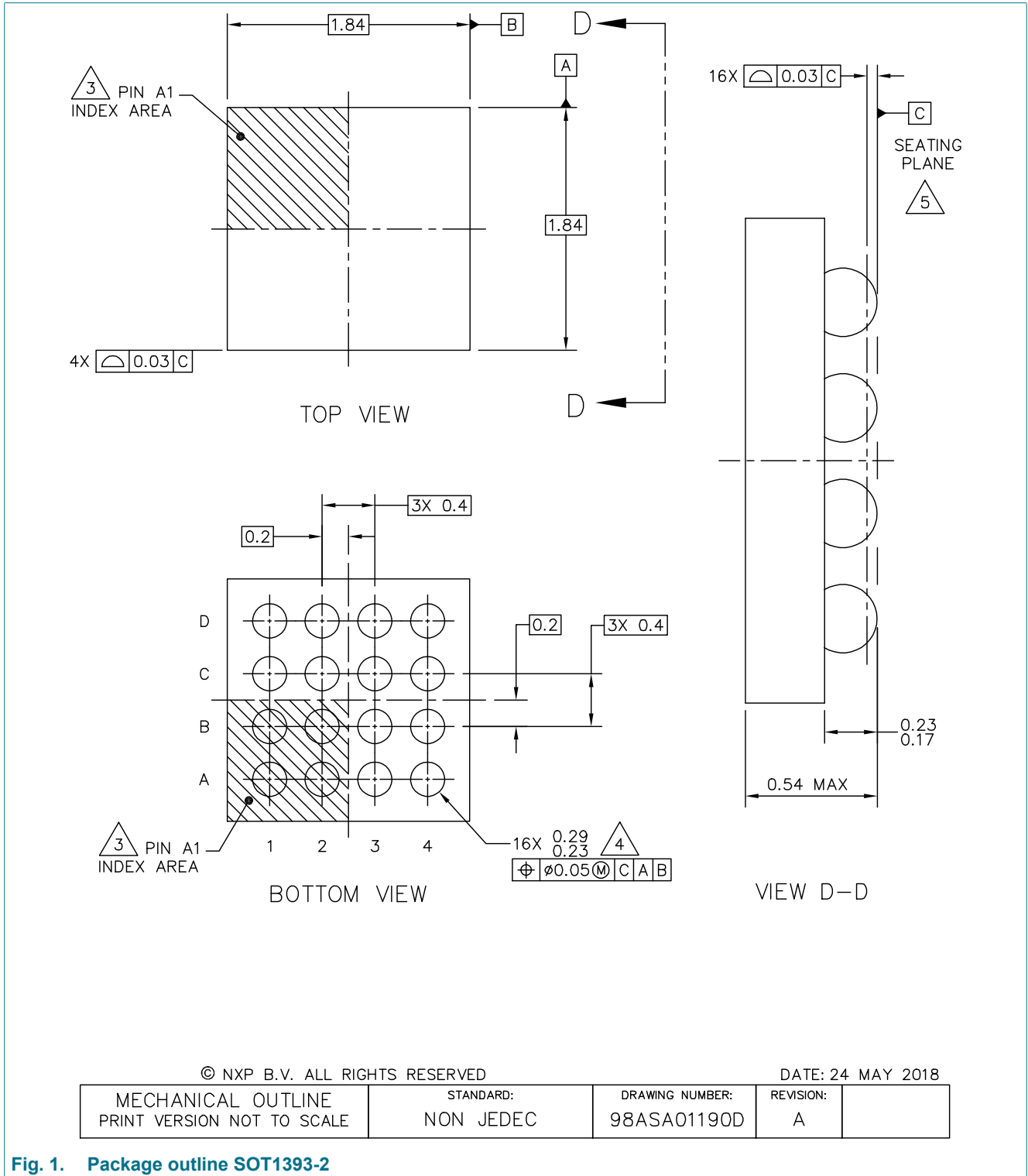
Fig. 1.   Package outline SOT1393-2

SOT1393-2

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Package information

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WLCSP16, wafer level chip-scale package; 16 bumps; 1.84 mm x 1.84 mm x 0.5 mm body

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

△3. PIN A1 CONFIGURATION MAY VARY.

△4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.

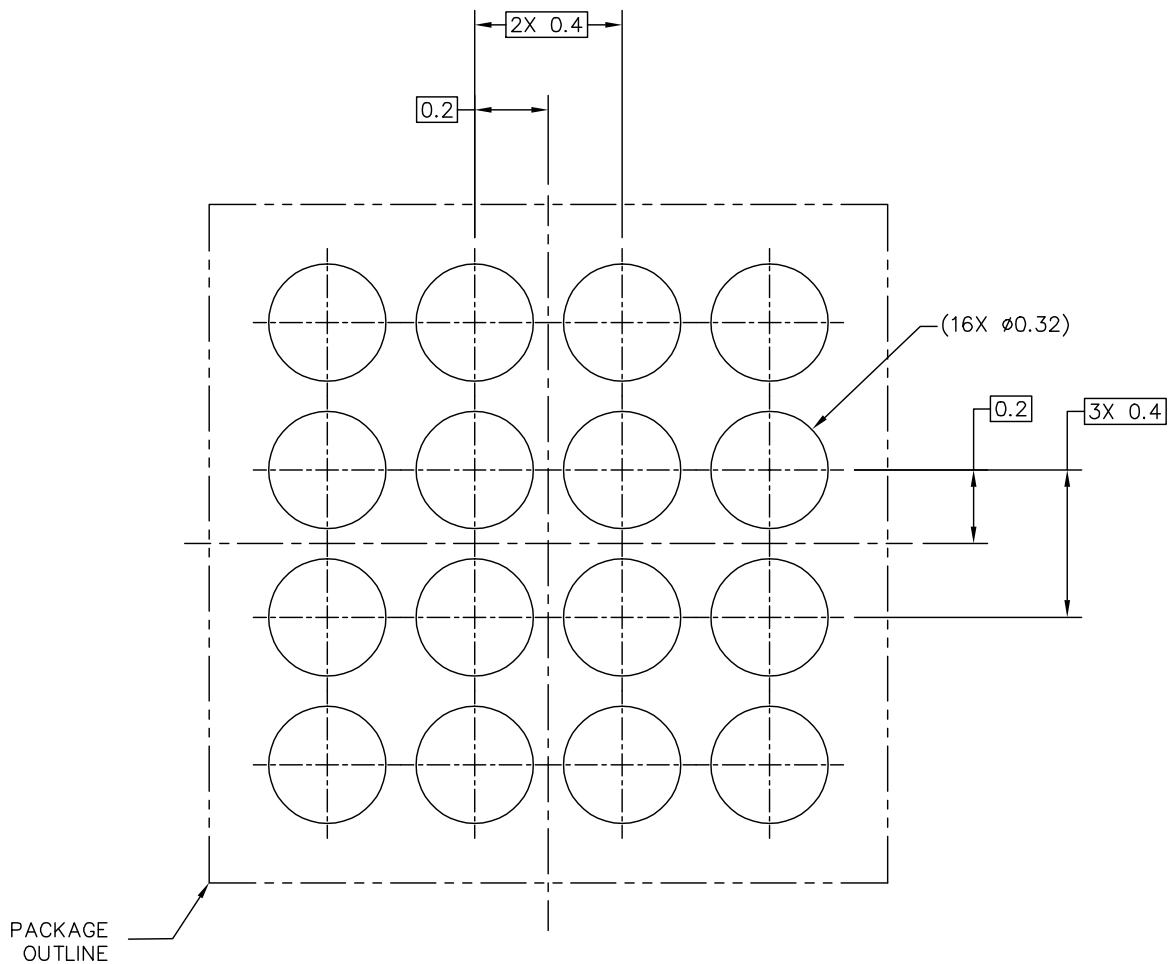△5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01190D	REVISION: A	

Fig. 2. Package outline note WLCSP16 (SOT1393-2)

3. Soldering

PACKAGE
OUTLINE

(16X ⌀0.32)

2X 0.4

0.2

0.2   3X 0.4

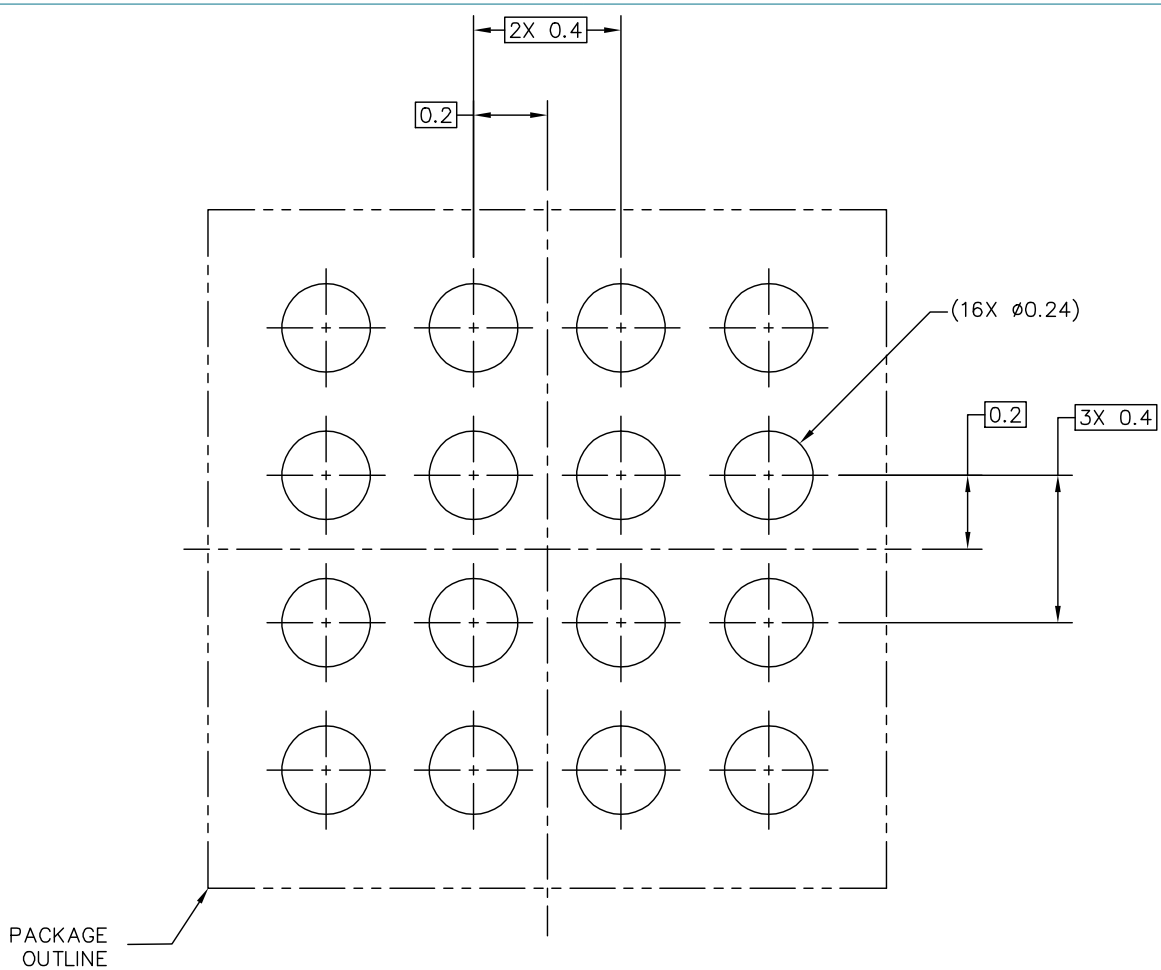PCB DESIGN GUIDELINES — SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION.
DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING
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| MECHANICAL OUTLINE
PRINT VERSION NOT TO SCALE | STANDARD:
NON JEDEC | DRAWING NUMBER:
98ASA01190D | REVISION:
A | |

Fig. 3.   Reflow soldering footprint for SOT1393-2

SOT1393-2

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WLCSP16, wafer level chip-scale package; 16 bumps; 1.84 mm x 1.84 mm x 0.5 mm body

2X 0.4

0.2

(16X ⌀0.24)

0.2   3X 0.4

PACKAGE
OUTLINE

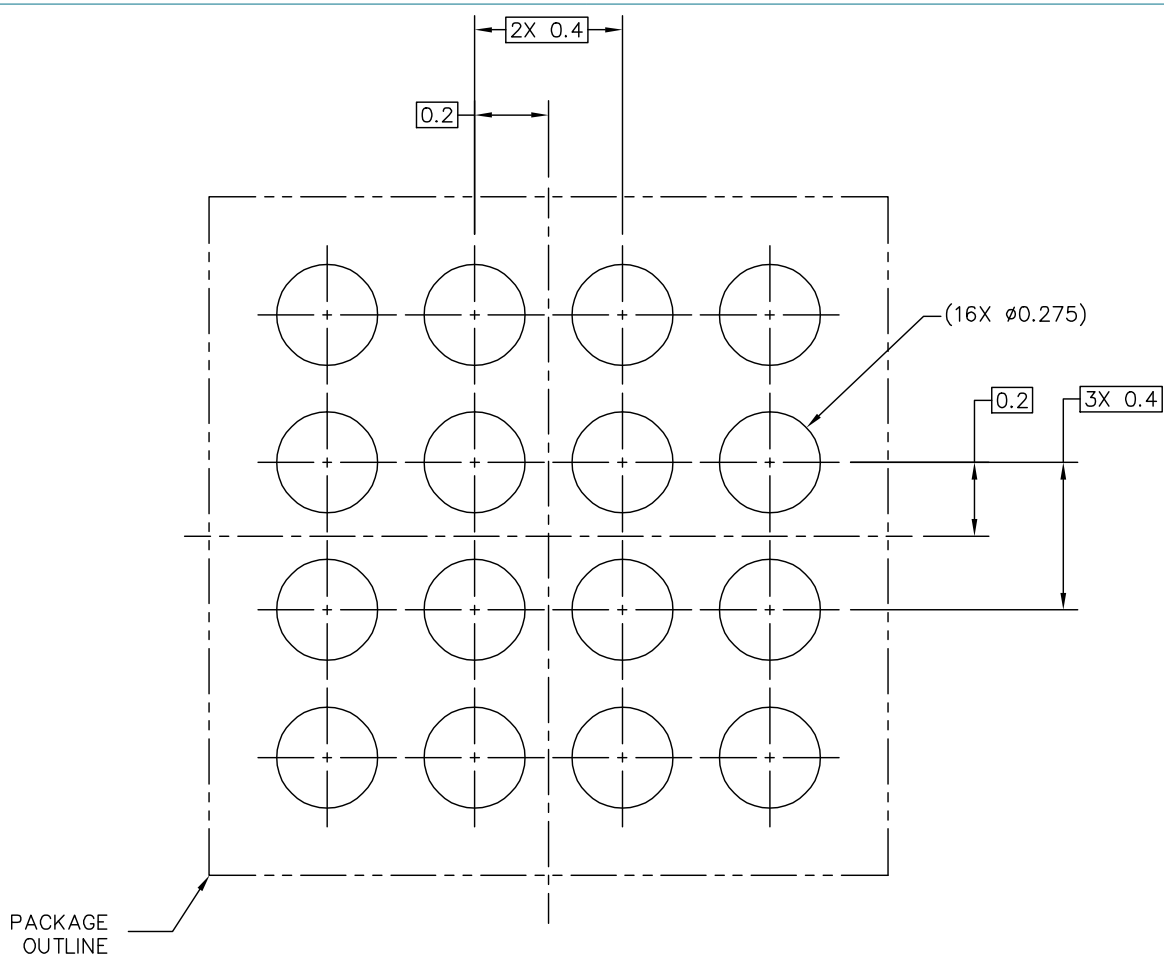PCB DESIGN GUIDELINES — I/O PADS AND SOLDERABLE AREA

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Fig. 4. Reflow soldering footprint part2 for WLCSP16 (SOT1393-2)

WLCSP16, wafer level chip-scale package; 16 bumps; 1.84 mm x 1.84 mm x 0.5 mm body

2X 0.4

0.2

(16X ⌀0.275)

0.2   3X 0.4

PACKAGE
OUTLINE

RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES — SOLDER PASTE STENCIL

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| MECHANICAL OUTLINE
PRINT VERSION NOT TO SCALE | STANDARD:
NON JEDEC | DRAWING NUMBER:
98ASA01190D | REVISION:
A | |

Fig. 5.   **Reflow soldering footprint part3 for WLCSP16 (SOT1393-2)**

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