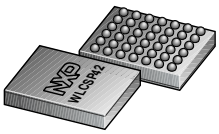


SOT1459-3

wafer level chip-scale package; 42 bumps; 3.13 x 2.46 x 0.525 mm

13 May 2016 **Package information**

1. Package summary

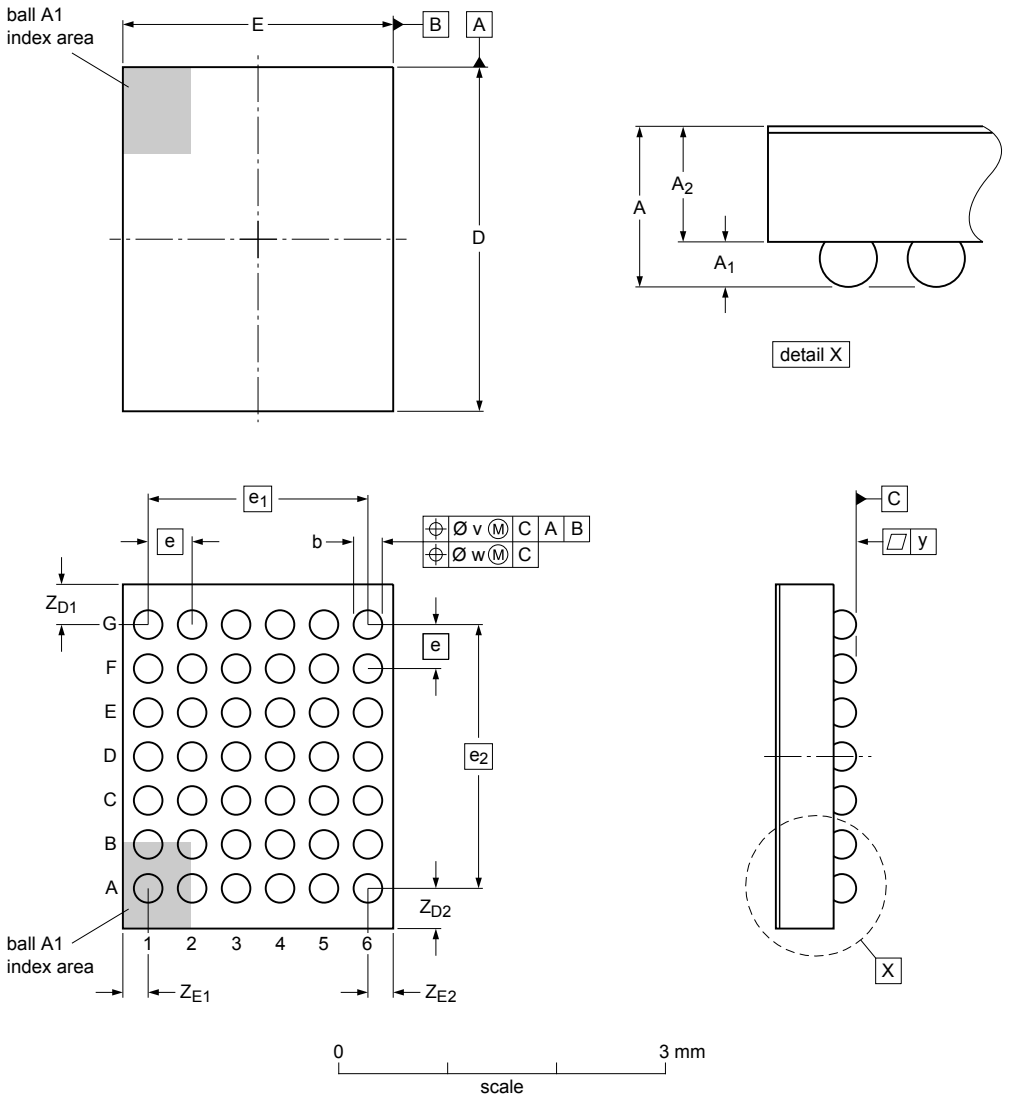
Terminal position code	B (bottom)
Package type descriptive code	WLCSP
Package type industry code	WLCSP42
Package style descriptive code	WLCSP (wafer level chip-size package)
Package style suffix code	NA (not applicable)
Mounting method type	S (surface mount)
Issue date	26-4-2016

Table 1. Package summary

Symbol	Parameter		Min	Typ	Nom	Max	Unit
D	package length		3.1	-	3.13	3.16	mm
E	package width		2.43	-	2.46	2.49	mm
A	seated height		0.485	-	0.525	0.565	mm
A_2	package height		-	-	0.33	-	mm
e	nominal pitch		-	-	0.4	-	mm
n_2	actual quantity of termination		-	-	42	-	

2. Package outline

WLCSP42: wafer level chip-scale package; 42 bumps; 3.13 x 2.46 x 0.525 mm (backside coating included) **SOT1459-3**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	Z_{D1}	Z_{D2}	Z_{E1}	Z_{E2}	v	w	y
mm	max	0.565				3.16	2.49										
	nom	0.525	0.20	0.33	0.26	3.13	2.46	0.4	2.0	2.4	0.365	0.365	0.245	0.215	0.05	0.02	0.03
	min	0.485				3.10	2.43										

Note: Backside coating 25 µm

sot1459-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1459-3		- - -				~~16-03-01~~ 16-05-09

Fig. 1. Package outline WLCSP42 (SOT1459-3)

3. Legal information

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