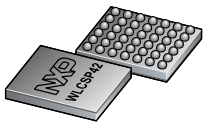


SOT1459-6

WLCSP42, wafer level chip-scale package; 42 bumps; 2.91 mm x 2.51 mm x 0.525 mm body (backside coating included)

27 March 2018 Package information

1. Package summary

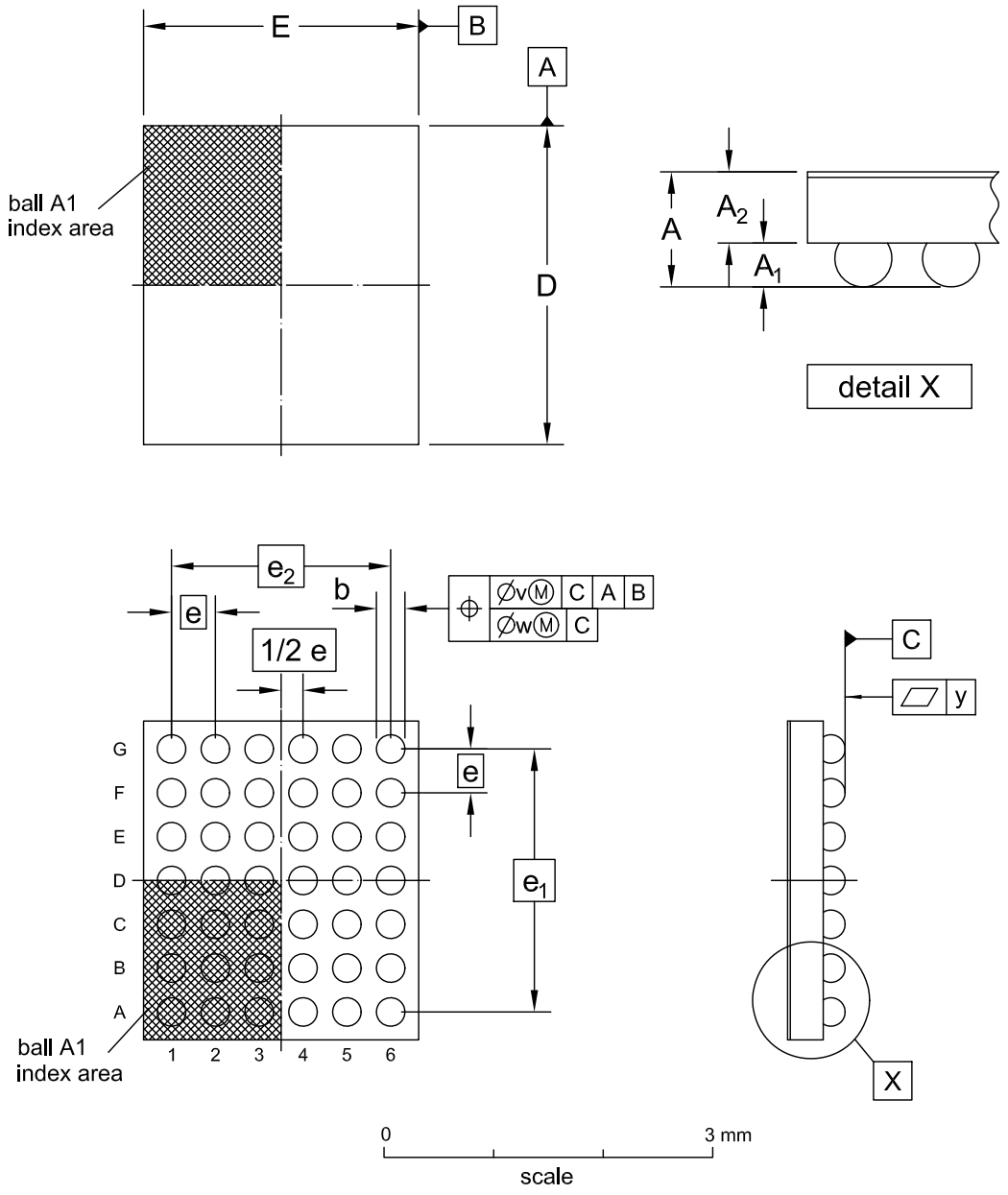
Terminal position code	B (bottom)
Package type descriptive code	WLCSP
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	28-7-2017
Manufacturer package code	SOT1459-6

Table 1. Package summary

Symbol	Parameter		Min	Typ	Nom	Max	Unit
D	package length		2.88	-	2.91	2.94	mm
E	package width		2.48	-	2.51	2.54	mm
A	seated height		0.485	-	0.525	0.565	mm
A_2	package height		0.3	-	0.325	0.35	mm
e	nominal pitch		-	-	0.4	-	mm
n_2	actual quantity of termination		-	-	42	-	A/A

WLCSP42, wafer level chip-scale package; 42 bumps; 2.91 mm x 2.51 mm x 0.525 mm body (backside coating included)

2. Package outline



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	MAX.	0.565	0.23	0.350	0.29	2.94	2.54	0.4	2.4	2.0	0.05	0.02	0.03
	NOM.	0.525	0.20	0.325	0.26	2.91	2.51						
	MIN.	0.485	0.17	0.300	0.23	2.88	2.48						

NOTE: Backside coating 25 um

Fig. 1. Package outline SOT1459-6

3. Soldering

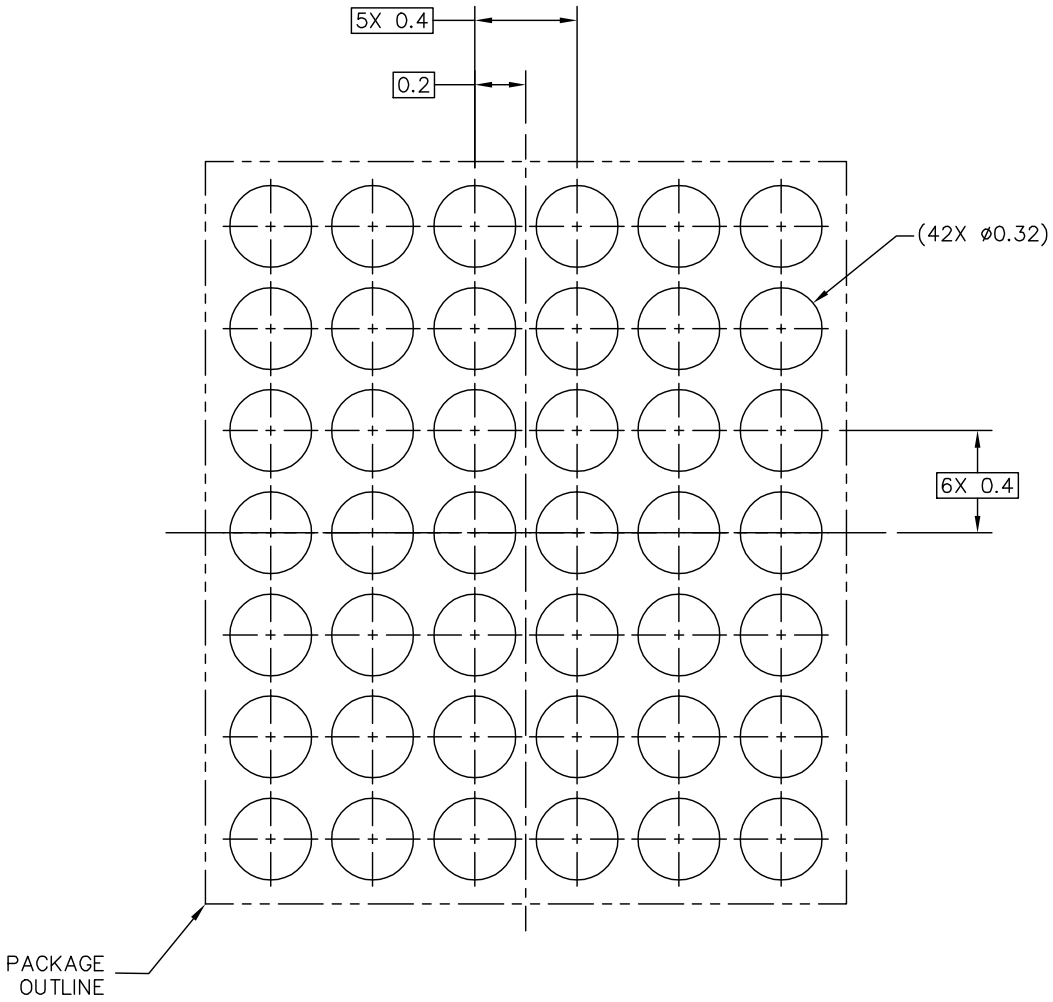


Fig. 2. Reflow soldering footprint for SOT1459-6

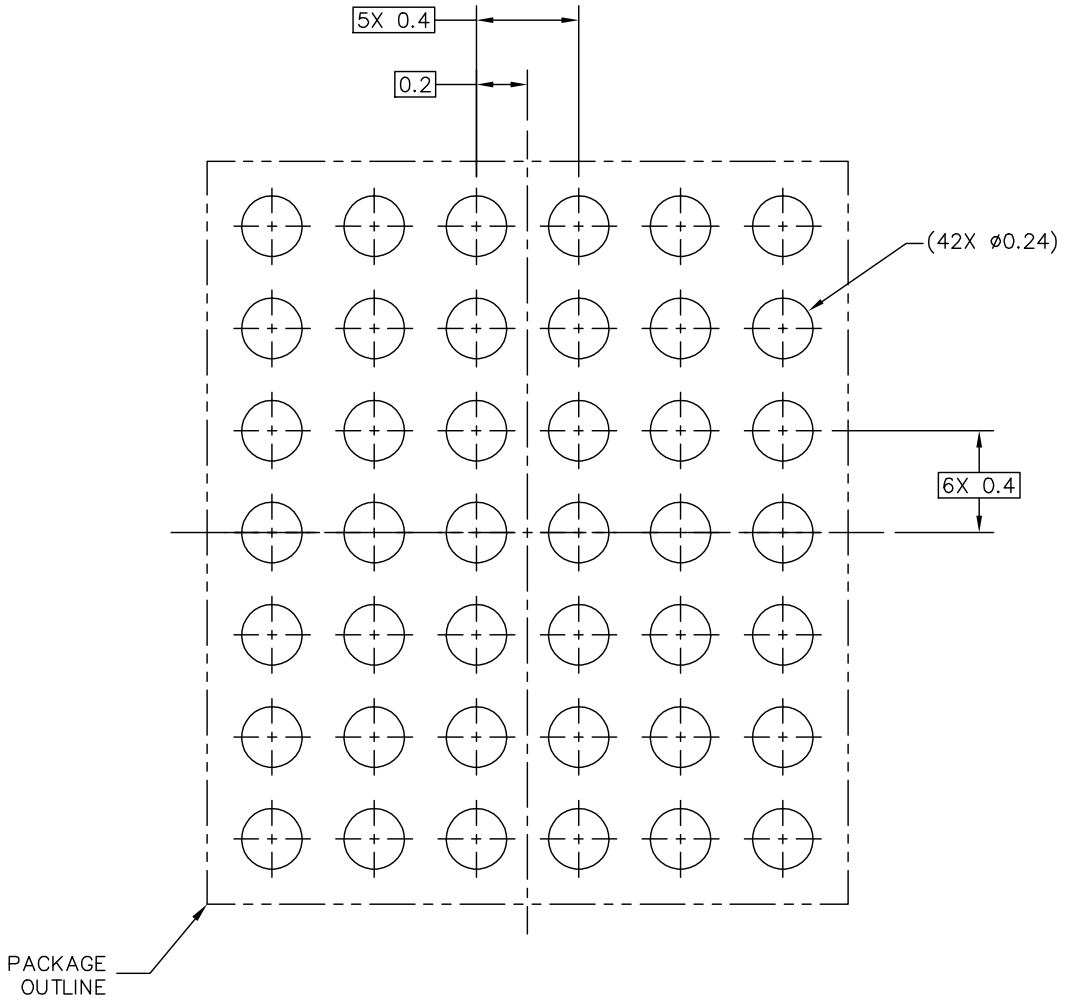


Fig. 3. Reflow soldering footprint part2 for WLCSP42 (SOT1459-6)

WLCSP42, wafer level chip-scale package; 42 bumps; 2.91 mm x 2.51 mm x 0.525 mm body (backside coating included)

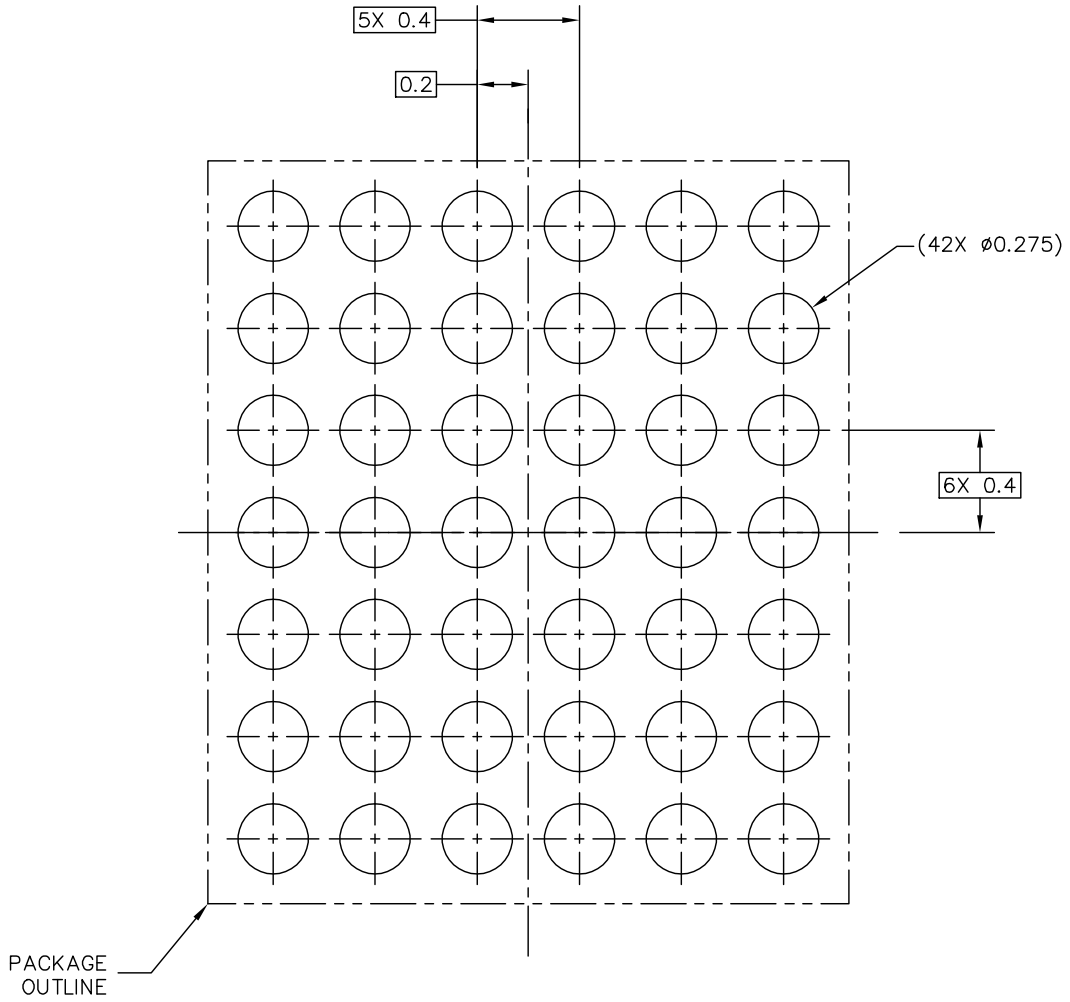


Fig. 4. Reflow soldering footprint part3 for WLCSP42 (SOT1459-6)

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5. Contents

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Date of release: 27 March 2018