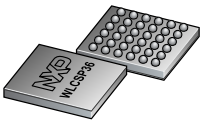


SOT1780-13

WLCSP36, wafer level chip-scale package, 36 terminals, 0.4 mm pitch, 2.79 mm x 2.59 mm x 0.525 mm body

6 May 2019 Package information

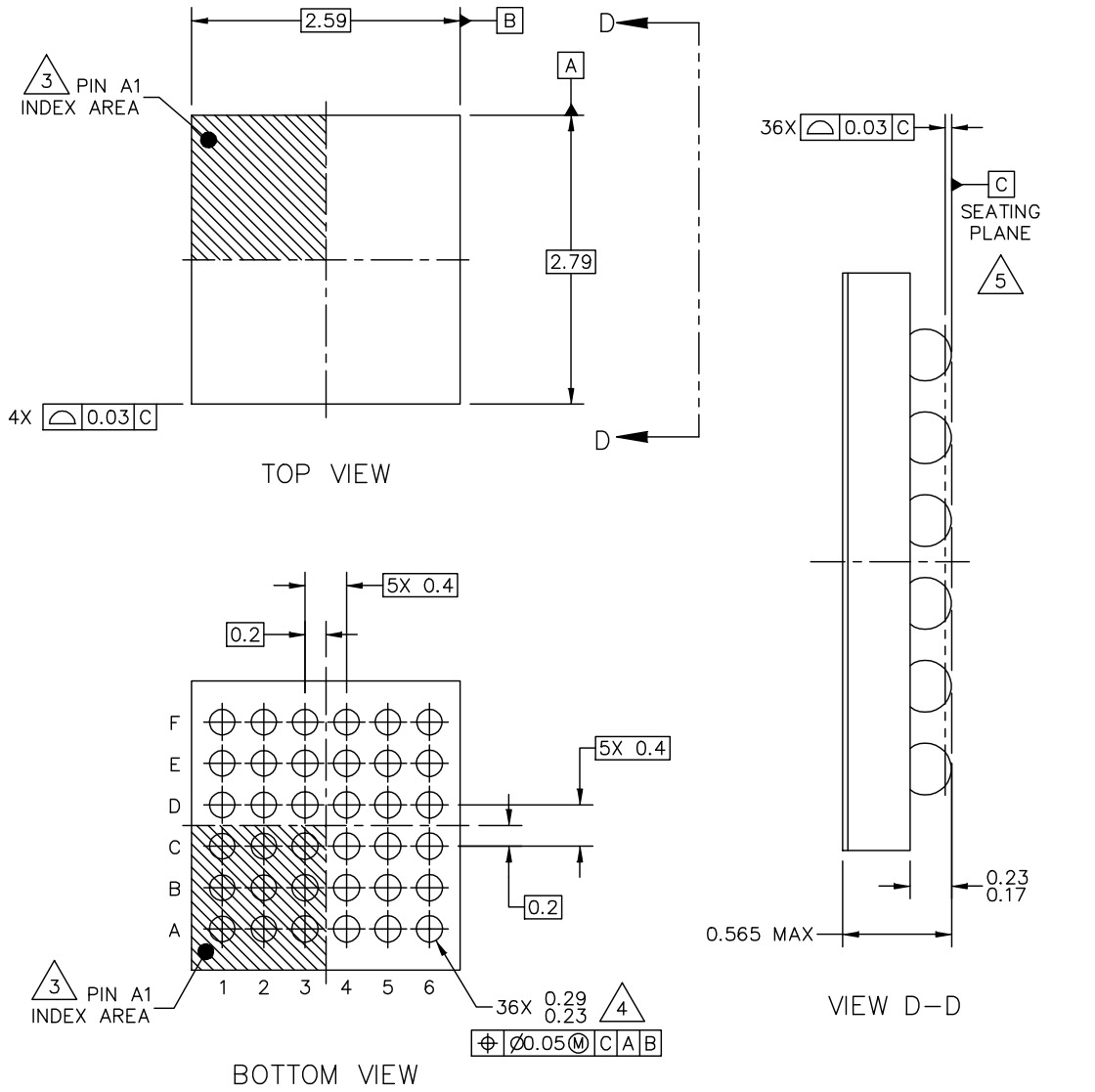
1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP36
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	18-04-2019
Manufacturer package code	98ASA01425D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	2.79	-	mm
package width	-	2.59	-	mm
package height	-	0.525	-	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	36	-	

2 Package outline



DATE: 18 APR 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01425D	REVISION: O	

Figure 1. Package outline WLCSP36 (SOT1780-13)

3 Soldering

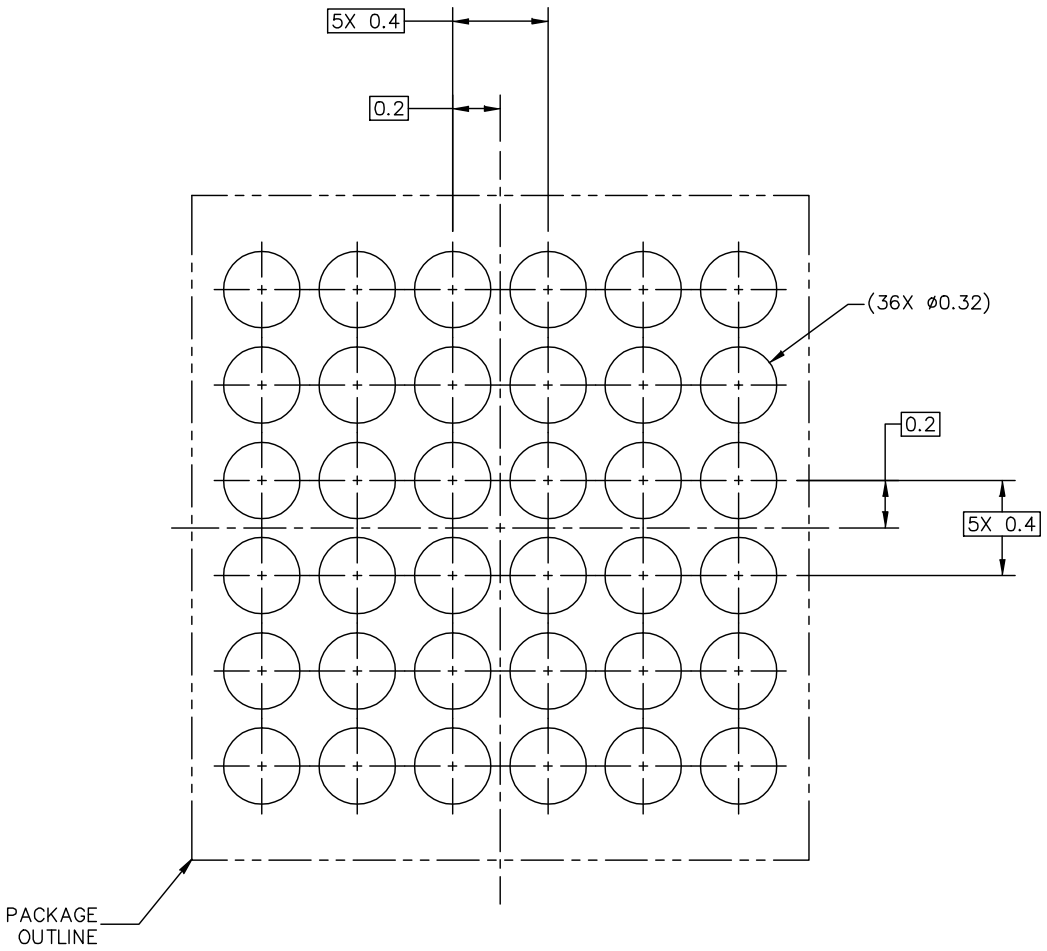
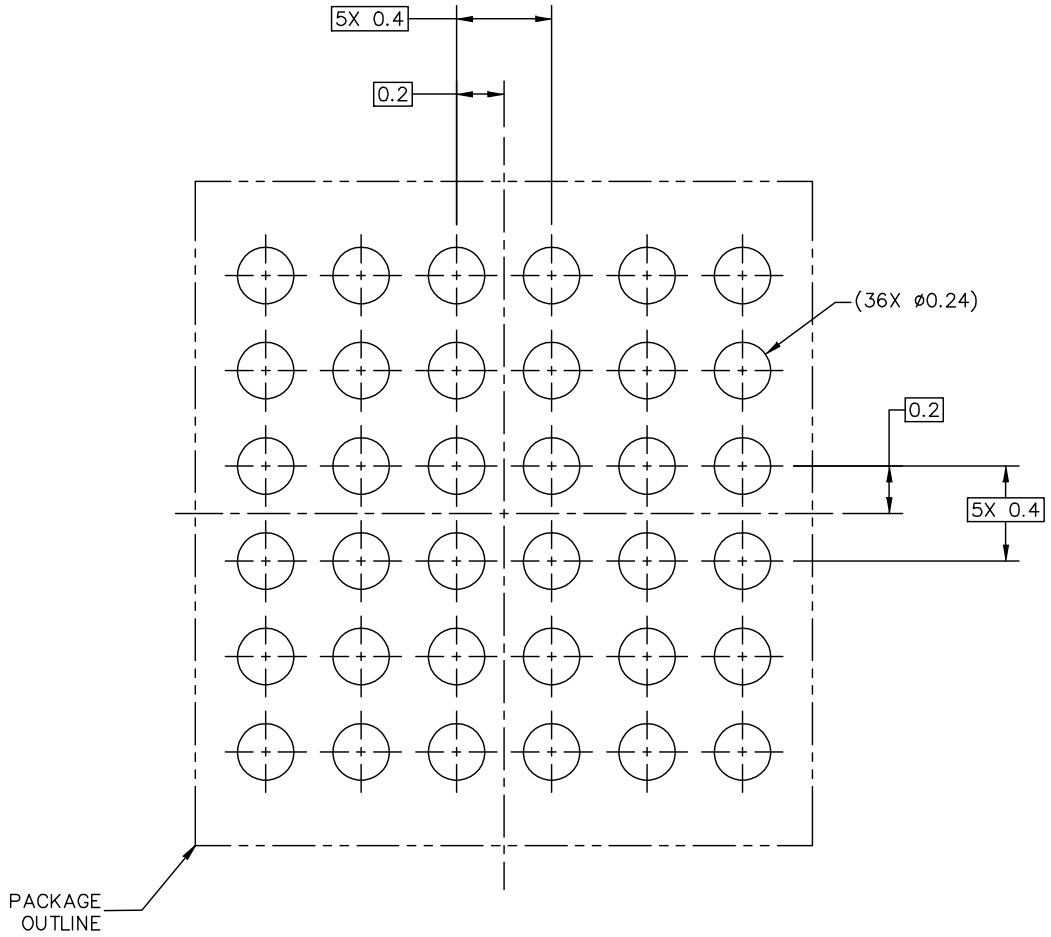


Figure 2. Reflow soldering footprint part1 for WLCSP36 (SOT1780-13)



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 18 APR 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01425D	REVISION: O	

Figure 3. Reflow soldering footprint part2 for WLCSP36 (SOT1780-13)

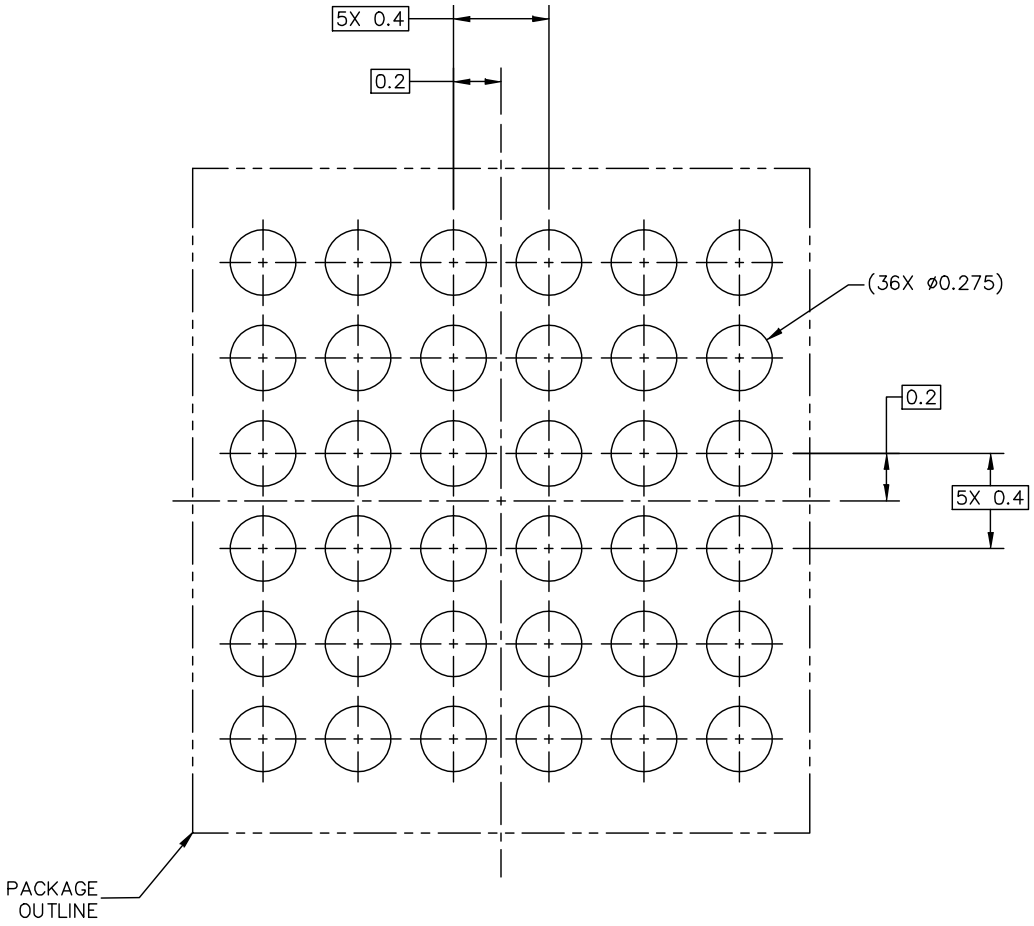


Figure 4. Reflow soldering footprint part3 for WLCSP36 (SOT1780-13)

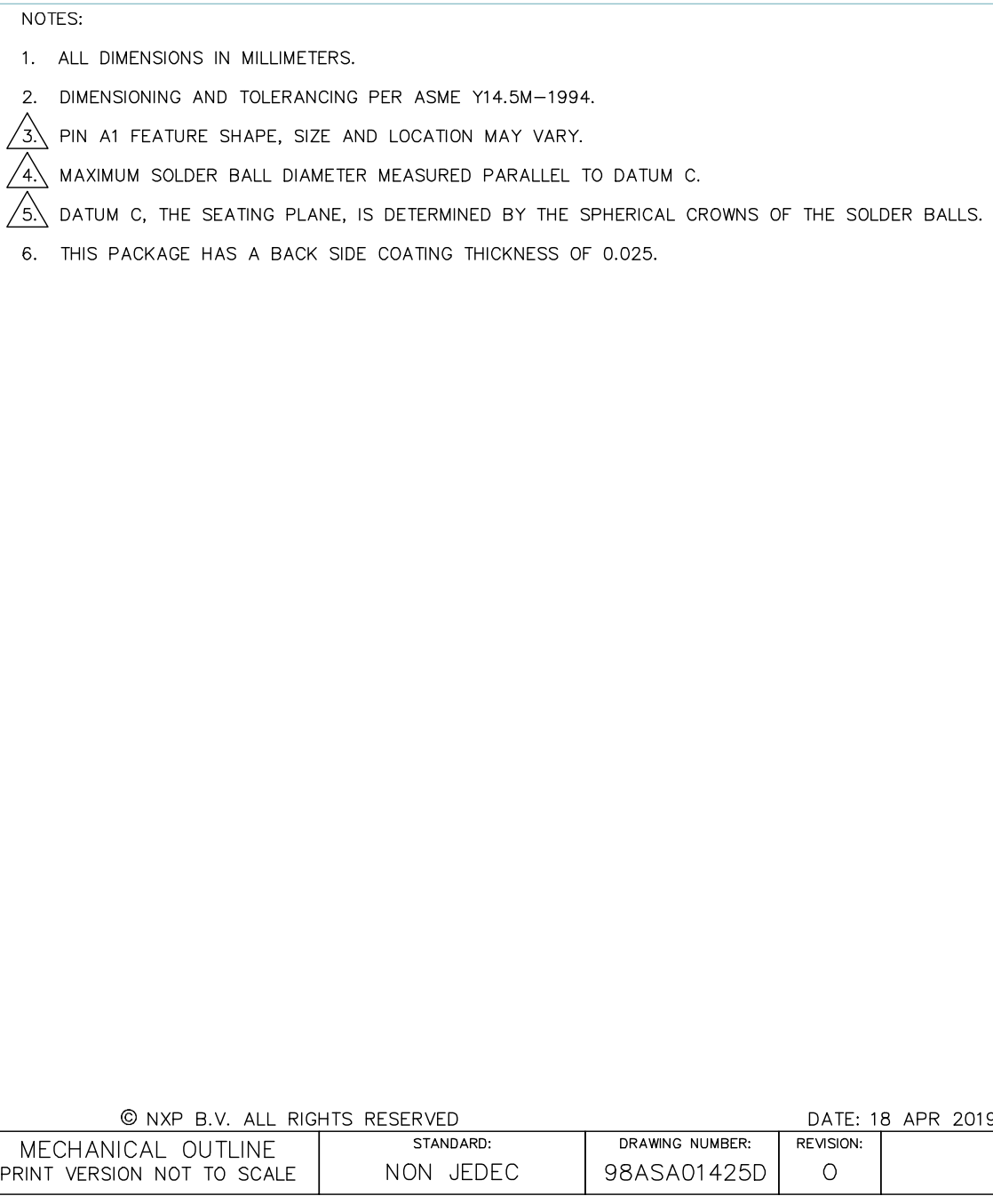


Figure 5. Package outline note WLCSP36 (SOT1780-13)

4 Legal information

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SOT1780-13

WLCSP36, wafer level chip-scale package, 36 terminals, 0.4 mm pitch, 2.79 mm x 2.59 mm x 0.525 mm body

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 6 May 2019