

SOT1975-2

WLCSP68, wafer level chip-scale package, 68 terminals; 0.35 mm pitch, 3.78 mm x 3.06 mm x 0.325 mm body (backside coating included)

6 January 2020

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP68
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	25-11-2019
Manufacturer package code	98ASA01559D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	3.75	3.78	3.81	mm
package width	3.03	3.06	3.09	mm
seated height	-	0.325	0.35	mm
nominal pitch	-	0.35	-	mm
actual quantity of termination	-	68	-	



WLCSP68, wafer level chip-scale package, 68 terminals; 0.35 mm pitch, 3.78 mm x 3.06 mm x 0.325 mm body (backside coating included)

2 Package outline

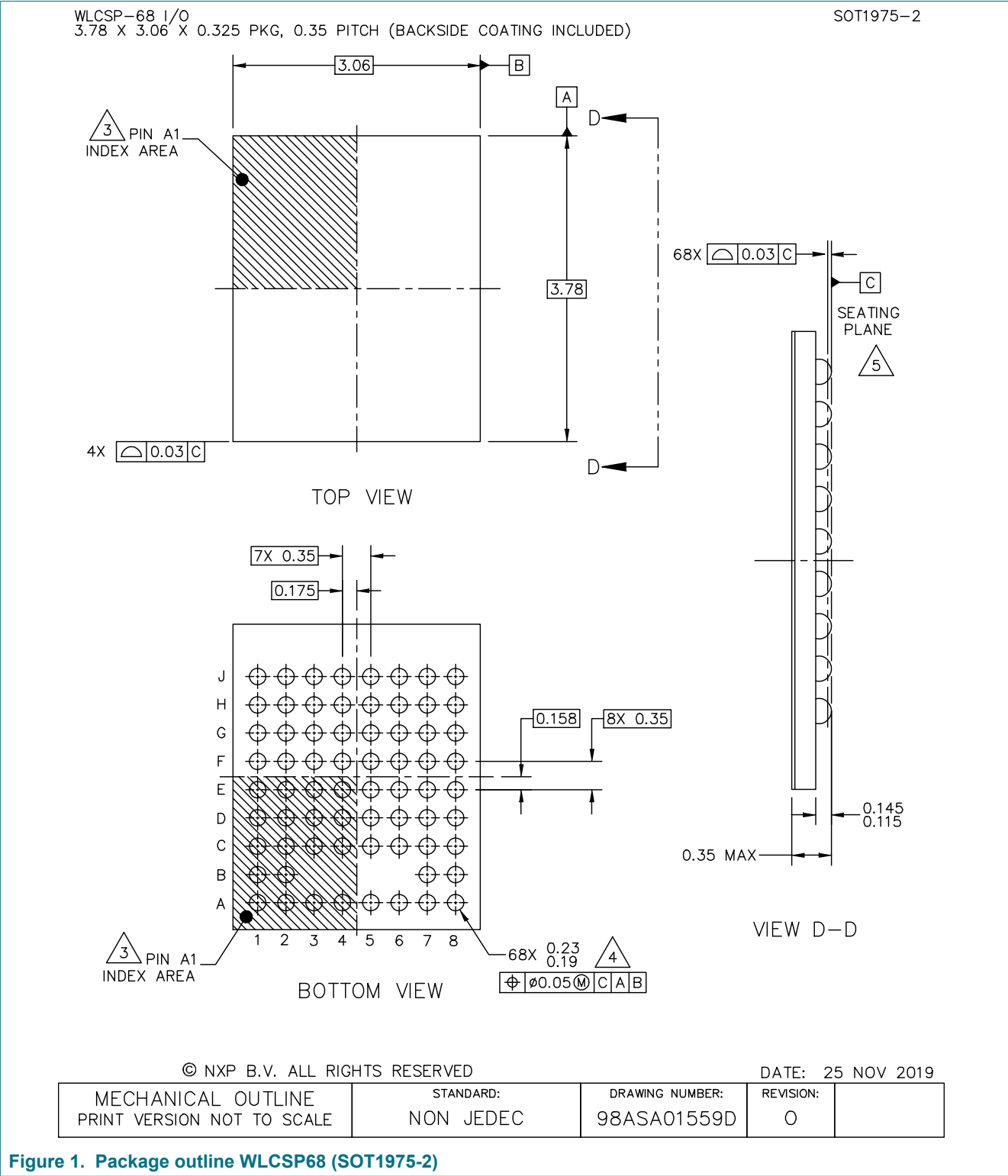


Figure 1. Package outline WLCSP68 (SOT1975-2)

WLCSP68, wafer level chip-scale package, 68 terminals; 0.35 mm pitch, 3.78 mm x 3.06 mm x 0.325 mm body (backside coating included)

3 Soldering

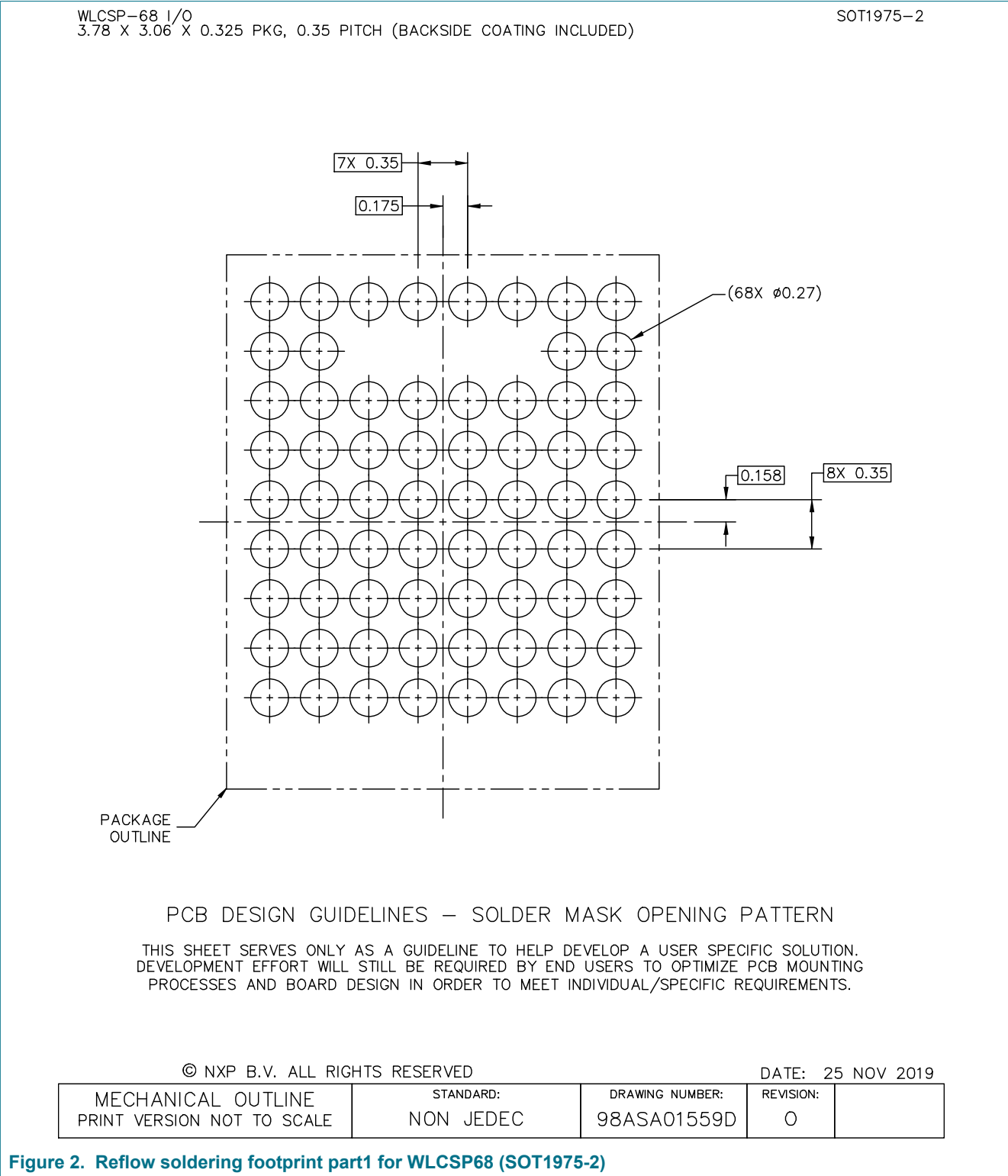
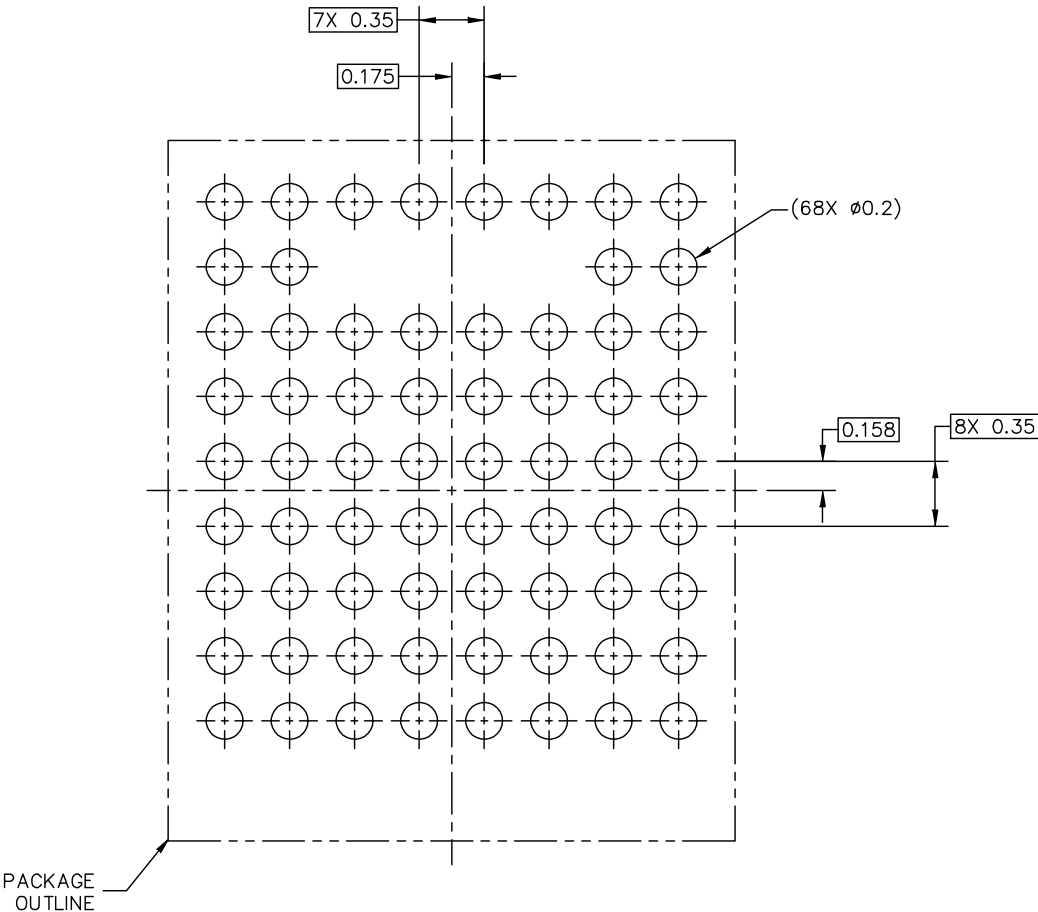


Figure 2. Reflow soldering footprint part1 for WLCSP68 (SOT1975-2)

WLCSP68, wafer level chip-scale package, 68 terminals; 0.35 mm pitch, 3.78 mm x 3.06 mm x 0.325 mm body (backside coating included)

WLCSP-68 I/O
3.78 X 3.06 X 0.325 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT1975-2



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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DATE: 25 NOV 2019

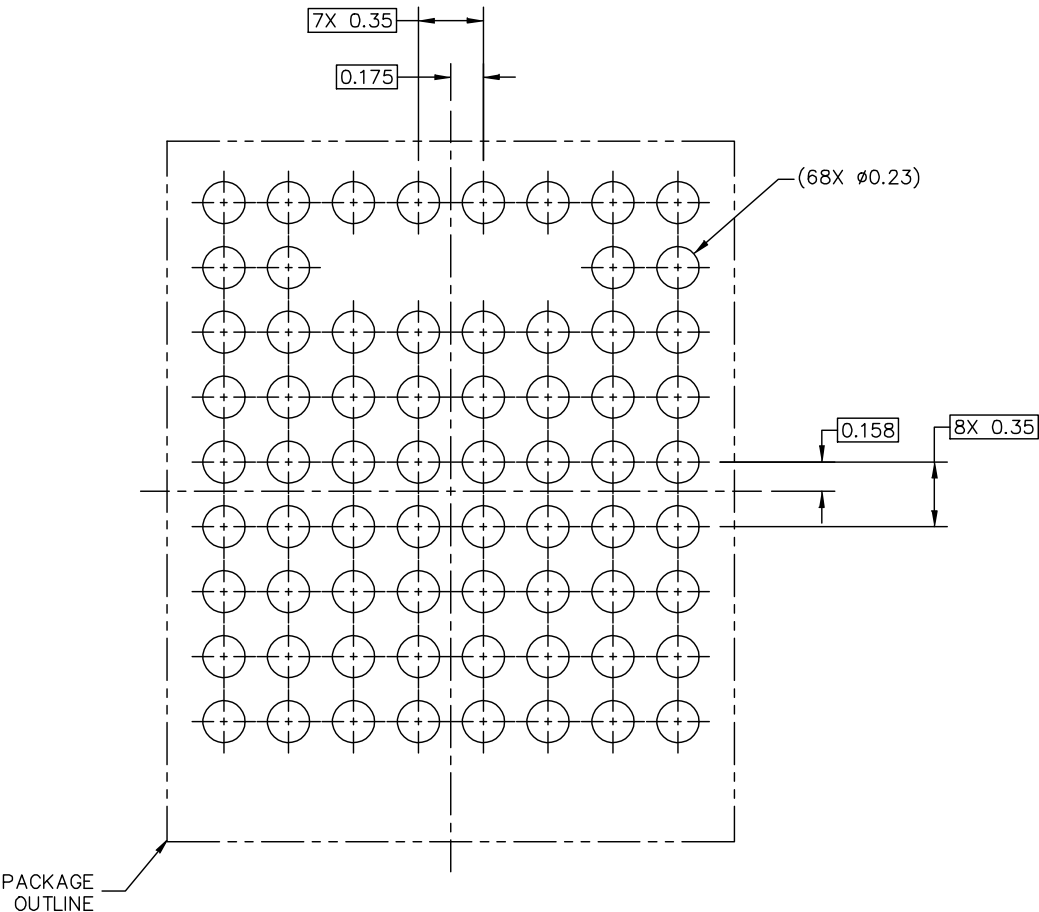
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01559D	REVISION: 0	
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Figure 3. Reflow soldering footprint part2 for WLCSP68 (SOT1975-2)

WLCSP68, wafer level chip-scale package, 68 terminals; 0.35 mm pitch, 3.78 mm x 3.06 mm x 0.325 mm body (backside coating included)

WLCSP-68 I/O
3.78 X 3.06 X 0.325 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT1975-2



RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 4. Reflow soldering footprint part3 for WLCSP68 (SOT1975-2)

WLCSP68, wafer level chip-scale package, 68 terminals; 0.35 mm pitch, 3.78 mm x 3.06 mm x 0.325 mm body (backside coating included)

WLCSP-68 I/O
3.78 X 3.06 X 0.325 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT1975-2

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
- 5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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Figure 5. Package outline note WLCSP68 (SOT1975-2)

WLCSP68, wafer level chip-scale package, 68 terminals; 0.35 mm pitch, 3.78 mm x 3.06 mm x 0.325 mm
body (backside coating included)

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