SOT2028-1

WLCSP48, wafer level chip-scale package; 48 bumps; 0.4 mm pitch, 3.15 mm x 2.89 mm x 0.38 mm body

2 June 2021

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP48
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	28-05-2021
Manufacturer package code	98ASA01467D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	3.12	3.15	3.18	mm
package width	2.86	2.89	2.92	mm
package height	-	0.38	0.41	
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	48	-	

2 Package outline

WLCSP-48 I/O
3.15 X 2.89 X 0.38 PKG, 0.4 PITCH

SOT2028-1

TOP VIEW

BOTTOM VIEW

VIEW D-D

RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND
ASSEMBLY RULES. MUST BE REVIEWED AND UPDATED BEFORE BEING ASSEMBLED INTERNALLY.

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DATE: 28 MAY 2021

| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA01467D | REVISION: C |

Figure 1. Package outline WLCSP48 (SOT2028-1)

SOT2028-1

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Package information

2 June 2021

2 / 8

WLCSP48, wafer level chip-scale package; 48 bumps; 0.4 mm pitch, 3.15 mm x 2.89 mm x 0.38 mm body

3   Soldering

WLCSP−48 I/O
3.15 X 2.89 X 0.38 PKG, 0.4 PITCH

SOT2028−1

6X 0.4

0.081

(48X ⌀0.17)

0.47

0.547

0.005

(CENTER OF BUMP
BELOW PACKAGE
CENTER LINE)

4X 0.43

PACKAGE
OUTLINE

PCB DESIGN GUIDELINES − SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION.
DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING
PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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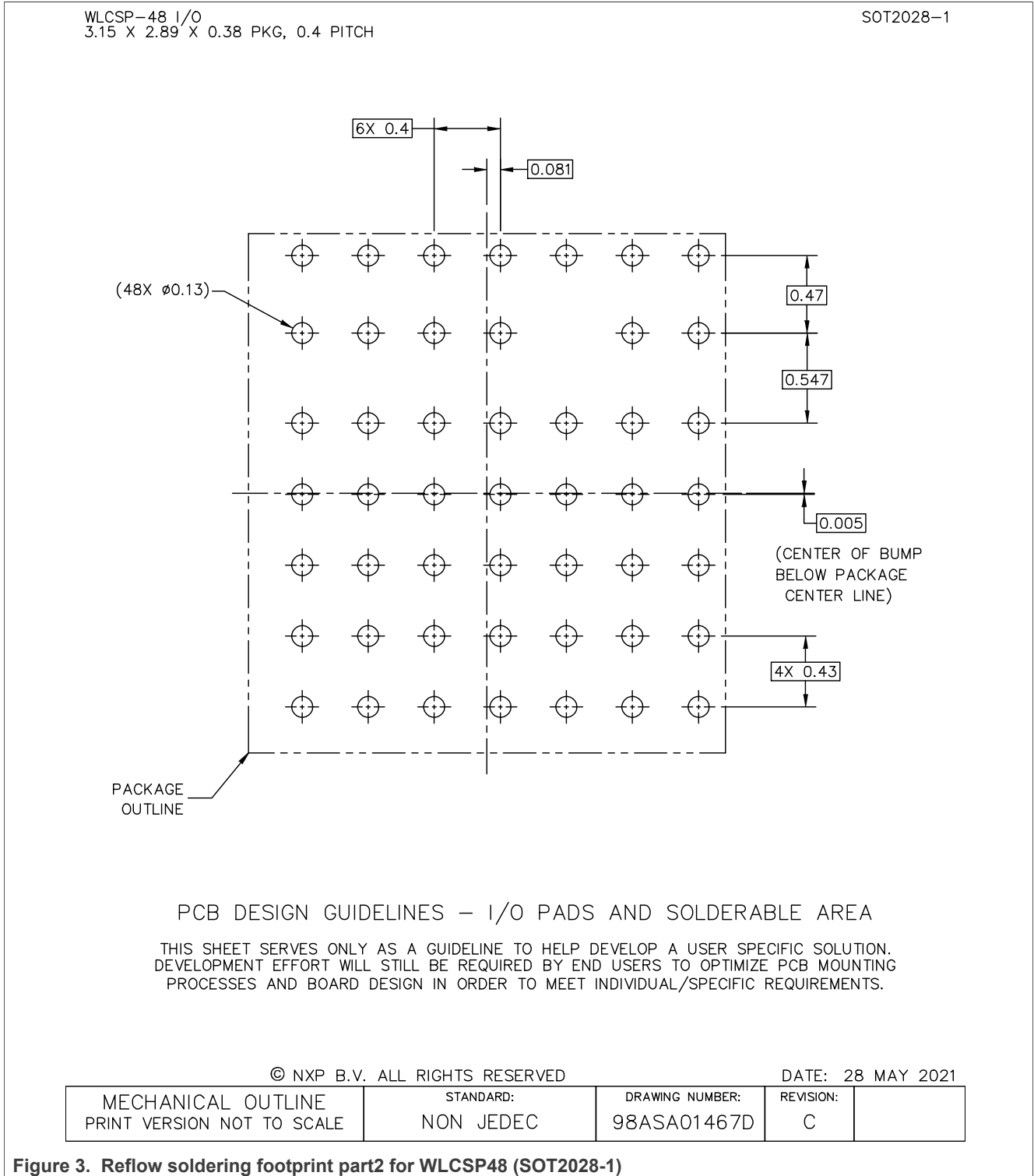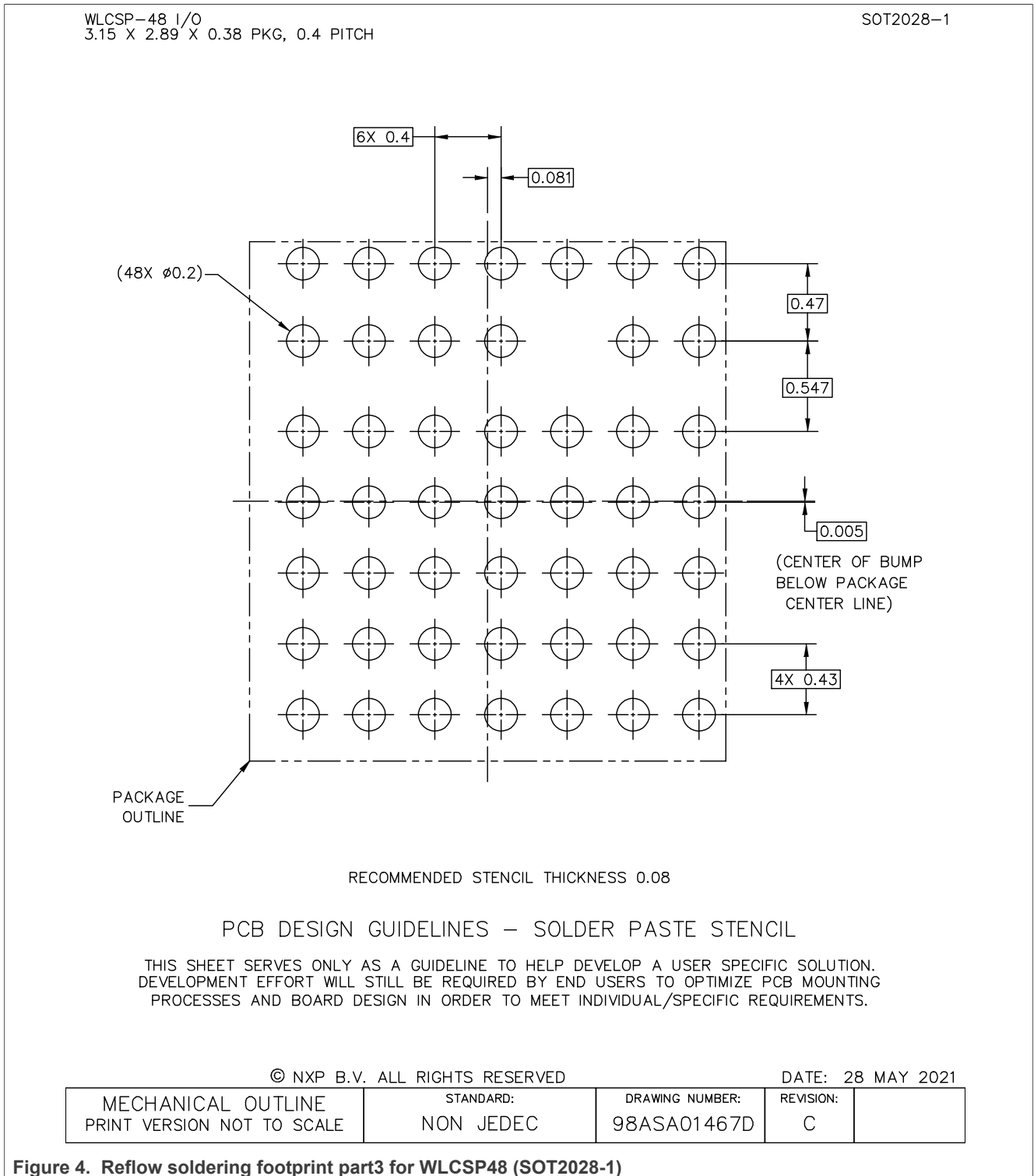| MECHANICAL OUTLINE
PRINT VERSION NOT TO SCALE | STANDARD:
NON JEDEC | DRAWING NUMBER:
98ASA01467D | REVISION:
C | |

Figure 2. Reflow soldering footprint part1 for WLCSP48 (SOT2028-1)

WLCSP48, wafer level chip-scale package; 48 bumps; 0.4 mm pitch, 3.15 mm x 2.89 mm x 0.38 mm body

WLCSP-48 I/O
3.15 X 2.89 X 0.38 PKG, 0.4 PITCH

SOT2028-1

6X 0.4

0.081

(48X ⌀0.13)

0.47

0.547

0.005

(CENTER OF BUMP
BELOW PACKAGE
CENTER LINE)

4X 0.43

PACKAGE
OUTLINE

PCB DESIGN GUIDELINES — I/O PADS AND SOLDERABLE AREA

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Figure 3. Reflow soldering footprint part2 for WLCSP48 (SOT2028-1)

SOT2028-1

Package information

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2 June 2021

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4 / 8

WLCSP48, wafer level chip-scale package; 48 bumps; 0.4 mm pitch, 3.15 mm x 2.89 mm x 0.38 mm body

WLCSP-48 I/O
3.15 X 2.89 X 0.38 PKG, 0.4 PITCH

SOT2028-1

6X 0.4

0.081

(48X ⌀0.2)

0.47

0.547

0.005

(CENTER OF BUMP
BELOW PACKAGE
CENTER LINE)

4X 0.43

PACKAGE
OUTLINE

RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES — SOLDER PASTE STENCIL

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| PRINT VERSION NOT TO SCALE | NON JEDEC | 98ASA01467D | C | |

Figure 4. Reflow soldering footprint part3 for WLCSP48 (SOT2028-1)

SOT2028-1

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Package information **2 June 2021**

5 / 8

WLCSP48, wafer level chip-scale package; 48 bumps; 0.4 mm pitch, 3.15 mm x 2.89 mm x 0.38 mm body

WLCSP-48 I/O
3.15 X 2.89 X 0.38 PKG, 0.4 PITCH

SOT2028-1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.

5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

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Figure 5. Package outline note WLCSP48 (SOT2028-1)

2 June 2021

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Contents