

SOT2084-1

HWFLGA18, thermal enhanced very-very thin fine-pitched land grid array package, 18 terminals, 0.4 mm pitch, 2.4 mm x 2 mm x 0.64 mm body

3 March 2021

Package information

1 Package summary

Terminal position code B (bottom)

Package type descriptive code HWFLGA18

Package style descriptive code LGA (land grid array package)

Mounting method type S (surface mount)

Issue date 10-09-2020

Manufacturer package code 98ASA01669D

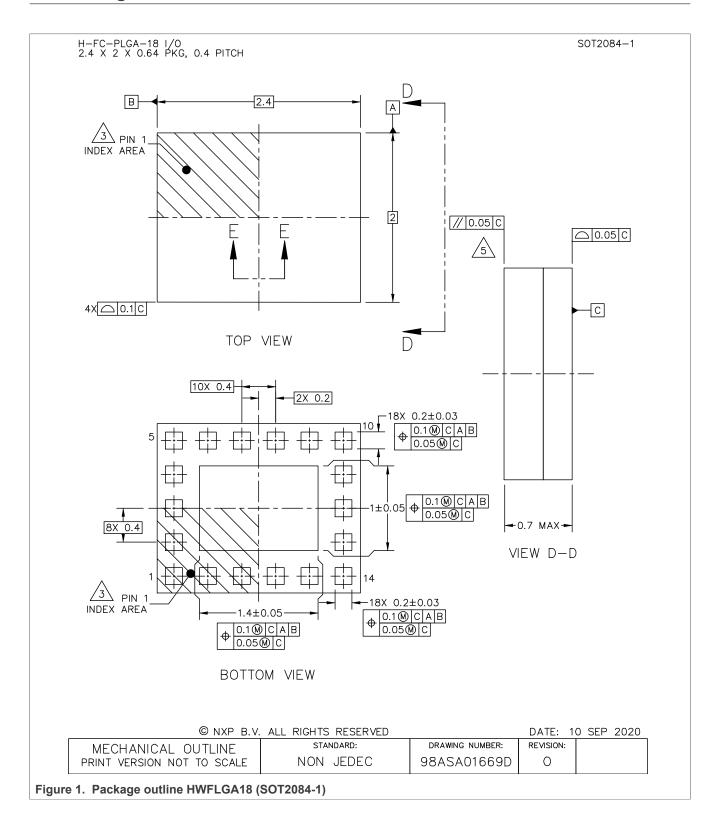
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	2.3	2.4	2.5	mm
package width	1.9	2	2.1	mm
seated height	-	0.64	0.7	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	18	-	

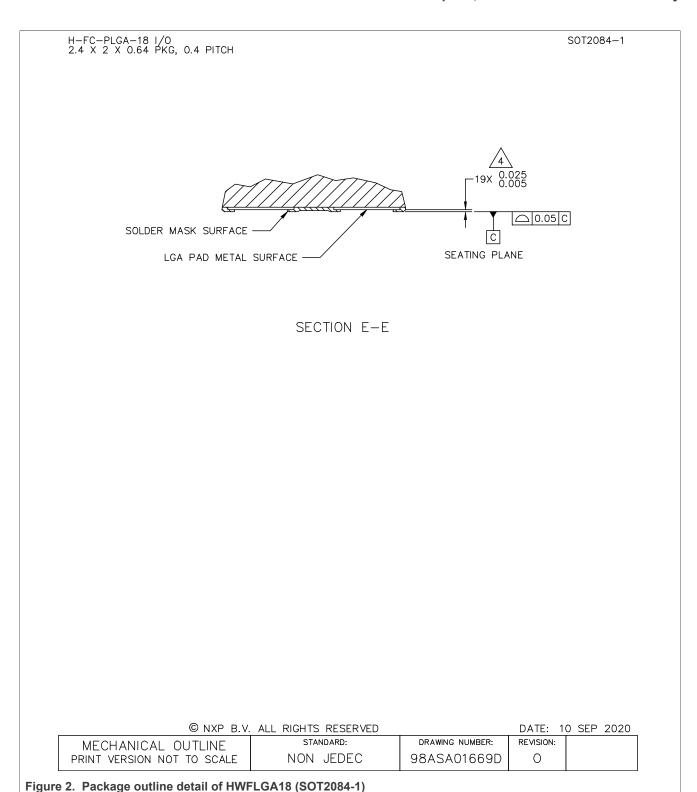


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2 Package outline



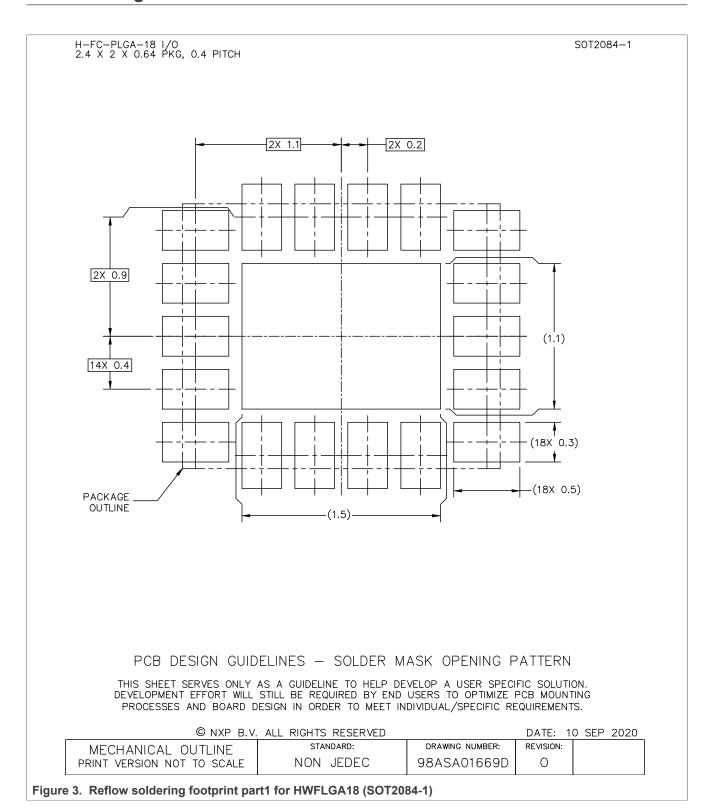
HWFLGA18, thermal enhanced very-very thin fine-pitched land grid array package, 18 terminals, 0.4 mm pitch, 2.4 mm x 2 mm x 0.64 mm body



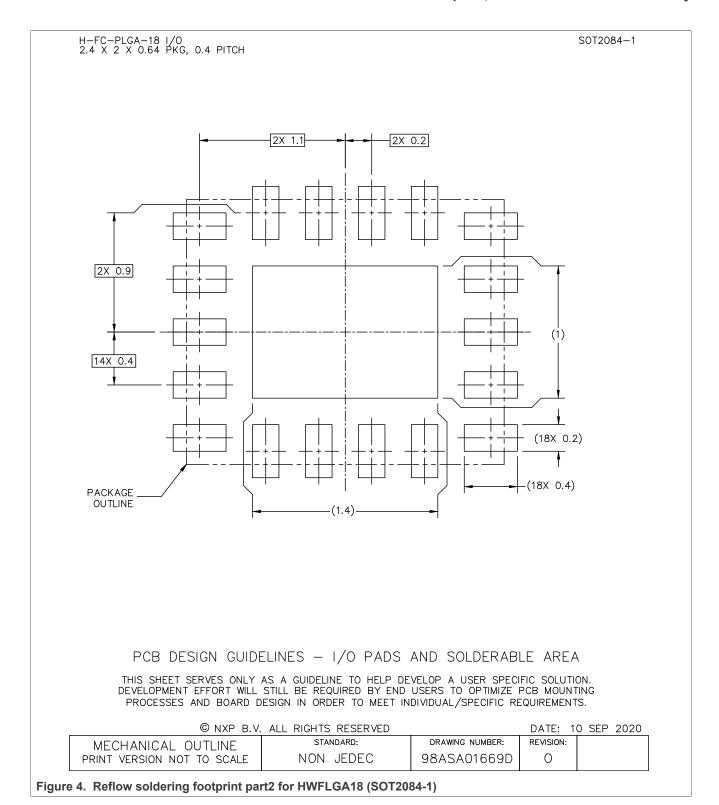
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3 Soldering



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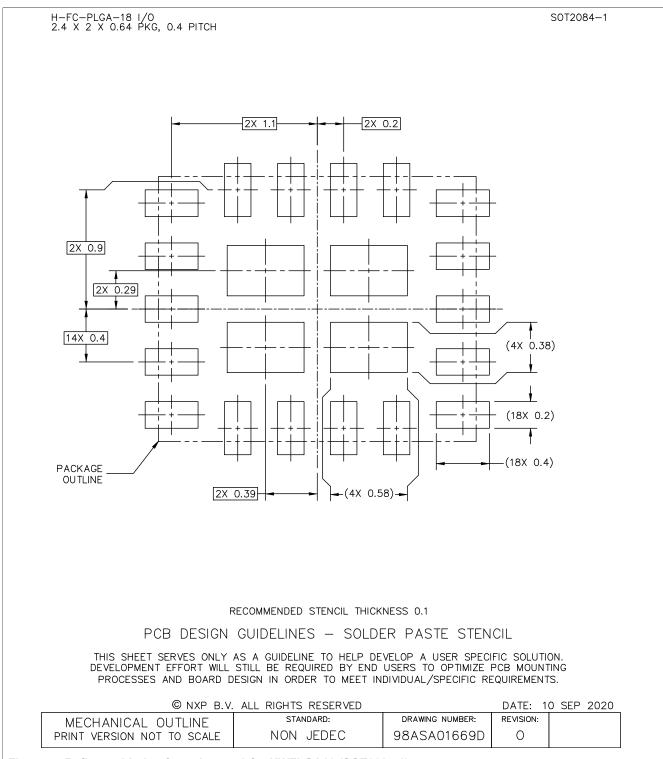


Figure 5. Reflow soldering footprint part3 for HWFLGA18 (SOT2084-1)

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H-FC-PLGA-18 I/O 2.4 X 2 X 0.64 PKG, 0.4 PITCH S0T2084-1 NOTES: 1. ALL DIMENSIONS ARE IN MILLIMETERS. 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994. $\sqrt{3}$. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY. DIMENSION APPLIES TO ALL LEADS. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE

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MECHANICAL OUTLINE	STANDARD:	DRAWING NUMBER:	REVISION:	
PRINT VERSION NOT TO SCALE	NON JEDEC	98ASA01669D	0	

Figure 6. Package outline note HWFLGA18 (SOT2084-1)

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4 Legal information

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