

SOT2084-2

HWFLGA18, thermal enhanced very-very thin fine-pitched land grid array package, 18 terminals, 0.4 mm pitch, 2.4 mm x 2 mm x 0.64 mm body

13 September 2022

Package information

1 Package summary

Terminal position code B (bottom)

Package type descriptive code HWFLGA18

Package style descriptive code LGA (land grid array package)

Mounting method type S (surface mount)

Issue date 17-08-2022

Manufacturer package code 98ASA01732D

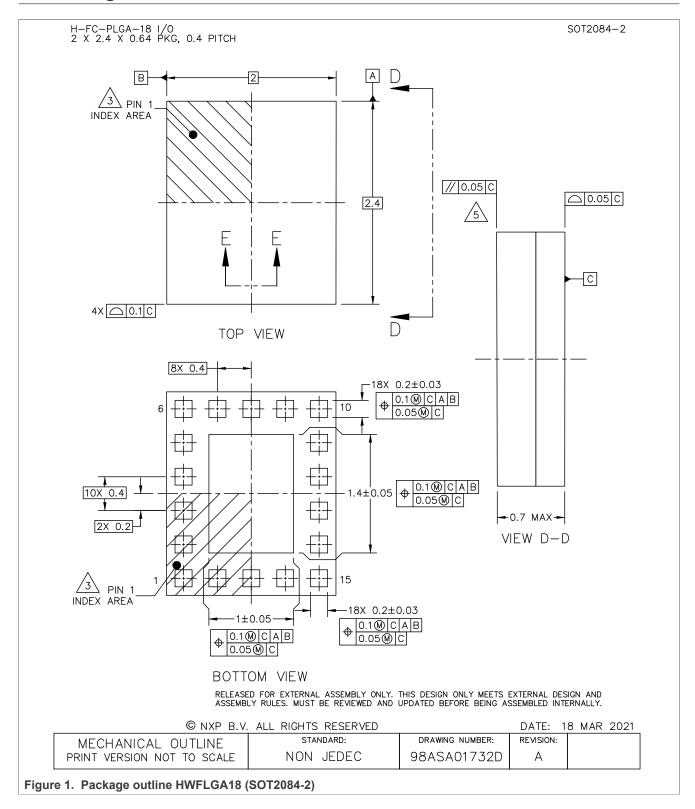
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	2.3	2.4	2.5	mm
package width	1.9	2	2.1	mm
seated height	-	0.64	0.7	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	18	-	



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2 Package outline



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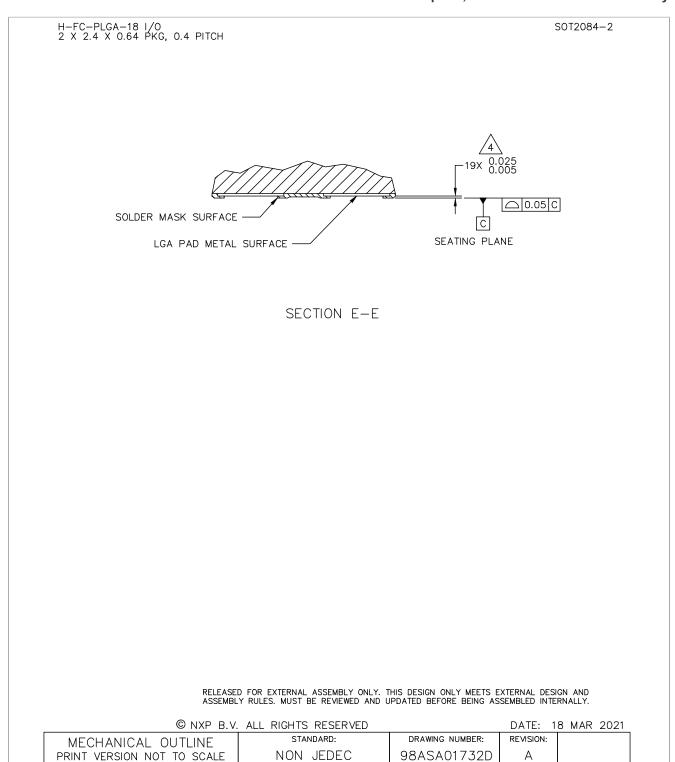
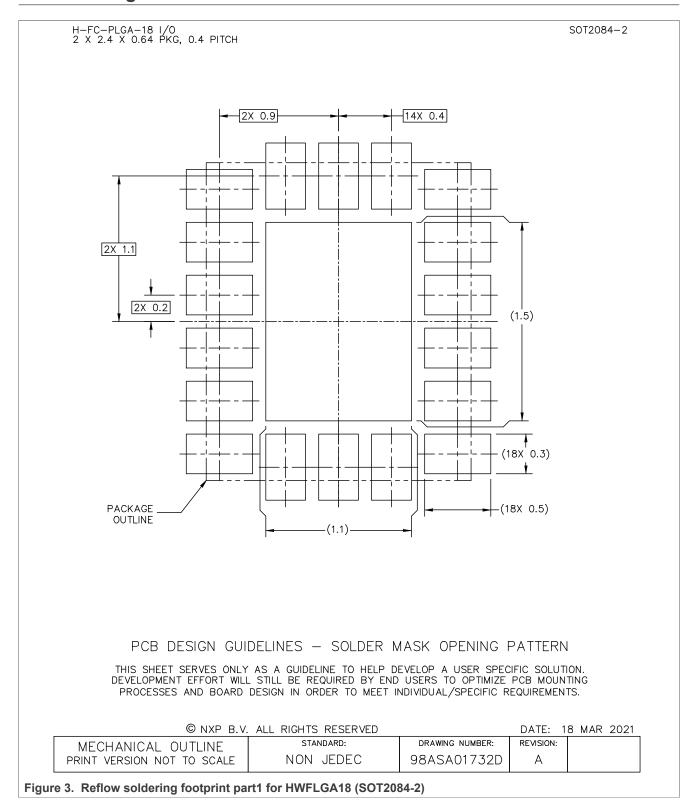


Figure 2. Package outline detail of HWFLGA18 (SOT2084-2)

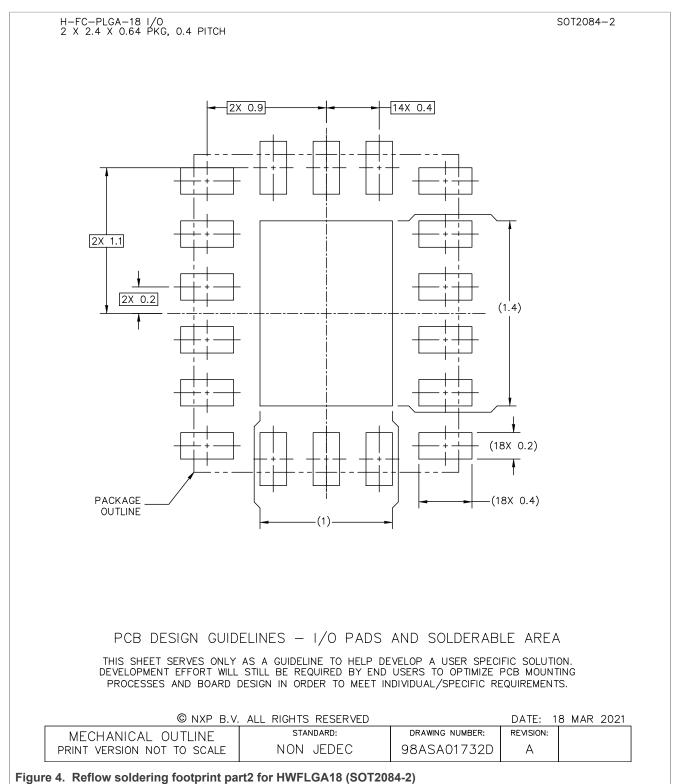
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3 Soldering

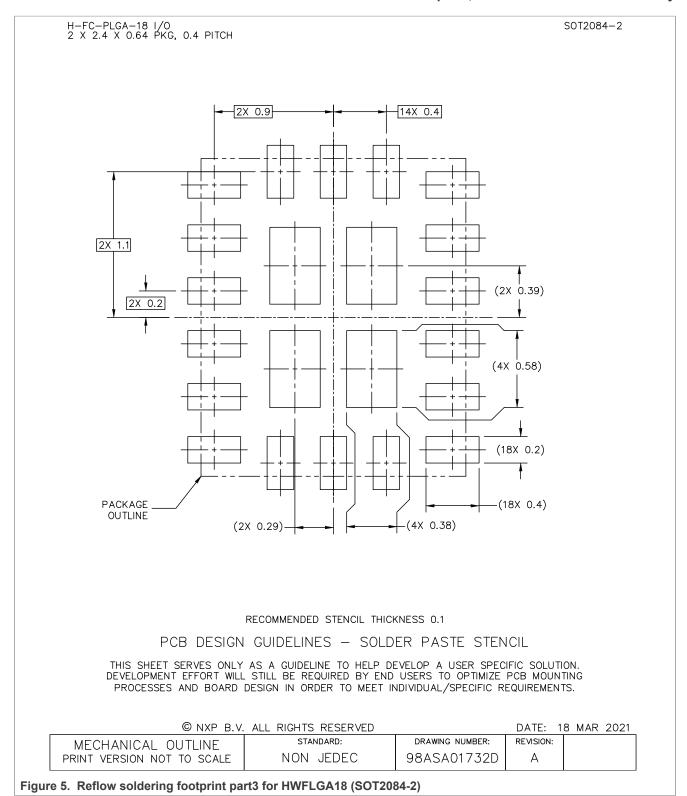


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H-FC-PLGA-18 I/O 2 X 2.4 X 0.64 PKG, 0.4 PITCH SOT2084-2 NOTES: 1. ALL DIMENSIONS ARE IN MILLIMETERS. 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY. DIMENSION APPLIES TO ALL LEADS. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE © NXP B.V. ALL RIGHTS RESERVED DATE: 18 MAR 2021

MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

STANDARD:

NON JEDEC

DRAWING NUMBER:

98ASA01732D

REVISION:

Α

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4 Legal information

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