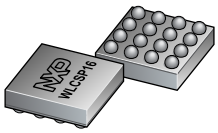


SOT2127-1

WLCSP16, wafer level chip scale package, 16 terminals, 0.35 mm pitch, 1.41 mm x 1.41 mm x 0.49 mm body (backside coating included)

2 March 2021 **Package information**

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP16
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	12-01-2021
Manufacturer package code	98ASA01735D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	1.38	1.41	1.44	mm
package width	1.38	1.41	1.44	mm
package height	-	0.49	0.525	mm
nominal pitch	-	0.35	-	mm
actual quantity of termination	-	16	-	

WLCSP16, wafer level chip scale package, 16 terminals, 0.35 mm pitch, 1.41 mm x 1.41 mm x 0.49 mm body (backside coating included)

2 Package outline

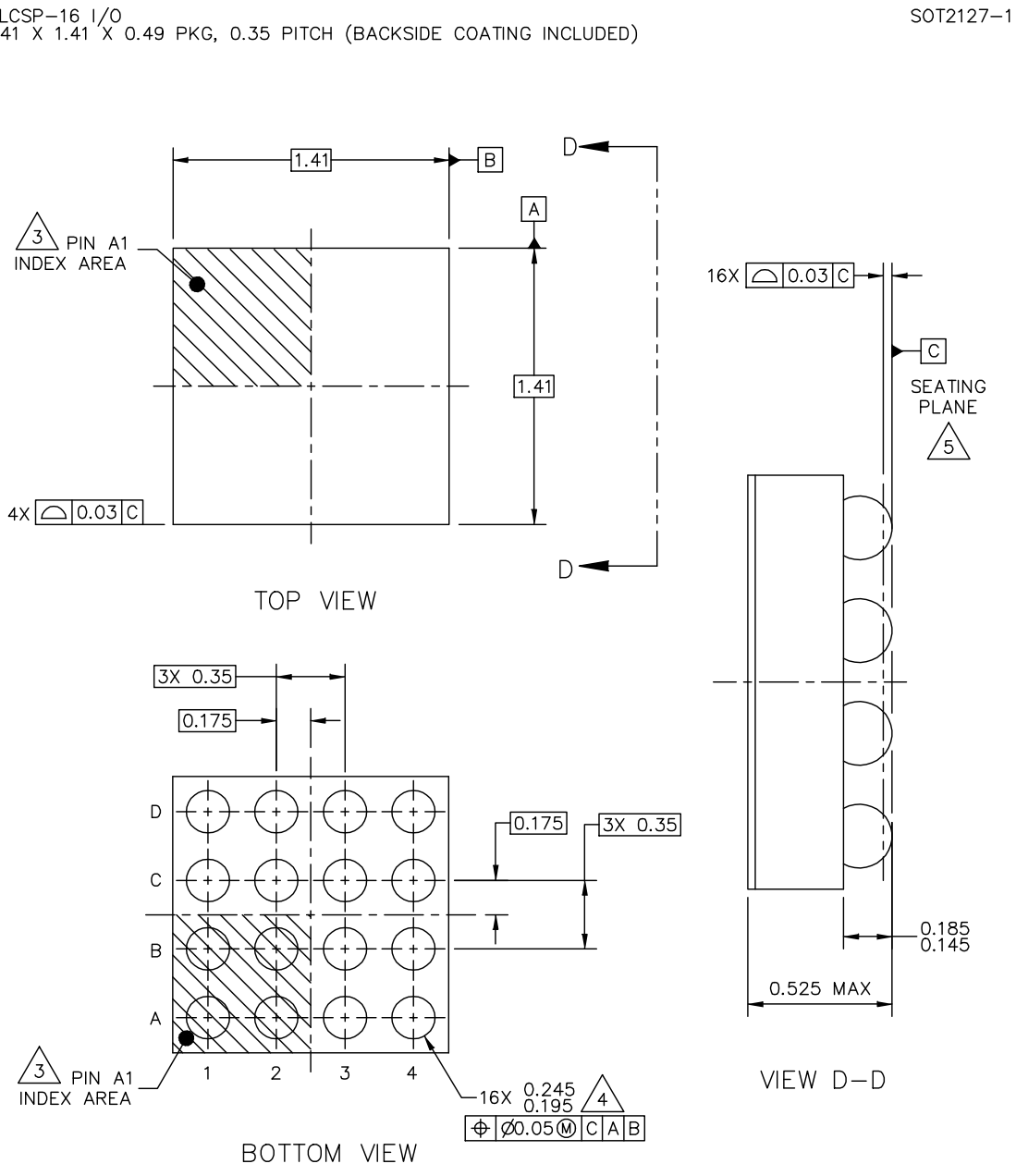


Figure 1. Package outline WLCSP16 (SOT2127-1)

3 Soldering

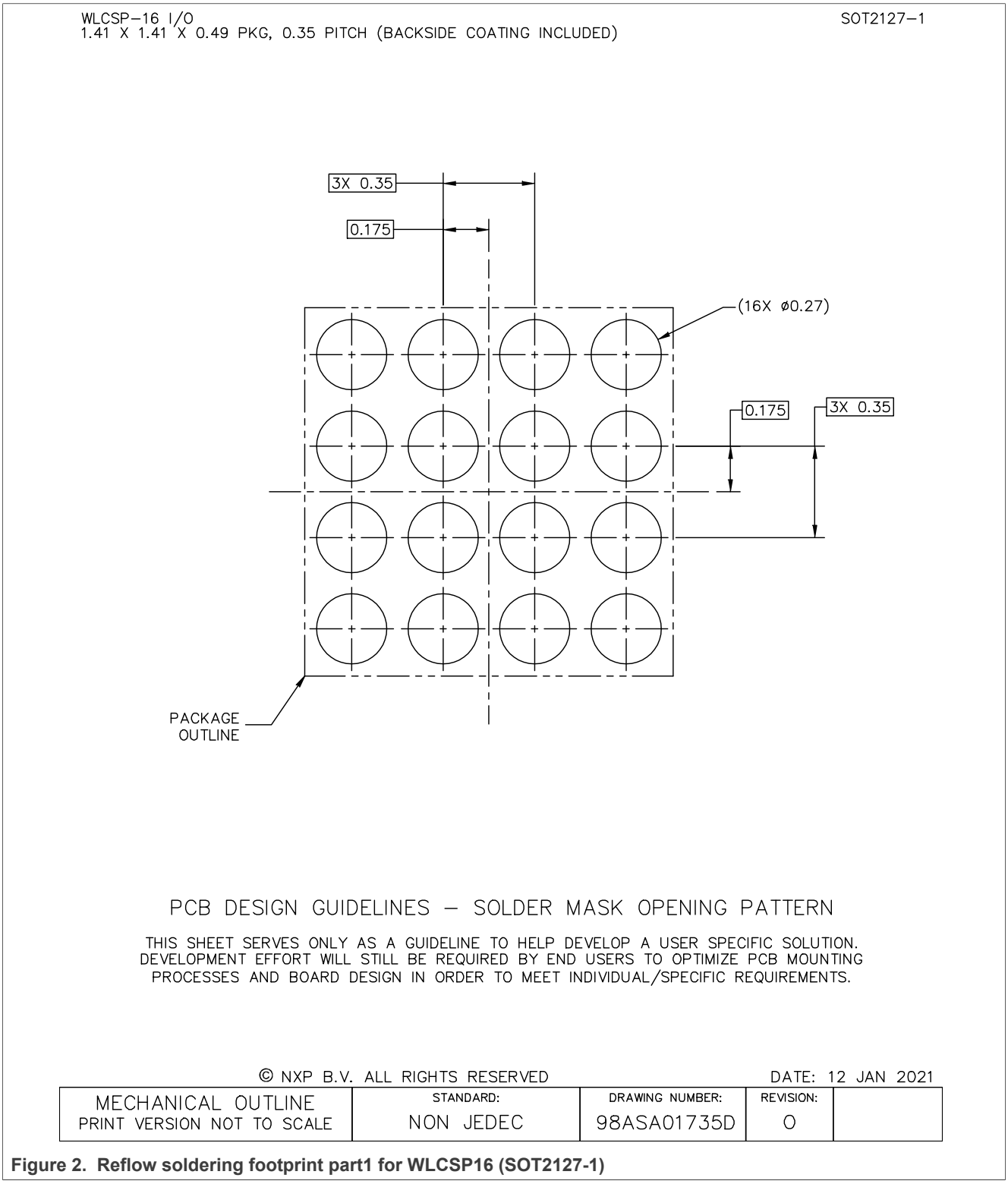
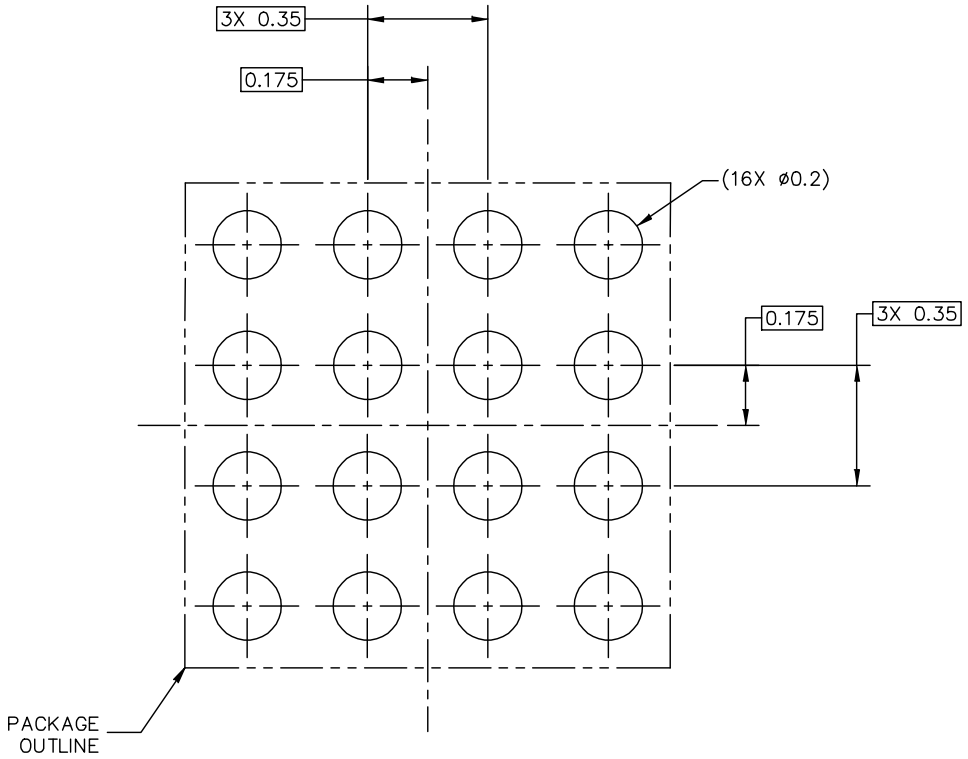


Figure 2. Reflow soldering footprint part1 for WLCSP16 (SOT2127-1)

WLCSP−16 I/O
1.41 X 1.41 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2127−1



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DATE: 12 JAN 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01735D	REVISION: O	

Figure 3. Reflow soldering footprint part2 for WLCSP16 (SOT2127-1)

WLCSP16, wafer level chip scale package, 16 terminals, 0.35 mm pitch, 1.41 mm x 1.41 mm x 0.49 mm body (backside coating included)

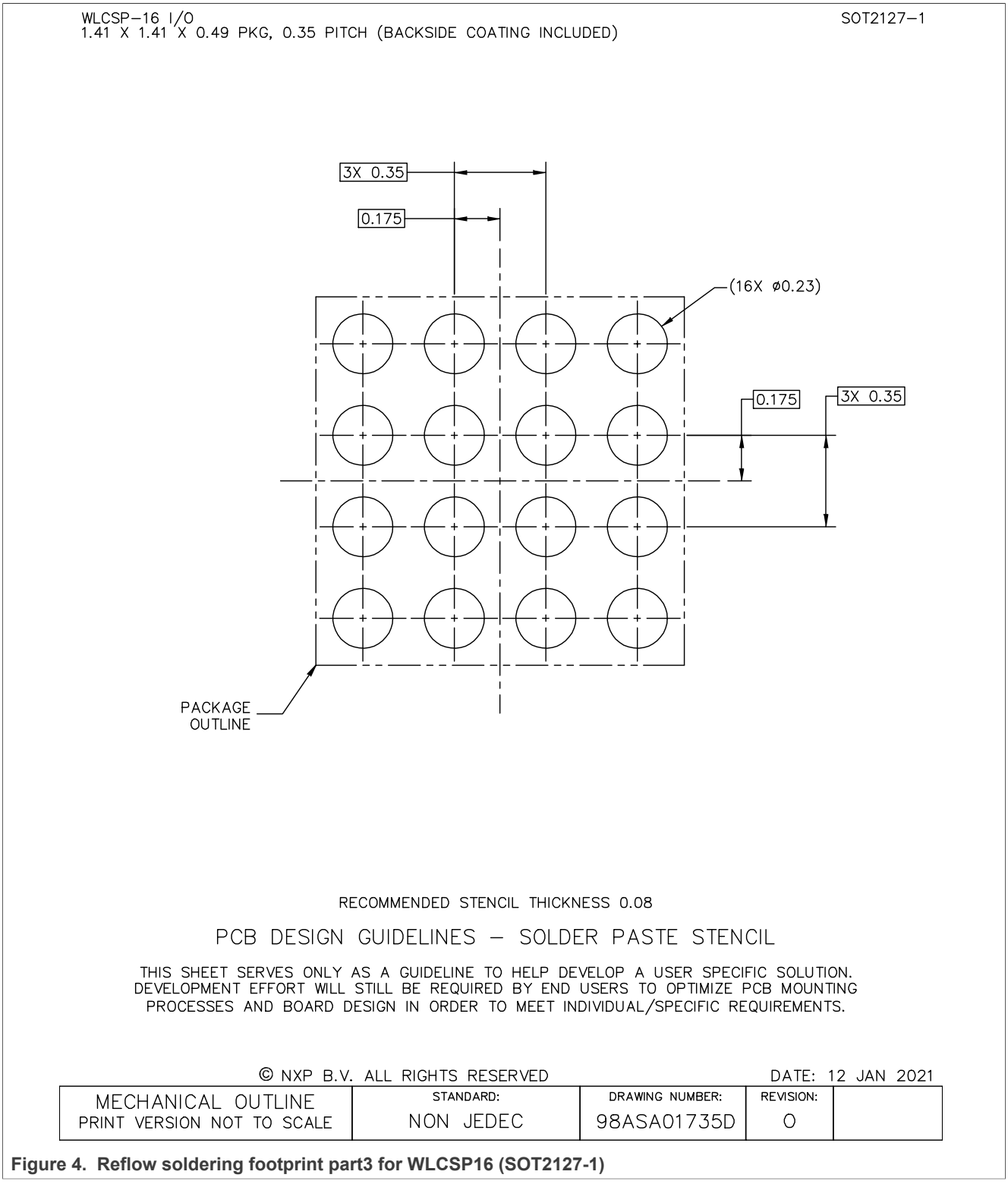

Figure 4. Reflow soldering footprint part3 for WLCSP16 (SOT2127-1)

WLCSP16, wafer level chip scale package, 16 terminals, 0.35 mm pitch, 1.41 mm x 1.41 mm x 0.49 mm body (backside coating included)

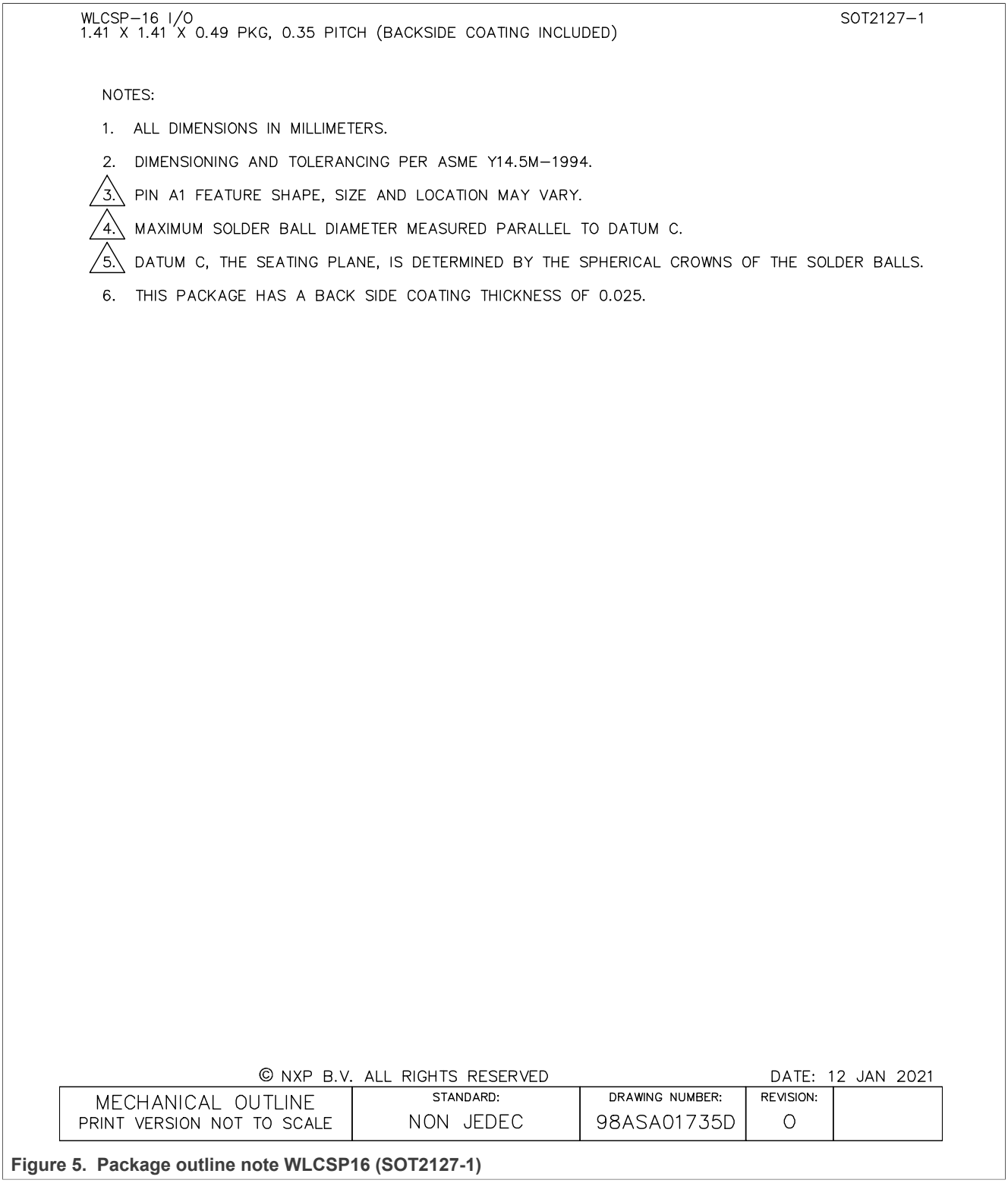

Figure 5. Package outline note WLCSP16 (SOT2127-1)

4 Legal information

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SOT2127-1

WLCSP16, wafer level chip scale package, 16 terminals, 0.35 mm pitch, 1.41 mm x 1.41 mm x 0.49 mm body (backside coating included)

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Date of release: 2 March 2021