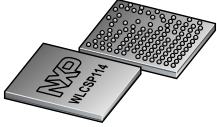


SOT2235-1

WLCSP114, wafer level chip scale package, 114 terminals, 0.33 mm pitch,
4.495 mm x 4.0 mm x 0.455 mm body (backside coating included)

3 December 2024

Package information



1 Package summary

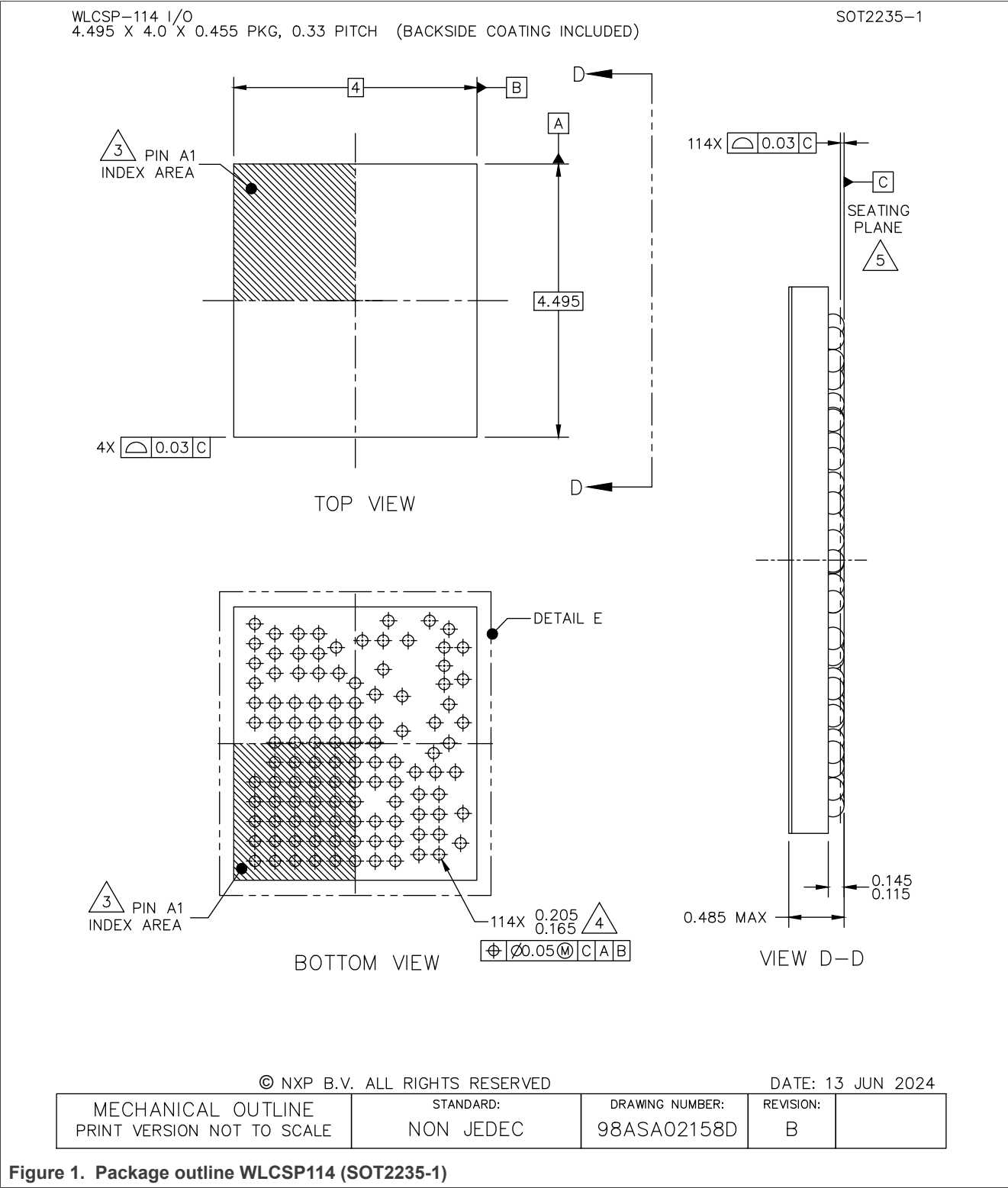
Terminal position code	U (upper)
Package type descriptive code	WLCSP114
Package style descriptive code	WLCSP (wafer level chip-size package)
Package body material type	S (silicon)
Mounting method type	S (surface mount)
Issue date	02-12-2024
Manufacturer package code	98ASA02158D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	4.465	4.495	4.525	mm
package width	3.97	4	4.03	mm
seated height	0.3	0.325	0.35	mm
package height	0.425	0.455	0.485	mm
nominal pitch	-	0.33	-	mm
actual quantity of termination	-	114	-	

WLCSP114, wafer level chip scale package, 114 terminals, 0.33 mm pitch, 4.495 mm x 4.0 mm x 0.455 mm body (backside coating included)

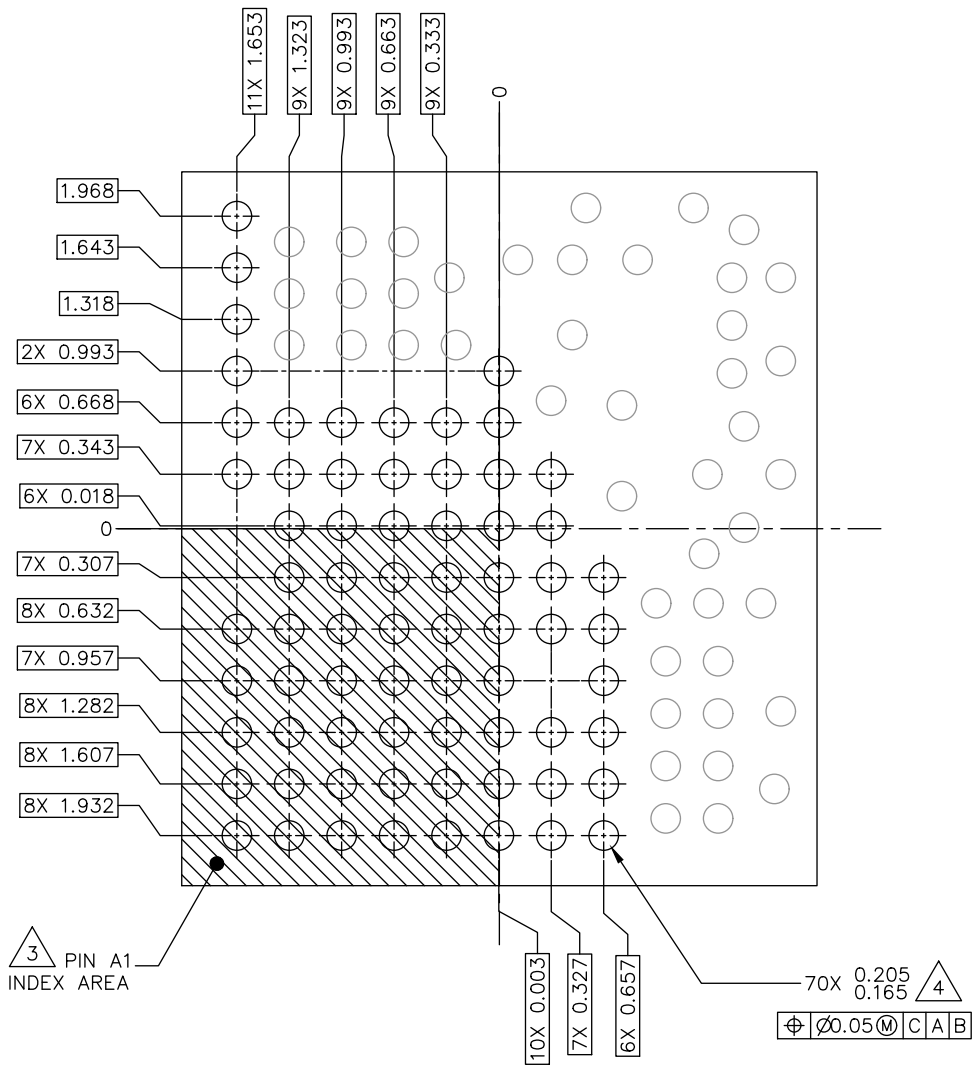
2 Package outline



WLCSP114, wafer level chip scale package, 114 terminals, 0.33 mm pitch, 4.495 mm x 4.0 mm x 0.455 mm body (backside coating included)

WLCSP-114 I/O
4.495 X 4.0 X 0.455 PKG, 0.33 PITCH (BACKSIDE COATING INCLUDED)

SOT2235-1



DETAIL E (I)
(ARRAY BUMPS (70X))

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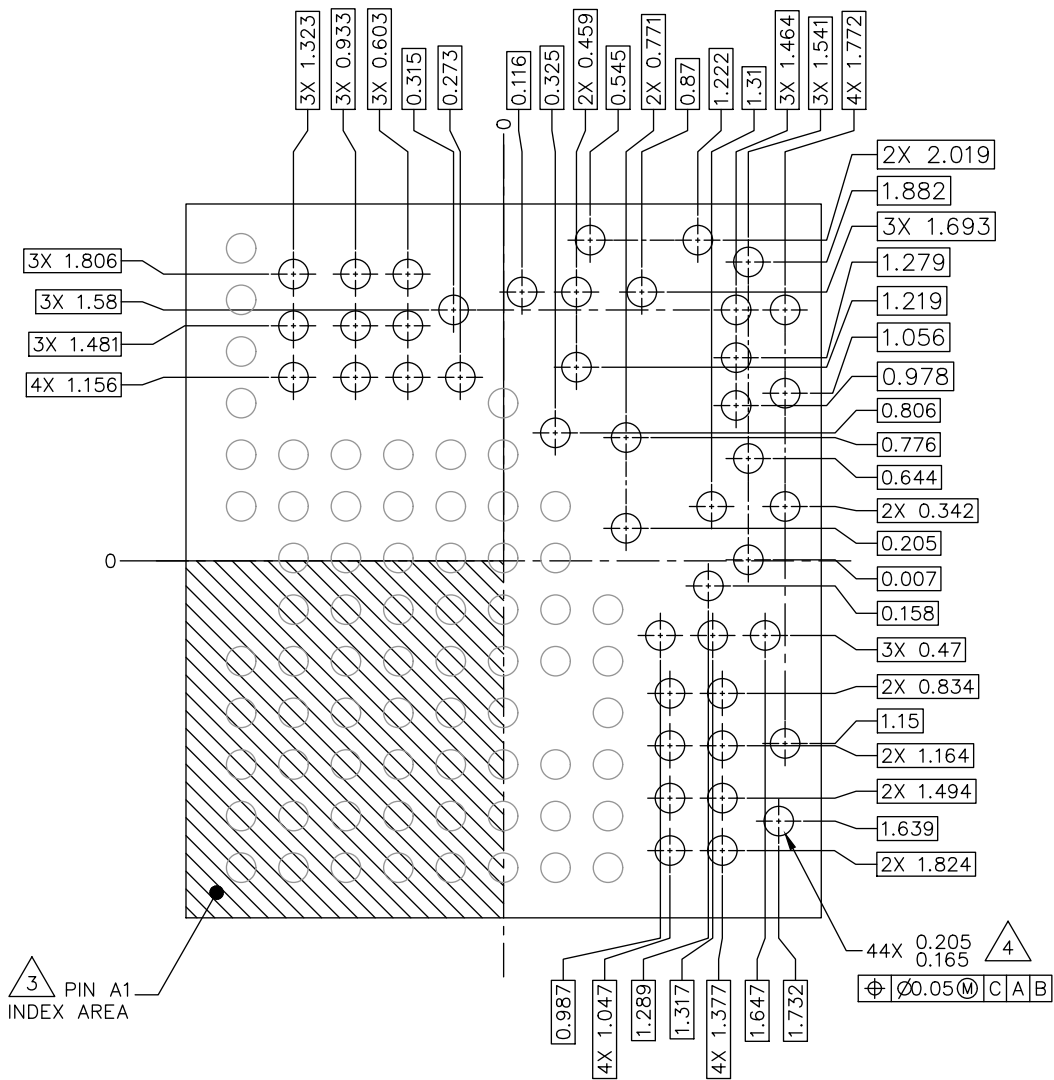
DATE: 13 JUN 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02158D	REVISION: B
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Figure 2. Package outline detail E (I) of WLCSP114 (SOT2235-1)

WLCSP114, wafer level chip scale package, 114 terminals, 0.33 mm pitch, 4.495 mm x 4.0 mm x 0.455 mm body (backside coating included)

WLCSP-114 I/O
4.495 X 4.0 X 0.455 PKG, 0.33 PITCH (BACKSIDE COATING INCLUDED) SOT2235-1



DETAIL E (II)
(NON-ARRAY BUMPS (44X))

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02158D	REVISION: B

Figure 3. Package outline detail E (II) of WLCSP114 (SOT2235-1)

WLCSP114, wafer level chip scale package, 114 terminals, 0.33 mm pitch, 4.495 mm x 4.0 mm x 0.455 mm body (backside coating included)

3 Soldering

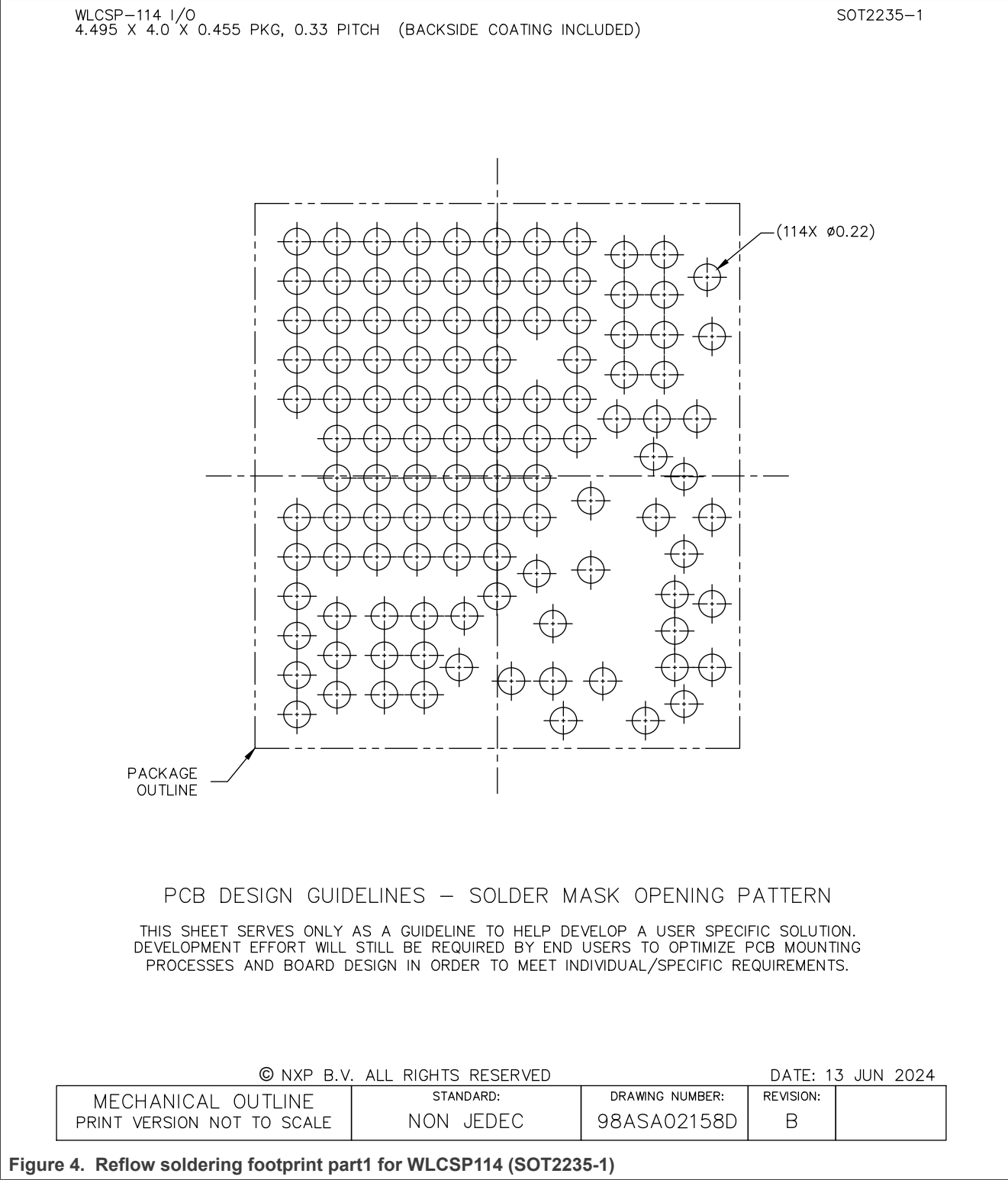
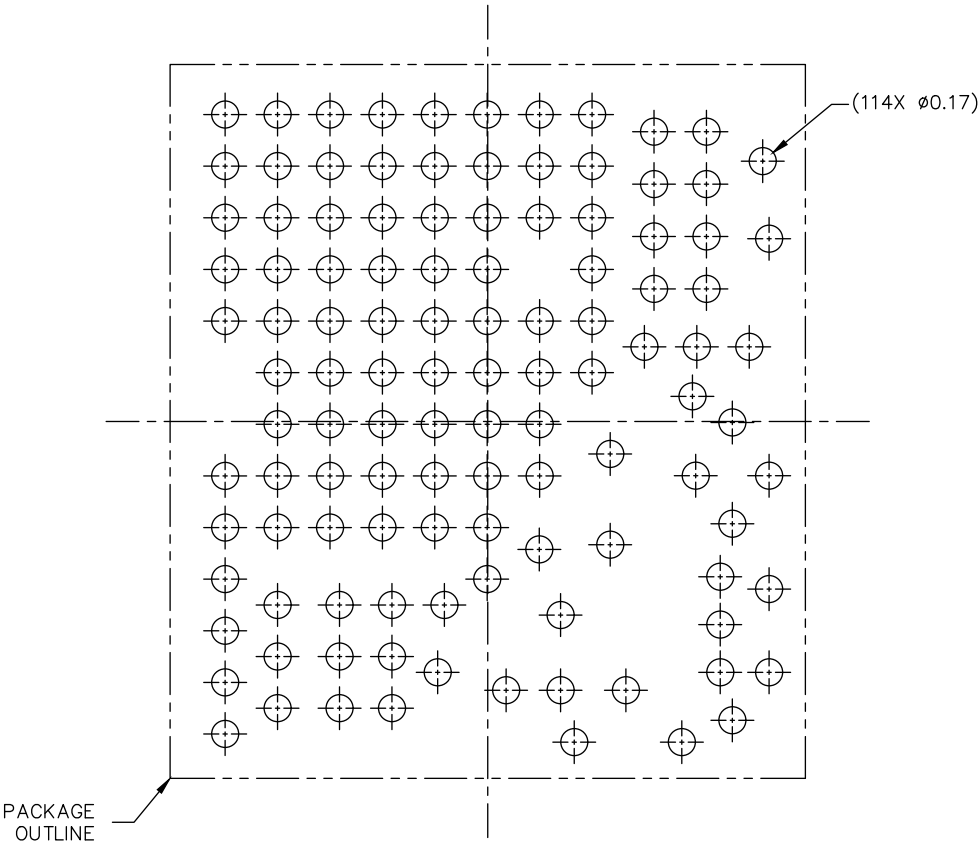


Figure 4. Reflow soldering footprint part1 for WLCSP114 (SOT2235-1)

WLCSP114, wafer level chip scale package, 114 terminals, 0.33 mm pitch, 4.495 mm x 4.0 mm x 0.455 mm body (backside coating included)

WLCSP-114 I/O
4.495 X 4.0 X 0.455 PKG, 0.33 PITCH (BACKSIDE COATING INCLUDED)

SOT2235-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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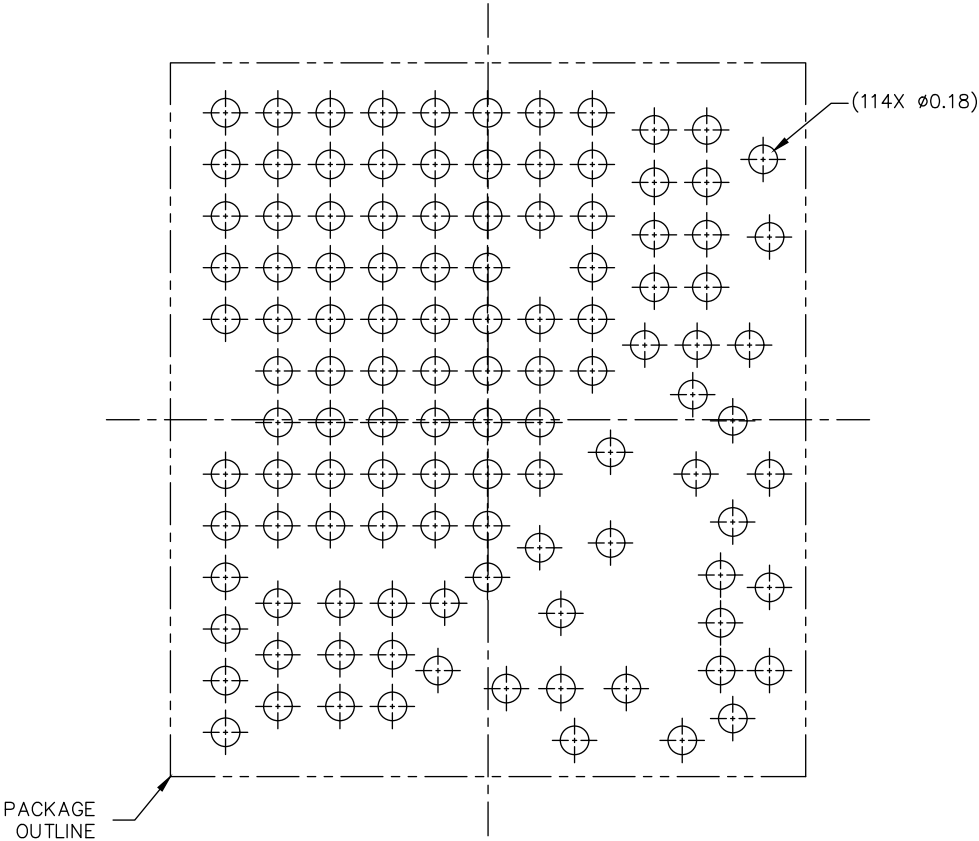
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02158D	REVISION: B	
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Figure 5. Reflow soldering footprint part2 for WLCSP114 (SOT2235-1)

WLCSP114, wafer level chip scale package, 114 terminals, 0.33 mm pitch, 4.495 mm x 4.0 mm x 0.455 mm body (backside coating included)

WLCSP-114 I/O
4.495 X 4.0 X 0.455 PKG, 0.33 PITCH (BACKSIDE COATING INCLUDED)

SOT2235-1



RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION.
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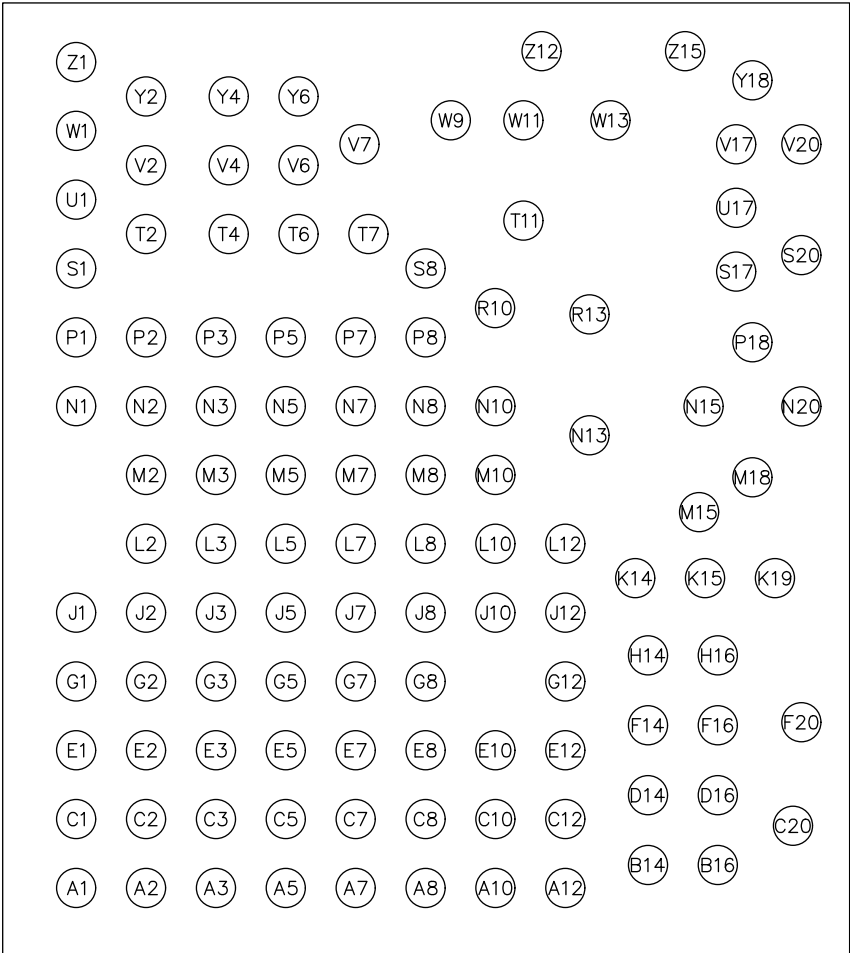
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02158D	REVISION: B	
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Figure 6. Reflow soldering footprint part3 for WLCSP114 (SOT2235-1)

WLCSP114, wafer level chip scale package, 114 terminals, 0.33 mm pitch, 4.495 mm x 4.0 mm x 0.455 mm body (backside coating included)

WLCSP-114 I/O
4.495 X 4.0 X 0.455 PKG, 0.33 PITCH (BACKSIDE COATING INCLUDED)

SOT2235-1



PIN NUMBERS
(VIEWED FROM BOTTOM, SAME AS DETAIL E)

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DATE: 13 JUN 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02158D	REVISION: B	
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Figure 7. Reflow soldering footprint part4 for WLCSP114 (SOT2235-1)

WLCSP114, wafer level chip scale package, 114 terminals, 0.33 mm pitch, 4.495 mm x 4.0 mm x 0.455 mm body (backside coating included)

WLCSP-114 I/O
4.495 X 4.0 X 0.455 PKG, 0.33 PITCH (BACKSIDE COATING INCLUDED)

SOT2235-1

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
- 5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02158D	REVISION: B	
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Figure 8. Package outline note WLCSP114 (SOT2235-1)

WLCSP114, wafer level chip scale package, 114 terminals, 0.33 mm pitch, 4.495 mm x 4.0 mm x 0.455 mm body (backside coating included)

4 Legal information

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WLCSP114, wafer level chip scale package, 114 terminals, 0.33 mm pitch, 4.495 mm x 4.0 mm x 0.455 mm body (backside coating included)

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