MC3S12RFAMPB
Rev. 1, 11/2005

MC3S12R-Family

16-Bit Microcontroller

Designed for high volume automotive multiplexing applications with stable code, members of the MC3S12R-Family of 16 bit ROM-based microcontrollers are fully pin compatible with the MC9S12D-Family of Flash-based microcontrollers. All MC3S12R-Family members are composed of standard on-chip peripherals including a 16-bit central processing unit (CPU12), up to 128K bytes of ROM, 8K bytes of RAM, two asynchronous serial communications interfaces (SCI), two serial peripheral interfaces (SPI), IIC-bus, an enhanced capture timer (ECT), two 8-channel 10-bit analog-to-digital converters (ADC), an eight-channel pulse-width modulator (PWM), and up to two CAN 2.0 A, B software compatible modules (MSCAN12). There is no integrated EEPROM on the MC3S12R-Family. System resource mapping, clock generation, interrupt control and bus interfacing are managed by the system integration module (SIM). The MC3S12R-Family has full 16-bit data paths throughout, however, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available in each module, up to 22 I/O ports are available with interrupt capability allowing Wake-Up from STOP or WAIT mode.

Features

NOTES

The R-Family Flash equivalent is the MC9S12D-Family

Not all features listed here are available in all configurations.

Additional information about D and B family inter-operability is given in:

- EB386 “HCS12 D-Family Compatibility Considerations” and
- EB388 “Using the HCS12 D-Family as a development platform for the HCS12 B family”

freescale™ semiconductor

- 16-bit CPU12
  - Upward compatible with M68HC11 instruction set
  - Interrupt stacking and programmer's model identical to M68HC11
  - HCS12 Instruction queue
  - Enhanced indexed addressing
- Multiplexed bus
  - Single chip or expanded
  - 16 address/16 data wide or 16 address/8 data narrow modes
  - External address space 1MByte for Data and Program space (112 pin package only)
- Wake-up interrupt inputs depending on the package option
  - 8-bit port H
  - 2-bit port J1:0
  - 2-bit port J7:6 shared with IIC, CAN4 and CAN0 module
  - 8-bit port P shared with PWM or SPI1
- Memory options
  - 64K, 128K Byte ROM
  - 8K Byte RAM
- Analog-to-Digital Converters
  - One or two 8-channel modules with 10-bit resolution depending on the package option
  - External conversion trigger capability
- Up to two 1M bit per second, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Receive, Transmit, Error and Wake-up
  - Low-pass filter wake-up function in STOP mode
  - Loop-back for self test operation
- Enhanced Capture Timer (ECT)
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels; 4 of the 8 input captures with buffer
  - Input capture filters and buffers, three successive captures on four channels, or two captures on four channels with a capture/compare selectable on the remaining four
  - Four 8-bit or two 16-bit pulse accumulators
  - 16-bit modulus down-counter with 4-bit prescaler
  - Four user-selectable delay counters for signal filtering

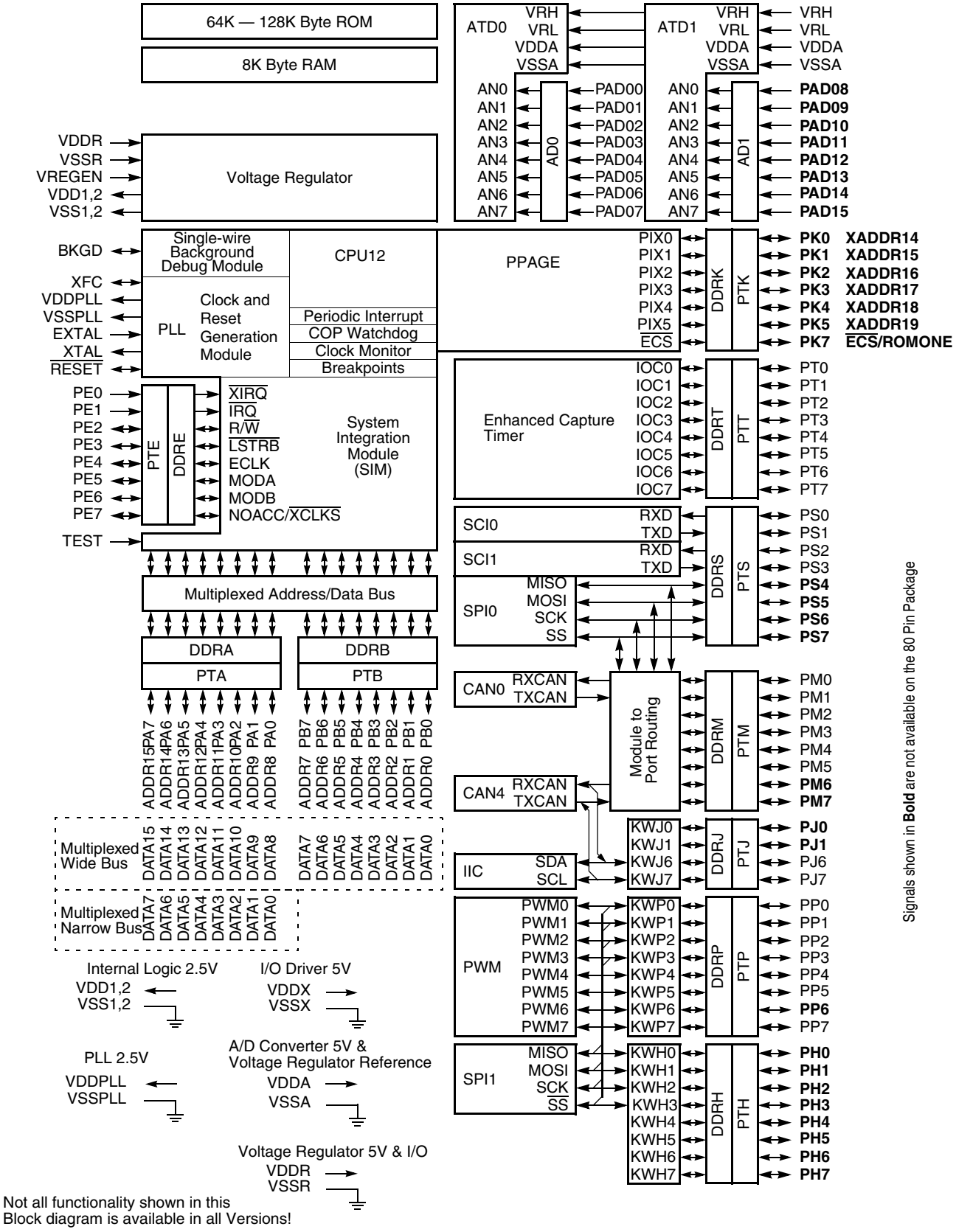
- 8 PWM channels with programmable period and duty cycle (7 channels on 80 Pin Packages)
  - 8-bit, 8-channel or 16-bit, 4-channel
  - Separate control for each pulse width and duty cycle
  - Center- or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
- Serial interfaces
  - Two asynchronous serial communications interfaces (SCI)
  - Up to two synchronous serial peripheral interfaces (SPI)
  - IIC
- SIM (System Integration Module)
  - CRG (windowed COP watchdog, real time interrupt, clock monitor, clock generation and reset)
  - MEBI (multiplexed external bus interface)
  - INT (interrupt control)
- Clock generation
  - Phase-locked loop clock frequency multiplier
  - Limp home mode in absence of external clock
  - Clock Monitor
  - Low power 0.5 to 16 MHz crystal oscillator reference clock
- Operating frequency for ambient temperatures T_A -40°C <= T_A <= 125°C
  - 50MHz equivalent to 25MHz Bus Speed for single chip
  - 40MHz equivalent to 20MHz Bus Speed in expanded bus modes.
- Internal 5V to 2.5V Regulator
- 112-Pin LQFP or 80-Pin QFP package
  - I/O lines with 5V input and drive capability
  - 5V A/D converter inputs and 5V I/O
  - 2.5V logic supply
- Development support
  - Single-wire background debug™ mode (BDM)
  - On-chip hardware breakpoints

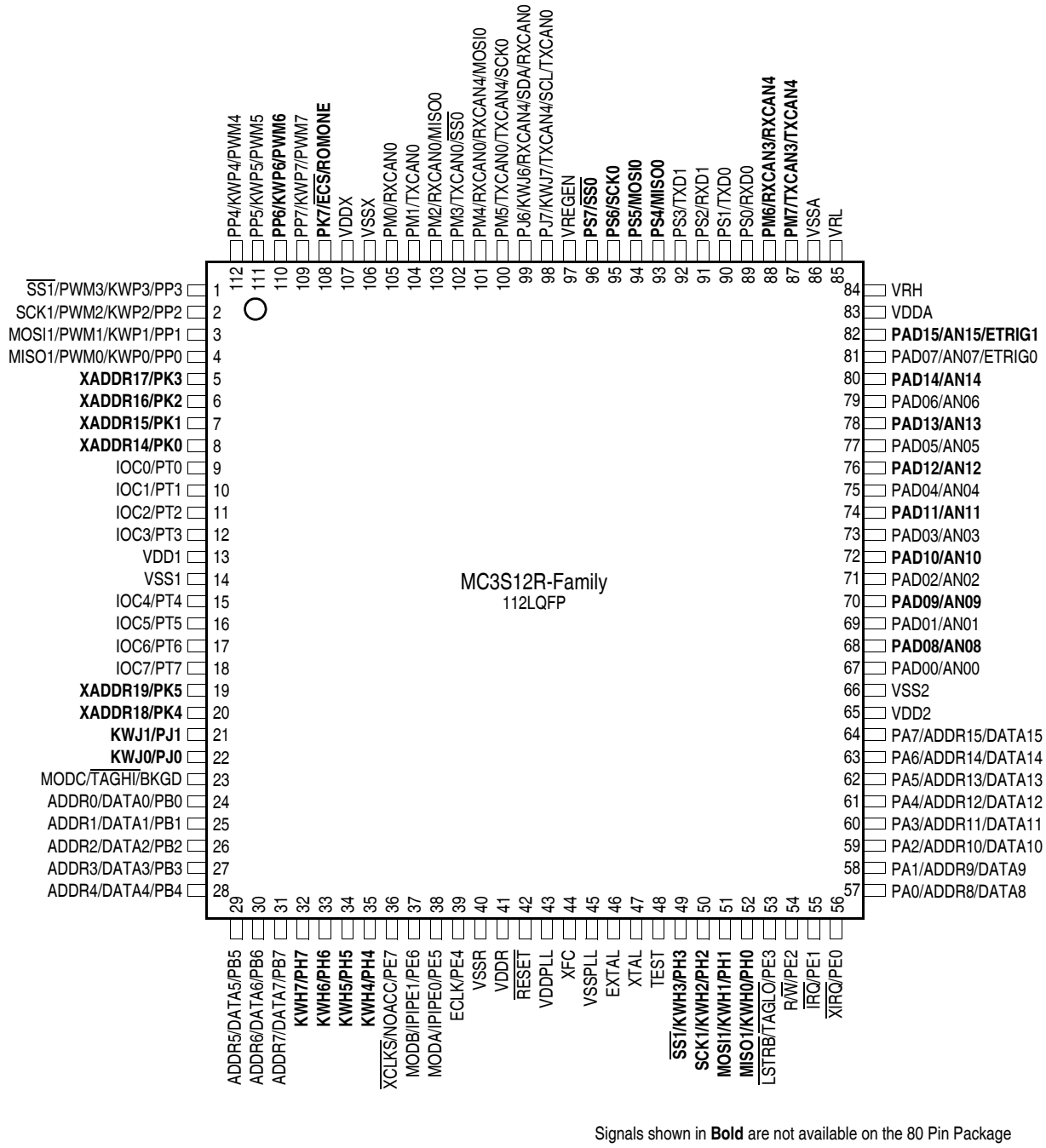
Table 1. List of MC3S12R-Family Members

Device	ROM	RAM	EE	Package	CAN	SCI	SPI	IIC	A/D	PWM	I/O	Flash Equiv.
MC3S12RG128	128K	8K	0	112LQFP	2	2	2	1	2/16	8	91	MC9S12DG128
				80QFP	2	2	2	1	1/8	7	59	
MC3S12RB128	128K	8K	0	112LQFP	1	2	1	1	2/16	8	91	MC9S12DG128
				80QFP	1	2	1	1	1/8	7	59	
MC3S12R64	64K	8K	0	112LQFP	1	2	1	1	2/16	8	91	MC9S12D64[1]
				80QFP	1	2	1	1	1/8	7	59	

NOTES:
1 To ensure compatibility with the MC9S12D64 FLASH devices, the internal RAM should not be remapped to a location outside of the first 16K page ($0000–$3FFF) in the memory map (4K RAM on the D64 vs. 8K RAM on the R64).

- Pin out explanations:
  - A/D is the number of modules/total number of A/D channels.
  - I/O is the sum of ports capable to act as digital input or output.
  - 112 Pin Packages:
    - Port A = 8, B = 8, E = 6 + 2 input only, H = 8, J = 4, K = 7, M = 8, P = 8, S = 8, T = 8, PAD = 16 input only.
    - 22 inputs provide Interrupt capability (H =8, P= 8, J = 4, IRQ, XIRQ)
  - 80 Pin Packages:
    - Port A = 8, B = 8, E = 6 + 2 input only, J = 2, M = 6, P = 7, S = 4, T = 8, PAD = 8 input only.
    - 11 inputs provide Interrupt capability (P= 7, J = 2, IRQ, XIRQ)
  - CAN0 can be routed under software control from PM1:0 to pins PM3:2 or PM5:4 or PJ7:6.
  - CAN4 pins are shared between IIC pins.
  - CAN4 can be routed under software control from PJ7:6 to pins PM5:4 or PM7:6.
  - Versions with 2 CAN modules will have CAN0 and CAN4.
  - Versions with one CAN module will have CAN0.
  - Versions with 2 SPI modules will have SPI0 and SPI1.
  - Versions with 1 SPI will have SPI0.
  - SPI0 can be routed to either Ports PS7:4 or PM5:2.
  - SPI1 pins are shared with PWM3:0; In 112 pin versions SPI1 can be routed under software control to PH3:0.


64K — 128K Byte ROM
8K Byte RAM
Voltage Regulator
VDDR
VSSR
VREGEN
VDD1,2
VSS1,2
Single-wire Background Debug Module
CPU12
BKGD
XFC
VDDPLL
VSSPLL
EXTAL
XTAL
RESET
PLL
Clock and Reset Generation Module
Periodic Interrupt
COP Watchdog
Clock Monitor
Breakpoints
PE0
PE1
PE2
PE3
PE4
PE5
PE6
PE7
PTE
DDRE
XIRQ
IRQ
R/W
LSTRB
ECLK
MODA
MODB
NOACC/XCLKS
System Integration Module (SIM)
TEST
Multiplexed Address/Data Bus
DDRA
PTA
DDRB
PTB
ADDR15PA7
ADDR14PA6
ADDR13PA5
ADDR12PA4
ADDR11PA3
ADDR10PA2
ADDR9 PA1
ADDR8 PA0
ADDR7 PB7
ADDR6 PB6
ADDR5 PB5
ADDR4 PB4
ADDR3 PB3
ADDR2 PB2
ADDR1 PB1
ADDR0 PB0
Multiplexed Wide Bus
DATA15
DATA14
DATA13
DATA12
DATA11
DATA10
DATA9
DATA8
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
Multiplexed Narrow Bus
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
Internal Logic 2.5V
VDD1,2
VSS1,2
I/O Driver 5V
VDDX
VSSX
PLL 2.5V
VDDPLL
VSSPLL
A/D Converter 5V &
Voltage Regulator Reference
VDDA
VSSA
Voltage Regulator 5V & I/O
VDDR
VSSR
Not all functionality shown in this
Block diagram is available in all Versions!
ATD0
VRH
VRL
VDDA
VSSA
AN0
AN1
AN2
AN3
AN4
AN5
AN6
AN7
AD0
PAD00
PAD01
PAD02
PAD03
PAD04
PAD05
PAD06
PAD07
ATD1
VRH
VRL
VDDA
VSSA
AN0
AN1
AN2
AN3
AN4
AN5
AN6
AN7
AD1
PAD08
PAD09
PAD10
PAD11
PAD12
PAD13
PAD14
PAD15
PPAGE
PIX0
PIX1
PIX2
PIX3
PIX4
PIX5
ECS
DDRK
PTK
PK0 XADDR14
PK1 XADDR15
PK2 XADDR16
PK3 XADDR17
PK4 XADDR18
PK5 XADDR19
PK7 ECS/ROMONE
Enhanced Capture Timer
IOC0
IOC1
IOC2
IOC3
IOC4
IOC5
IOC6
IOC7
DDRT
PTT
PT0
PT1
PT2
PT3
PT4
PT5
PT6
PT7
SCI0
RXD
TXD
SCI1
RXD
TXD
DDRS
PTS
PS0
PS1
PS2
PS3
PS4
PS5
PS6
PS7
SPI0
MISO
MOSI
SCK
SS
CAN0
RXCAN
TXCAN
CAN4
RXCAN
TXCAN
Module to Port Routing
DDRM
PTM
PM0
PM1
PM2
PM3
PM4
PM5
PM6
PM7
KWJ0
KWJ1
KWJ6
KWJ7
DDRJ
PTJ
PJ0
PJ1
PJ6
PJ7
IIC
SDA
SCL
PWM
PWM0
PWM1
PWM2
PWM3
PWM4
PWM5
PWM6
PWM7
KWP0
KWP1
KWP2
KWP3
KWP4
KWP5
KWP6
KWP7
DDRP
PTP
PP0
PP1
PP2
PP3
PP4
PP5
PP6
PP7
SPI1
MISO
MOSI
SCK
SS
KWH0
KWH1
KWH2
KWH3
KWH4
KWH5
KWH6
KWH7
DDRH
PTH
PH0
PH1
PH2
PH3
PH4
PH5
PH6
PH7
Signals shown in Bold are not available on the 80 Pin Package



Signals shown in **Bold** are not available on the 80 Pin Package

Figure 1. Pin Assignments 112 LQFP for MC3S12R-Family

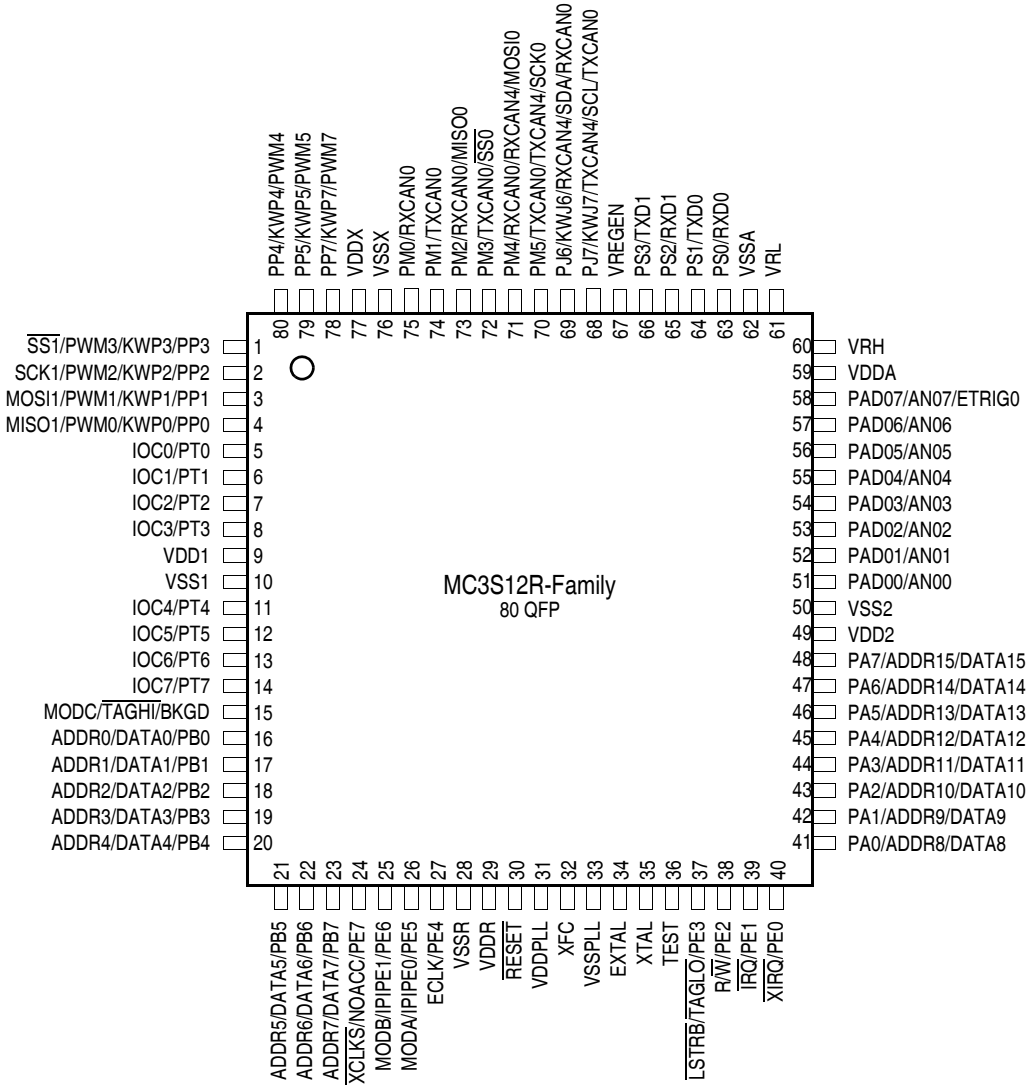
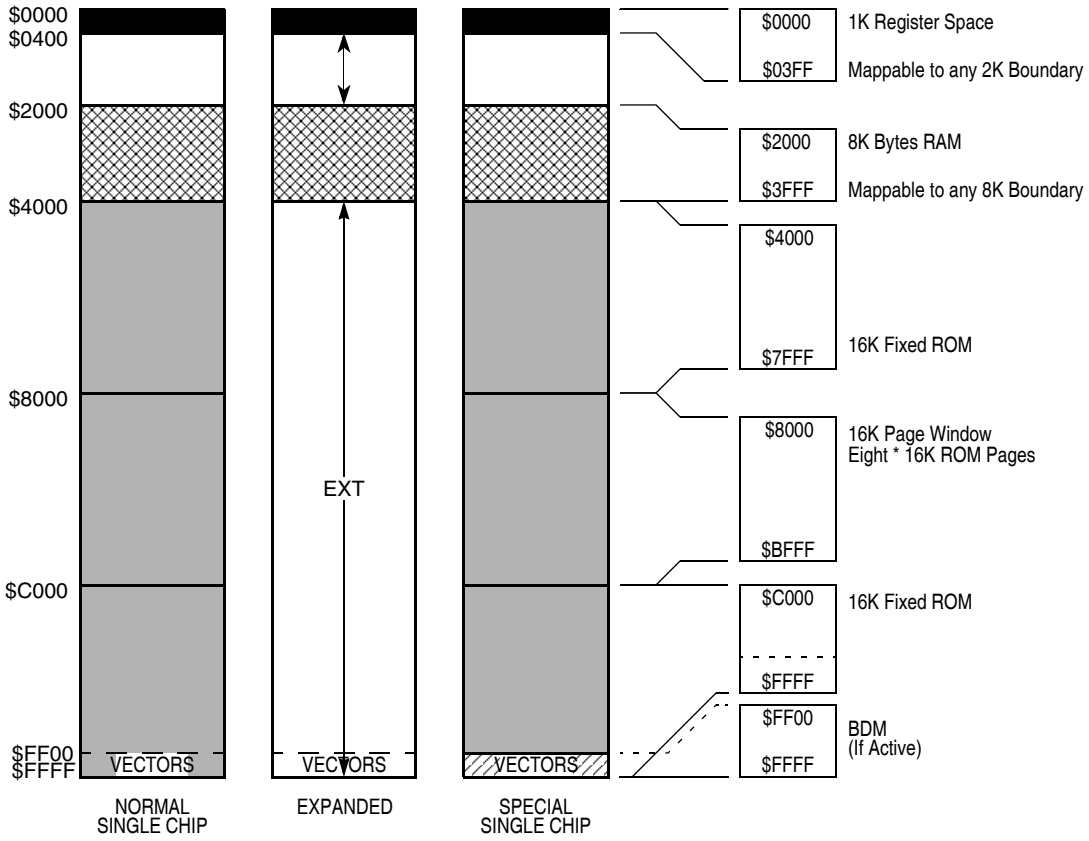


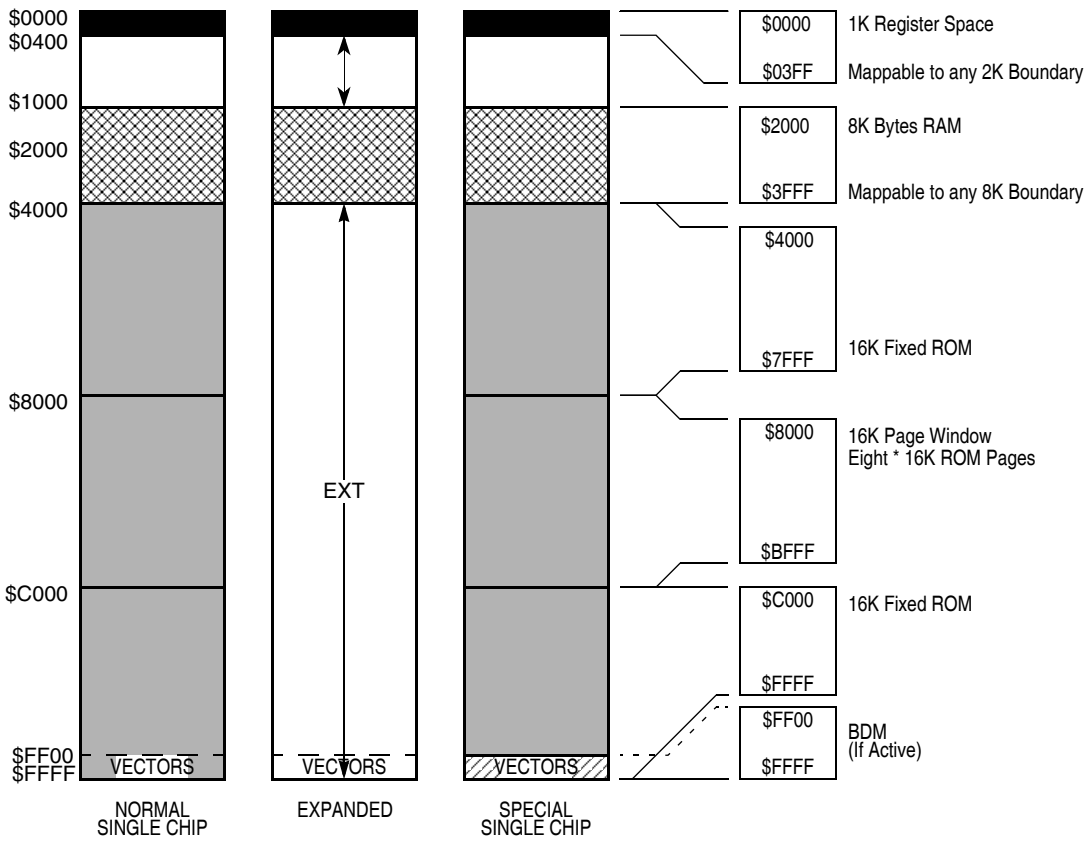
Figure 2. Pin Assignments in 80 QFP for MC3S12R-Family



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000–$03FF: Register Space
$0000–$1FFF: 8K RAM

Figure 3. MC3S12RG128 User Configurable Memory Map

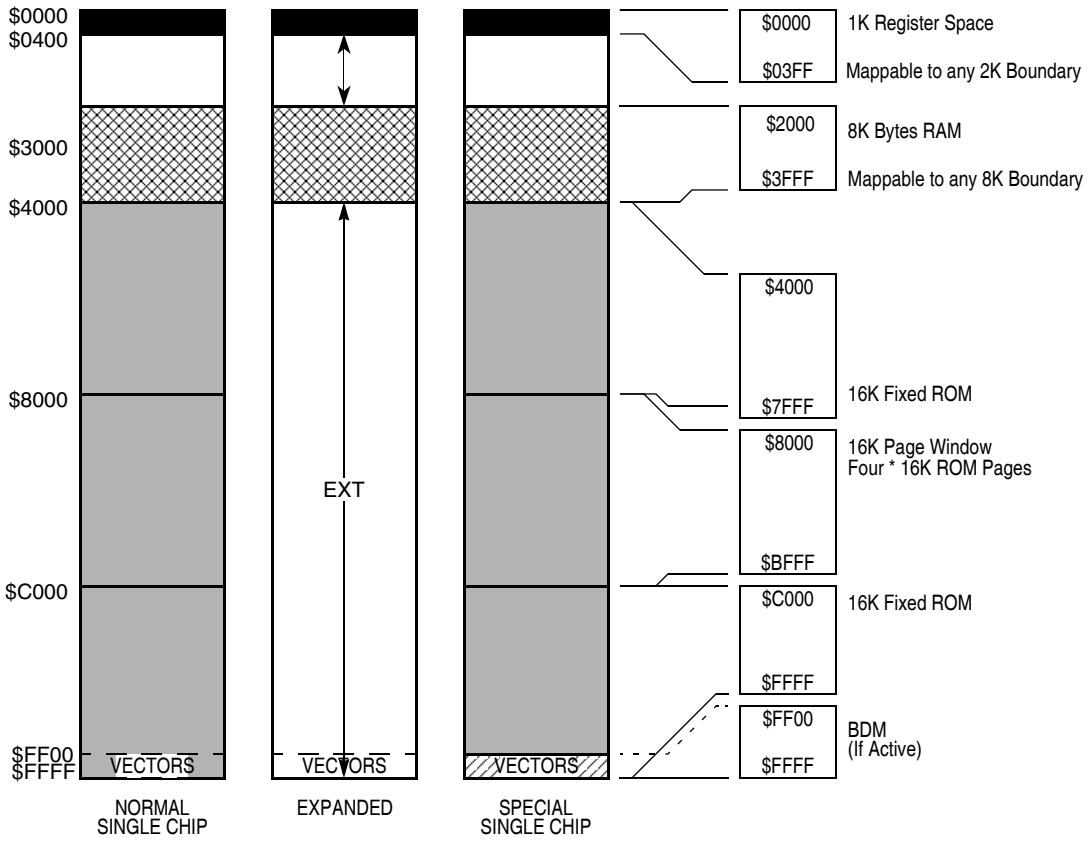


The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000–$03FF: Register Space

$0000–$1FFF: 8K RAM

Figure 4. MC3S12RB128 User Configurable Memory Map

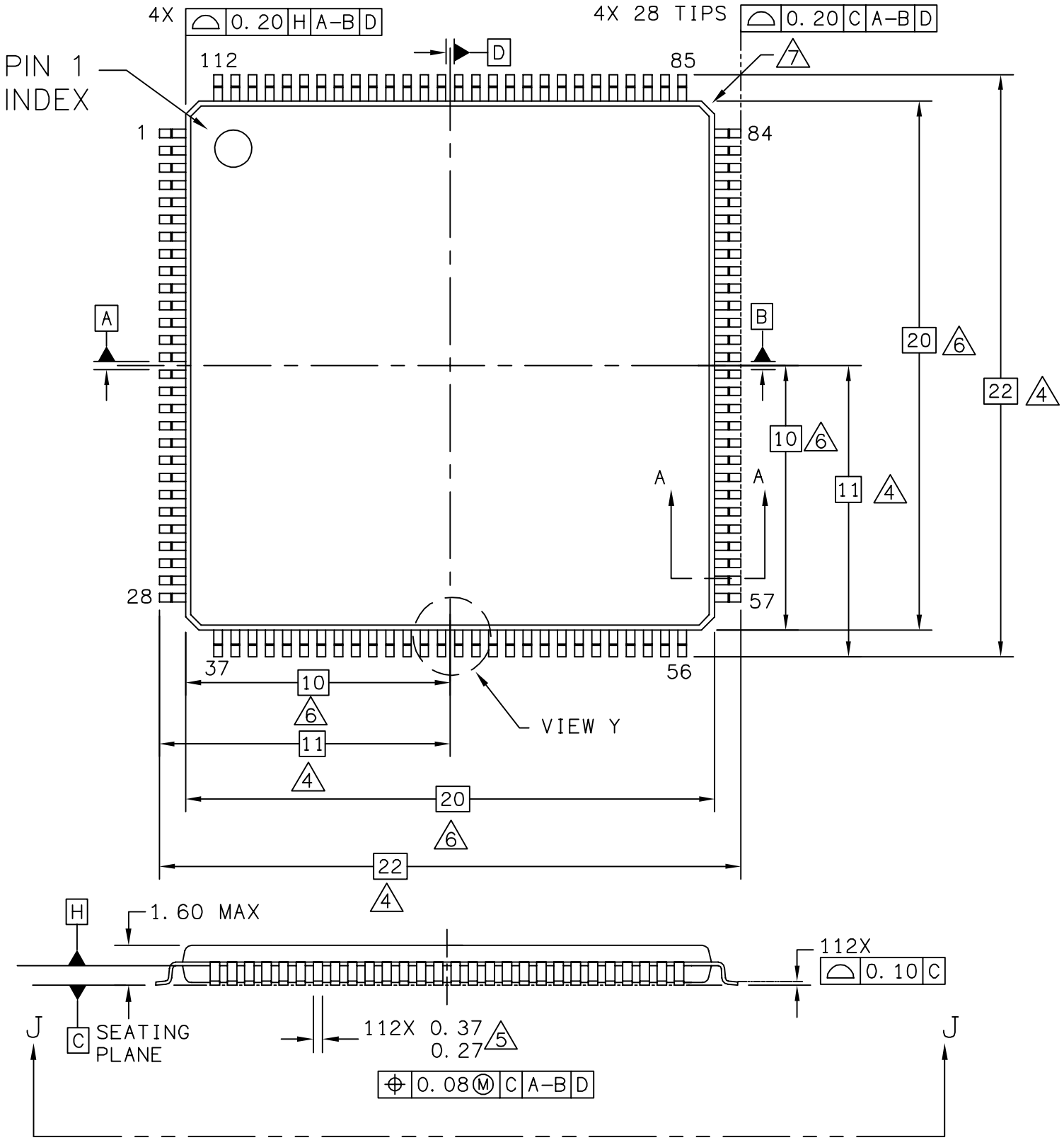


The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000–$03FF: Register Space

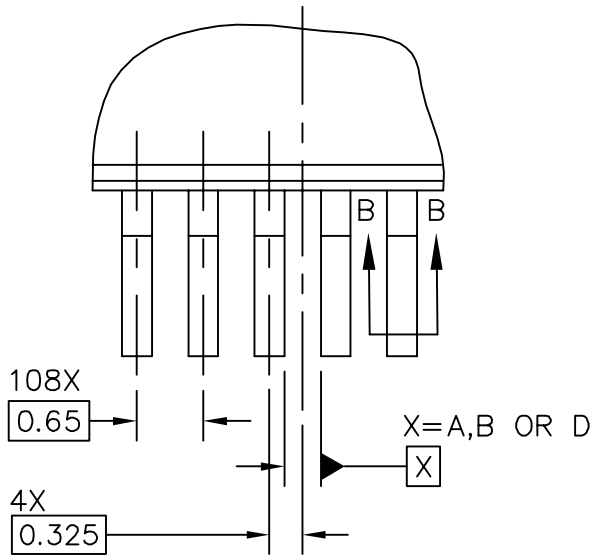
$0000–$1FFF: 8K RAM

Figure 5. MC3S12R64 User Configurable Memory Map

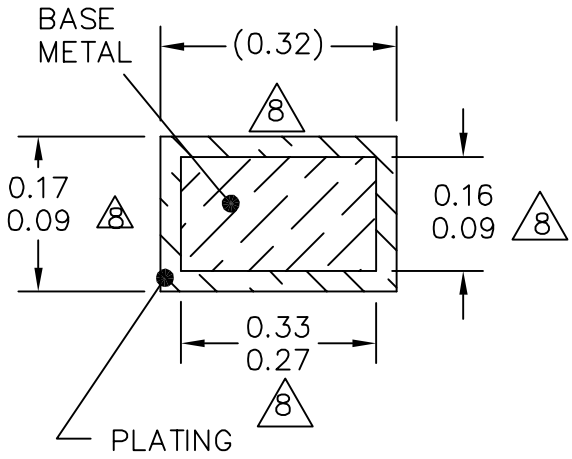


MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

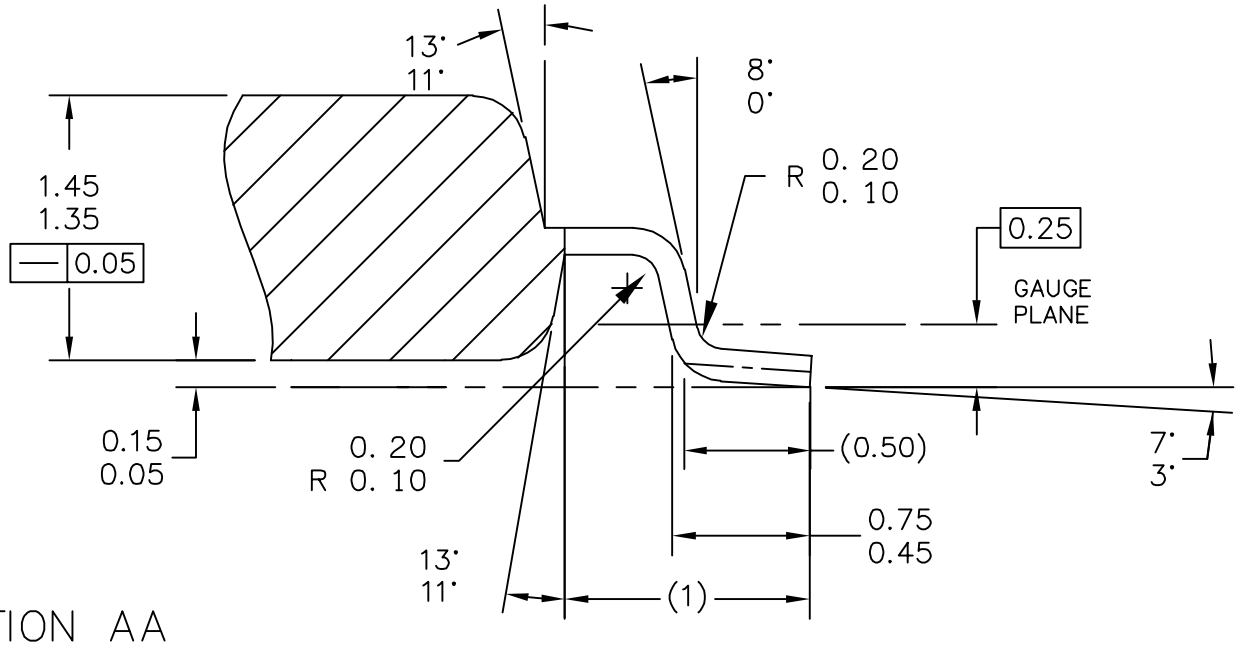
TITLE: 112LD LQFP 20 X 20 X 1.4 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987-02	25 MAY 2005
	STANDARD: JEDEC MS-026 BFA	



VIEW Y



SECTION B–B



SECTION AA

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

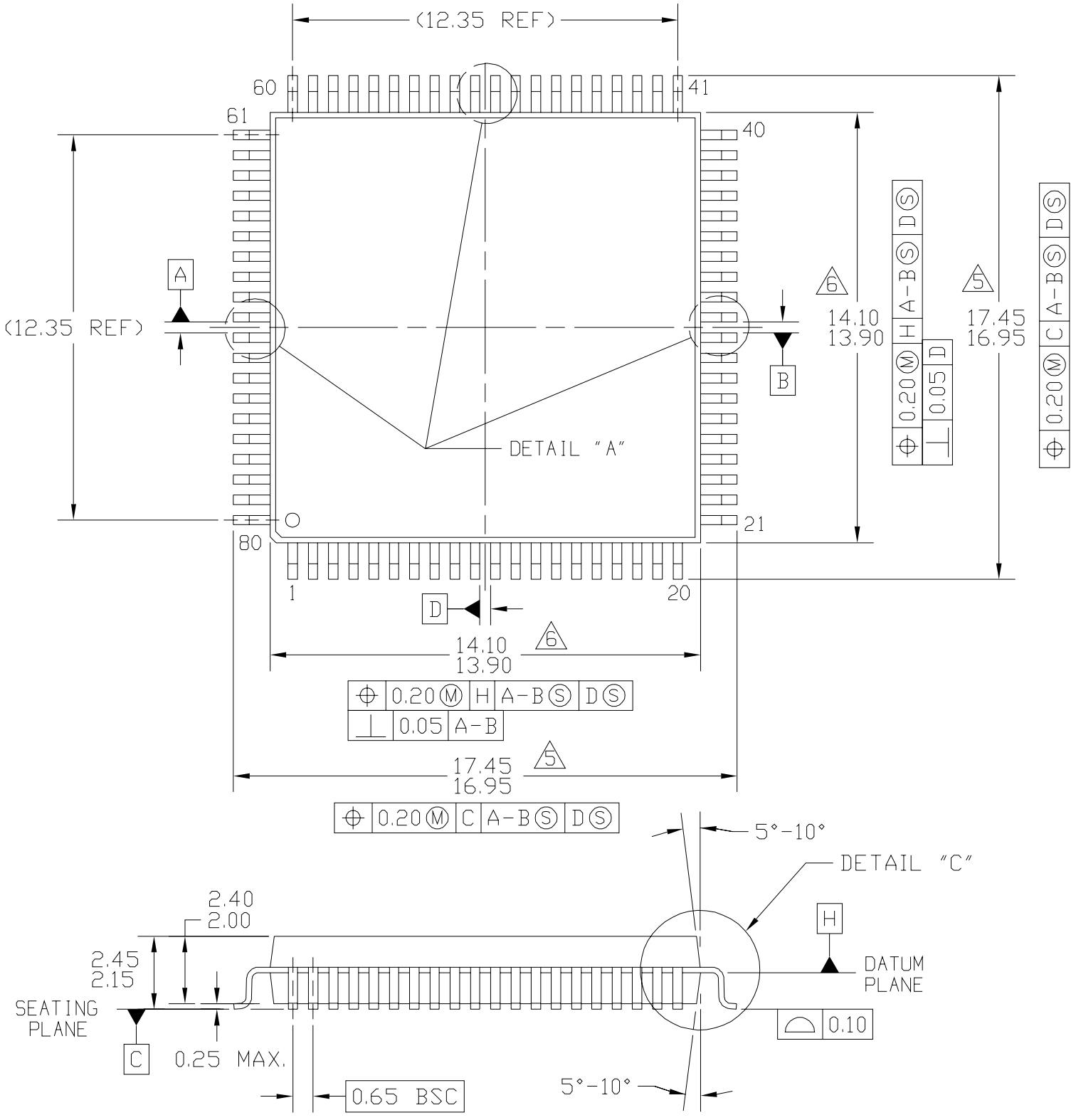
TITLE:	DOCUMENT NO: 98ASS23330W	REV: E
112LD LQFP 20 X 20 X 1.4 0.65 PITCH	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.

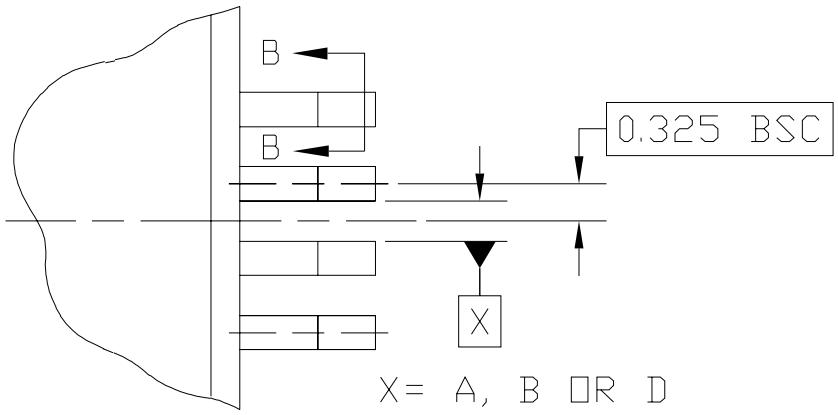
MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: 112LD LQFP, 20 X 20 X 1.4 PKG, 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987-02	25 MAY 2005
	STANDARD: JEDEC MS-026 BFA	

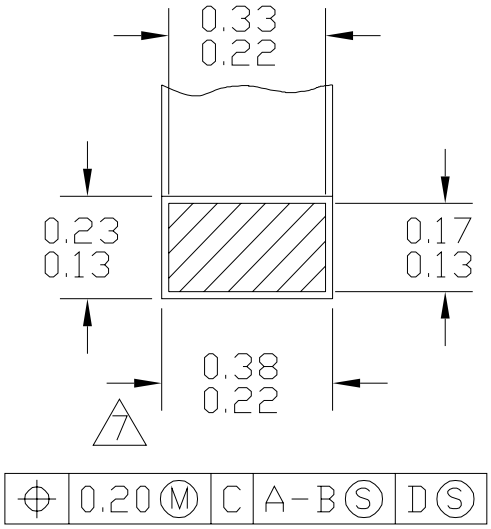


MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

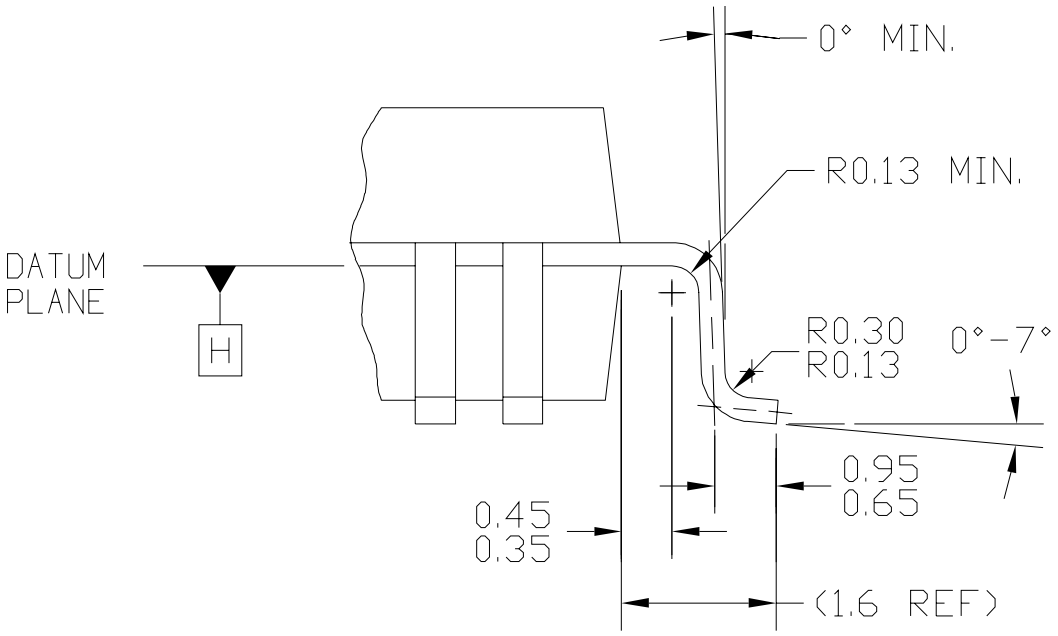
TITLE:	DOCUMENT NO: 98ASB42846B	REV: C
QUAD FLAT PACKAGE, 80 LEAD, 14 X 14 X 2.2 PKG, 0.65 LEAD PITCH	CASE NUMBER: 841B-02	20 MAY 2005
	STANDARD: NON-JEDEC	



DETAIL "A"



SECTION B-B
VIEW ROTATED 90°



DETAIL "C"

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42846B	REV: C
QUAD FLAT PACKAGE, 80 LEAD, 14 X 14 X 2.2 PKG, 0.65 LEAD PITCH	CASE NUMBER: 841B-02	20 MAY 2005
	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

2. CONTROLLING DIMENSION: MILLIMETER.

3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.

5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE -C-.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.

7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42846B	REV: C
QUAD FLAT PACKAGE, 80 LEAD, 14 X 14 X 2.2 PKG, 0.65 LEAD PITCH	CASE NUMBER: 841B-02	20 MAY 2005
	STANDARD: NON-JEDEC	

This page intentionally left blank.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

MC3S12RFAMPB
Rev. 1, 11/2005

freescale™
semiconductor