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Consumer Systems Group

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MPC821

Product Brief

MPC821
PowerPC Personal Systems Microprocessor

The MPC821 microprocessor is a versatile, one-chip integrated microprocessor and peripheral combination that can be used in a variety of portable electronic applications. It is particularly useful in the portable computer and personal communication market. The MPC821 integrates a high-performance embedded PowerPC™ core with a communication processor module that uses a specialized RISC processor for communication. It can perform embedded signal processing functions and support six serial channels—two serial communication controllers, two serial management controllers, a serial peripheral interface, and a interprocessor-integrated communication controller. This two-processor architecture consumes power more efficiently than traditional architectures because the communication processor module frees the PowerPC core from peripheral tasks.

FEATURES

The following list summarizes the main features of the MPC821 microprocessor:

- PowerPC Single-Issue Integer Core
- Precise Exception Model
- Extensive System Development Support
  - ❏ On-chip watchpoints and breakpoints
  - ❏ Program flow tracking
  - ❏ On-chip emulation (OnCE) development interface
- Embedded PowerPC Core Provides 66MIPS (using Dhrystone 2.1) or 115K Dhrystones 2.1 at 50MHz and 33MIPS (using Dhrystone 2.1) or 58K Dhrystones 2.1 at 25MHz
- Low Power (<241mW @ 25MHz, 2.2V Internal, 3.3V I/O for Core, Caches, MMUs, and I/O)
- PowerPC System Interface, Including a Periodic Interrupt Timer, Bus Monitor, and Clocks
- Fully Static Design
- Four Main Power-Saving Modes
  - ❏ Normal, doze, sleep, and power-down
  - ❏ Normal, doze, and sleep modes provide subsets of each mode
- 357-Pin OMPAC Ball Grid Array Packaging
- 32-bit Address and Data Buses
  - ❏ Bus supports multiple master designs
  - ❏ Four-beat transfer bursts and two-clock minimum bus transactions
  - ❏ Dynamic bus sizing controlled by on-chip memory controller
  - ❏ Data parity support
  - ❏ Tolerates 5V inputs, but provides 3.3V outputs

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

SEMICONDUCTOR PRODUCT INFORMATION

- Flexible Memory Management
  - ❏ 32-entry, fully associative instruction translation lookaside buffers
  - ❏ 32-entry, fully associative data translation lookaside buffers
  - ❏ 4K, 16K, 512K, or 8M page size support
  - ❏ 1K protection granularity
  - ❏ Support for multiple protection groups and tasks
  - ❏ Attribute support for trapping, writethrough, cache-inhibit, and memory-mapped I/O
  - ❏ Software tablewalk support
- 4K Physical Address, Two-Way, Set-Associative Data Cache
  - ❏ Single-cycle access on hit
  - ❏ 4-word line size, burst fill, least recently used replacement
  - ❏ Cache lockable online granularity
  - ❏ Tag and attribute reading for debugging purposes
- 4K Physical Address, Two-Way, Set-Associative Instruction Cache
  - ❏ Single-cycle access on hit
  - ❏ 4-word line size, burst fill, least recently used replacement
  - ❏ Cache lockable online granularity
  - ❏ Cache control supports PowerPC invalidate instruction
  - ❏ Cache-inhibit supported for the entire cache or per memory management unit page in conjunction with memory management logic
  - ❏ Tag and attribute reading for debugging purposes
- Eight-Bank Memory Controller
  - ❏ Glueless interface to SRAM, DRAM, EPROM, FLASH and other peripherals
  - ❏ Byte-write enable and selectable parity generation
  - ❏ 32-bit address decodes with bit masks
- System Interface Unit
  - ❏ Clock synthesizer
  - ❏ Power management
  - ❏ Reset controller
  - ❏ PowerPC decrementer and timebase
  - ❏ Real-time clock
  - ❏ Periodic interrupt timer
  - ❏ Hardware bus monitor and software watchdog timer
  - ❏ IEEE 1149.1 JTAG test access port
- Communication Processor Module
  - ❏ Embedded 32-bit RISC microcontroller architecture for flexible I/O
  - ❏ Uses an on-chip dual-port RAM and virtual DMA channel controller to interface with core
  - ❏ Continuous mode transmission and reception on all serial channels
  - ❏ Serial DMA channels for reception and transmission on all serial channels
  - ❏ Parallel I/O registers with open-drain and interrupt capability
  - ❏ Implements memory-to-memory and memory-to-I/O transfers with virtual DMA functionality

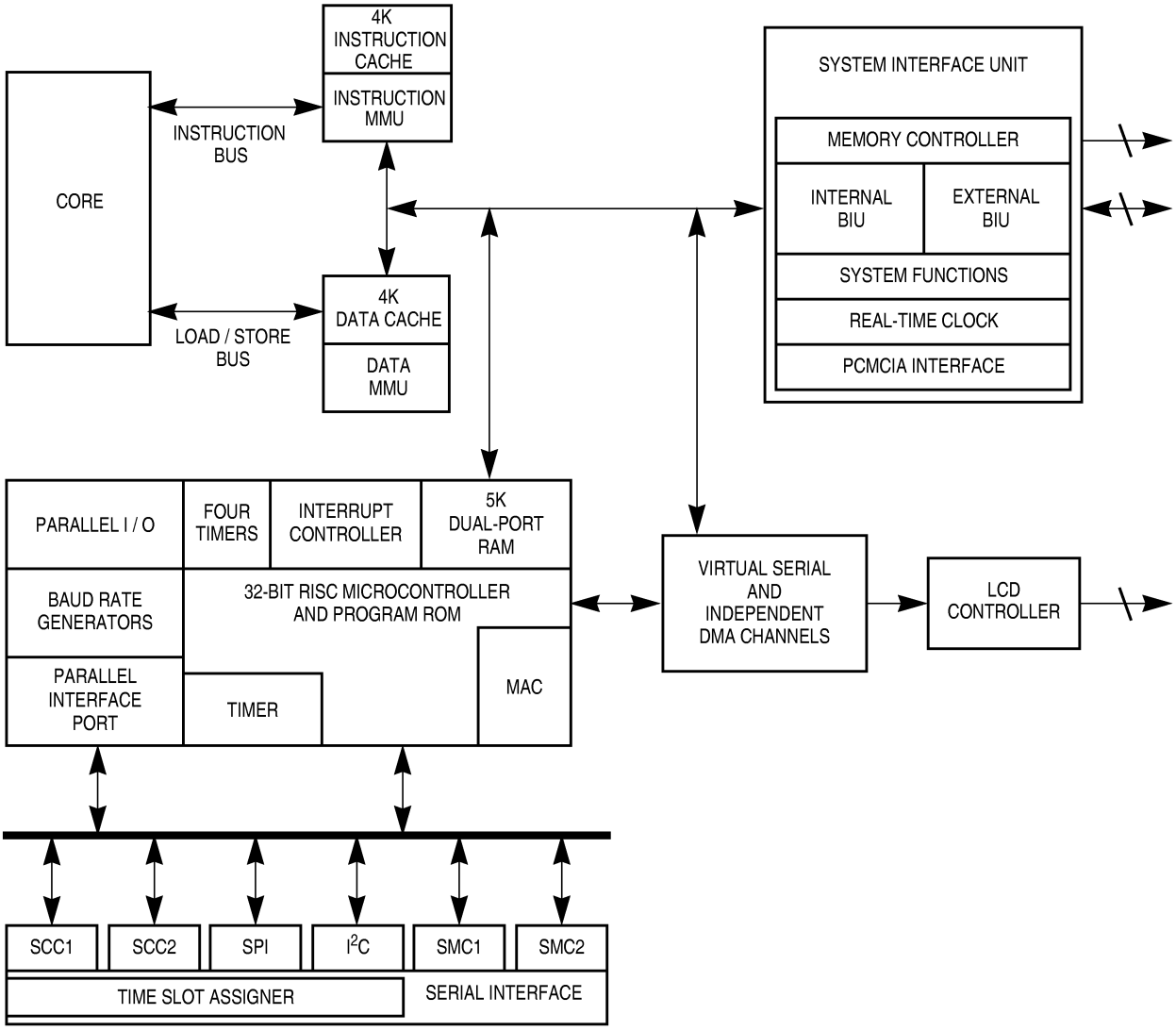
- Protocols supported by ROM or download microcode and the two hardware serial communication controller channels include, but are not limited to, the digital portions of:
  - Ethernet/IEEE 802.3 CS/CDMA
  - HDLC/SDLC™ and HDLC bus
  - AppleTalk™
  - Signaling system #7
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Binary synchronous communication
  - Totally transparent
  - Totally transparent with CRC
  - Profibus (RAM microcode option)
  - Asynchronous HDLC
  - DDCMP
  - V.14 (RAM microcode option)
  - X.21 (RAM microcode option)
  - V.32bis datapump filters
  - IrDA serial infrared
  - Basic rate ISDN (BRI) in conjunction with SMC channels
  - Primary rate ISDN
- Two hardware serial communication controller (SCC) channels support the above protocols
- Two hardware serial management controller (SMC) channels
  - Provides management for BRI devices as general circuit interface controller in time-division multiplexed channels
  - Transparent and low-speed UART operation
- Hardware serial peripheral interface
  - Multimaster, master, and slave mode support
- I^2C™ (microwire compatible) interface
  - Master and slave mode support
- Time-slot assigner
  - One or two TDMA channels supported
  - Bit or byte resolution
  - Independent transmit and receive routing, frame synchronization, and dynamic clocking modification ability
  - Software-configurable for internal interconnection of communication processor module serial channels
  - Typically implements T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate and user-defined TDMA serial interfaces
- Parallel interface port supports Centronics interfaces and chip-to-chip interconnection
- Four independent baud rate generators and four input clock pins used to supply clocks to SMC and SCC serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

- LCD Controller
  - ❏ 1, 2, or 4 bits per pixel gray mode using advanced frame rate control algorithm
  - ❏ 4-, 8-, or 9-bit parallel output to the LCD panel
  - ❏ Single or dual-scan screen support
  - ❏ Data for dual-scan screen: 2+2 or 4+4 parallel bits (2+2 means 2 bits for low screen and 2 bits for high screen in parallel)
  - ❏ TFT / RGB output drives advanced buffer LCD driver chips
  - ❏ Built-in 256 entry color RAM
  - ❏ Maps each 4-bit color code to one of 512 colors, which are defined by a 3-bit code for red, green, and blue.
  - ❏ Maps each 2-bit gray level code to one of eight gray levels
  - ❏ Programmable wait time between lines and frames
  - ❏ Panel voltage control programmable LVDAC through duty cycle for contrast adjustments. Implemented by using another existing on-chip timer.
  - ❏ Programmable polarity for all LCD interface signals
- Two PC Card (PCMCIA 2.1) Master Interface

ARCHITECTURE

The MPC821 microprocessor uses a dual-processor architectural design approach to provide a high-performance, general-purpose RISC integer processor and a special-purpose 32-bit RISC communication processor module. The peripherals are uniquely designed for communication requirements and can provide embedded signal processing functions for communication and user interface enhancements and the I/O support needed for high-speed digital communication. The MPC821 is composed of three main modules that interface with the 32-bit internal bus:

- The embedded PowerPC core
- The system interface unit
- the communication processor module



MPC821 Block Diagram

EMBEDDED PowerPC CORE

The PowerPC core is a fully static design that consists of three functional blocks—an integer block, a hardware multiplier/divider, and a load/store block. It executes all integer and load/store operations directly on the hardware. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. Its interface to the internal and external buses is 32 bits. The PowerPC core uses a 2-instruction load/store queue, a 4-instruction pre-fetch queue, and a 6-instruction history buffer. The core performs branch folding and branch prediction with conditional pre-fetch, but without conditional execution. The PowerPC core can operate on 32-bit external operands with one bus cycle.

The PowerPC integer block supports 32 × 32-bit fixed-point general-purpose registers. It can execute one integer instruction at each clock cycle. Each element in the integer block is clocked only when valid data in the data queue is ready for operation. This reduces the amount of power the device uses to perform an operation. The PowerPC core is integrated with memory management units (MMUs) and 4K instruction and data caches. The MMUs provide a 32-entry fully-associative instruction and data TLB with 4K (1K protection), 16K, 512K, and 8M page sizes. It supports 16 virtual address spaces with eight protection groups. Three special registers are available as scratch registers to support software tablewalk and update.

The 4K, two-way, set-associative instruction cache with physical addressing allows single cycle access on hit with no added latency for miss. It has four words per line and supports burst line fill using an LRU replacement algorithm. The cache can be locked on a line basis for application critical routines. The 4K, two-way, set-associative data cache with physical addressing allows single cycle access on hit with one added clock latency for miss. It has four words per line and supports burst line fill using an LRU replacement algorithm. The cache can be locked on a line basis for application critical routines. Via the memory management unit, the data cache can be programmed to support copyback or writethrough mode. The inhibit mode can be programmed on a per-MMU page basis.

The PowerPC core uses the instruction and data caches to deliver approximately 66MIPS at 50MHz (using Dhrystone 2.1) or 115K Dhrystones and 33MIPS at 25MHz (using Dhrystone 2.1) or 58K Dhrystones. This is based on the assumption that it is issuing one instruction per cycle with a cache hit rate of 94%.

COMMUNICATION PROCESSOR MODULE

The communication processor module is where the MPC821 gets its communication capabilities. It has features that allow the MPC821 to excel in a variety of low-power personal communication and control applications. These features are divided into three blocks:

- RISC communication processor
- Twelve serial DMA channels
- Four general-purpose timers

The communication processor module consists of multiply accumulate hardware, two serial communication controllers (SCCs), two serial management controllers (SMCs), one serial peripheral interface (SPI), one interprocessor-integrated communication (I^2C) controller, a 5K dual-port RAM, an interrupt controller, a time-slot assigner, three parallel ports, a parallel interface port, and four independent baud rate generators. These allow you to maximize your system flexibility and throughput.

The twelve serial DMA channels support the SCCs, SMCs, and SPIs. The independent DMAs provide two channels of general-purpose DMA capability for each serial DMA channel. IDMAs offer high-speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic. The RISC microcontroller can access the IDMA registers directly in the buffer chaining modes. The four general-purpose timers on the communication processor module are functionally similar to the two general-purpose timers found on the MC68360 Quad Integrated Communication Controller (QUICC). However, they offer some minor enhancements, such as the internal cascading of two timers to form a 32-bit timer. The MPC821 also contains a periodic interval timer in the system interface unit, which brings the total of on-chip timers to five.

SYSTEM INTERFACE UNIT

The system interface unit provides support for traditional 68K big-endian memory system interfaces, traditional ×86 little-endian memory systems, and PowerPC little-endian memory systems. It also provides power management functions, reset control, PowerPC decrementer and timebase, and a real-time clock. Although, internally, the PowerPC core is always a 32-bit device, it can be configured to operate with an 8-, 16-, or 32-bit data bus. Regardless of the system bus size, dynamic bus sizing is supported, which allows 8-, 16-, and 32-bit peripherals and memory to coexist on a 32-bit system bus.

The memory controller supports up to eight memory banks with glueless interfaces to DRAM, SRAM, PSRAM, EPROM, Flash EPROM, SRDRAM, EDO, and other peripherals with two-clock initial access to external SRAM and bursting support. It provides variable block sizes between 32K and 256M. The memory controller provides 0 to 15 wait states for each bank of memory and uses address type matching to qualify each memory bank access. It provides four byte-enable signals for varying width devices, one output enable signal, and one boot chip-select available at reset.

The DRAM interface supports 8-, 16-, and 32-bit ports and uses a programmable state machine to support almost any memory interface. Memory banks can be defined in depths of 256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, or 64M for all port sizes. In addition, the memory depth can be defined as 64K and 128K for 8-bit memory or 128M and 256M for 32-bit memory. The DRAM controller supports page mode access for successive transfers within bursts. The MPC821 supports a glueless interface to one bank of DRAM, while external buffers are required for additional memory banks. The refresh unit provides CAS before RAS, a programmable refresh timer, active refresh during external reset, refresh disable modes, and stacking for up to seven refresh cycles.

LCD CONTROLLER

The LCD controller on the MPC821 supports a versatile interface. It provides monochrome or 4/16-level grayscale, 256 color TFT (9 bits, 3 × 3 RGB), and passive color (×STN) 4/8-bit data. The controller supports 4-bit non-split, 8-bit non-split, 2+2-bit split, or 4+4-bit split. It is programmable for frame rate, number of pixels per line, and number of lines per frame. The panel voltage is programmable through a duty cycle for contrast adjustments implemented in the communication processor module program. Display data is stored in your own memory space and is transferred into the controller using the DMA channels.

PCMCIA CONTROLLER

The PCMCIA interface is a master controller and that is compliant with Release 2.1. The interface supports a maximum of two independent PCMCIA sockets with the required external transceivers/buffers. It provides eight memory or I/O windows and each window can be allocated to each socket. If only one PCMCIA port is being used, the unused PCMCIA port can be used as a general-purpose input with interrupt capability.

POWER MANAGEMENT

The MPC821 supports a wide range of power management features including normal, doze, sleep, and power-down modes. In normal mode, the MPC821 is fully powered with all internal units operating at the full speed of the processor. Each of the normal low, doze high, doze low, sleep, and power-down modes define lower power with less operational features. Doze mode disables core functional units except the timebase decrementer, PLL, memory controller, real-time clock, and LCD controller, and places the communication processor module in low-power standby mode. Sleep mode is the next lower power mode that disables everything else except the real-time clock and periodic interrupt timer, thus leaving the PLL active for quick wake-up. Power-down mode disables all logic in the processor (except the minimum logic required to restart the device). It uses the least amount of power, but it requires the longest wake-up time.

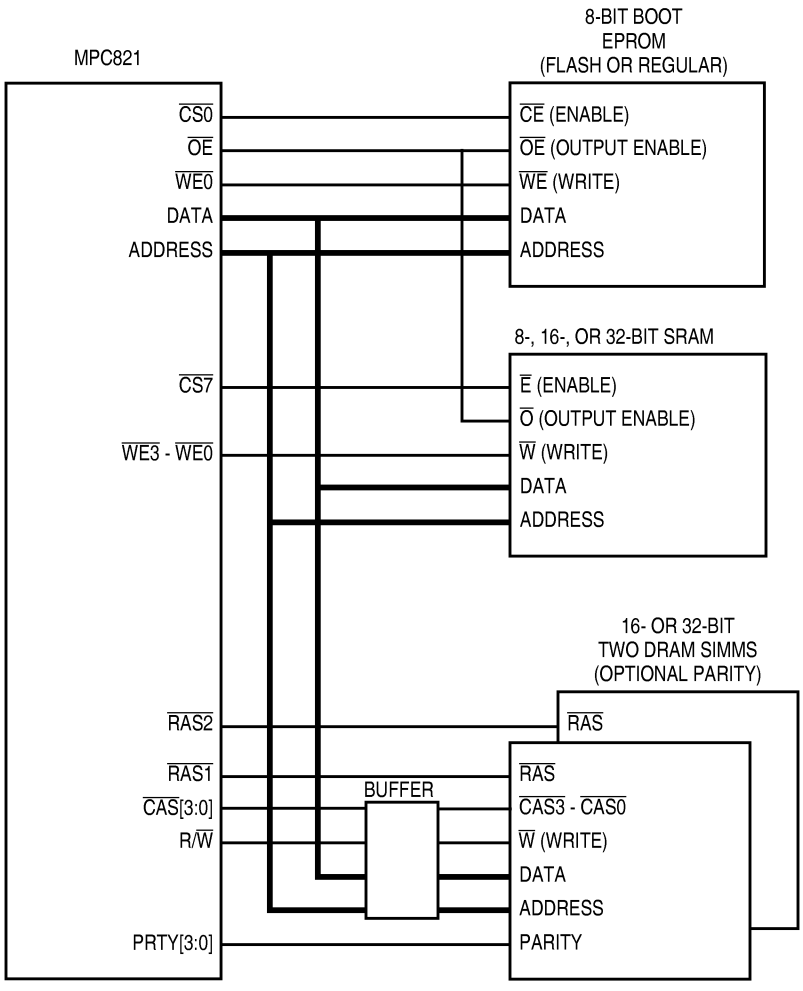
The MPC821 also provides a separate set of power pins for the internal logic in the device. These power pins can be used to provide the device with a 2.2V power source that can be used when the processor is operating at 25MHz or less. This capability reduces the power consumption of the device by an additional 30%.

SYSTEM DEBUG SUPPORT

The MPC821 contains an advanced debug interface that provides superior debug capabilities without causing any degradation in the speed of operation. It supports six watchpoint pins that can be combined with eight internal comparators, four of which operate on the address on the instruction bus. The other four comparators are split— two comparators operate on the address on the load/store bus and two comparators operate on the data on the load/store bus. The MPC821 can compare using =, ≠, <, > conditions to generate watchpoints. Each watchpoint can then generate a breakpoint to be programmed to trigger in a programmable number of events.

MPC821 GLUELESS SYSTEM DESIGN

The MPC821 is designed to interface easily with other system components. Figure 2 illustrates a system configuration that offers one EPROM, one flash EPROM, and supports two DRAM SIMMs. Depending on the capacitance of the system bus, external buffers may be required as they are for the dual DRAM-bank design shown. From a logic standpoint, however, a glueless system is maintained and buffers would not be required for single DRAM-bank systems.



MPC821 System Configuration

The following table contains the package type and operating frequencies of the MPC821. For part numbers with an xxx or xx suffix, check for the most current revision before ordering. The table below only contains the base part numbers.

PACKAGE TYPE	FREQUENCY	TEMPERATURE	BASE PART NUMBER
Ball Grid Array Ball Grid Array	0-25MHz 0-50MHz 25MHz	0 to 70˚ C 0 to 70˚ C -40 to 85˚ C	XPC821ZP25xxx XPC821ZP50xxx XPC821CZP25xx

The documents listed in the table below contain detailed information on the MPC821. You can obtain these documents from the Motorola Literature Distribution Center closest to you or from our website at www.mot.com/mpc821.

DOCUMENT TITLE	PART NUMBER	CONTENTS
MPC821 User's Manual	MPC821UM/D	Detailed Information for Design
PowerPC Microprocessor Family: The Programming Environments for 32-Bit Microprocessors	MPCFPE32B/D	PowerPC Instruction Set
PowerPC Resource Guide	BR1724/D	Independent Vendor Listing of Supporting Software and Development Tools

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

SEMICONDUCTOR PRODUCT INFORMATION

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