Freescale Semiconductor
Product Brief

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MSC8157 Product Brief

Broadband Wireless Access DSP

The MSC8157 device is a member of the fourth generation of Freescale high-end multicore DSP devices that target the communications infrastructure. It builds upon the proven success of the previous multicore DSPs and is designed to support mainly the 3G-LTE (FDD and TDD), HSPA+, LTE-Advanced, and WiMAX markets. The MSC8157 is pin compatible with the MSC8157, MSC8158, and MSC8158E devices.

Contents

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1 Features

The MSC8157 device targets high-bandwidth highly computational DSP applications and is optimized for 3G-LTE (FDD and TDD), UMTS, and WiMAX applications. The device includes a combination of fully programmable DSP cores and powerful hardware acceleration to provide best in class performance, power efficiency, connectivity, and cost effectiveness.

1.1 Block Diagram

The MSC8157 devices are highly integrated DSP processors that contain six StarCore SC3850 DSP subsystems with 32 Kbyte L1 instruction cache per core, 2 Kbyte L1 instruction cache per core; 32 Kbyte L1 data cache per core; 512 Kbyte L2 unified instruction/data cache per core (can be configured as M2 Memory) and 3072 Kbyte of shared M3 memory (for a total of 6 Mbyte internal memory); a DDR memory controller; a second generation of multi-accelerator platform engine (MAPLE-B2) for forward error correction schemes including Turbo or Viterbi decoding, Turbo encoding and rate matching, MIMO MMSE, IRC and ML equalization schemes, matrix operations, CRC insertion and check, DFT/iDFT and FFT/iFFT calculations, and Chip Rate acceleration; two Serial RapidIO interfaces; six lanes Common Public Radio Interface (CPRI) v4.1 controller; two Gigabit Ethernet controllers; a PCI-Express controller; a 16 bidirectional channels DMA controller; an SPI interface; a UART interface; and an I^2C interface. A dual RISC-engine QUICC Engine subsystem supports the two Gigabit Ethernet controllers and the SPI controller. A 10-lane High-Speed Serial Interface (HSSI) subsystem with two DMA controllers supports and multiplexes the signals for the two Serial RapidIO controllers including an enhanced Messaging Unit, six CPRI controllers, and PCI-Express controller and also multiplexes the two SGMII ports. Each SC3850 DSP core has four ALUs each with a dual 16×16 MAC per ALU and performs at 8000 million multiply accumulates per second (MMACS) at 1 GHz yielding a maximum total performance of 48000 MMACS per device.

In each SC3850 core subsystem, the SC3850 core connects to the following:

- 32 Kbyte 8-way level 1 instruction cache (L1 ICache)
- 32 Kbyte 8-way level 1 data cache (L1 DCache)
- 512 Kbyte 8-way level 2 unified instruction/data cache (L2 Cache/M2 Memory)
- Memory management unit (MMU)
- Enhanced programmable interrupt controller (EPIC)
- Debug and profiling unit (DPU)
- Two 32-bit timers

A block diagram of the MSC8157 is shown in Figure 1. A separate block diagram for the SC3850 DSP core platform is shown in Figure 2. Figure 3 shows a block diagram of MAPLE-B2.

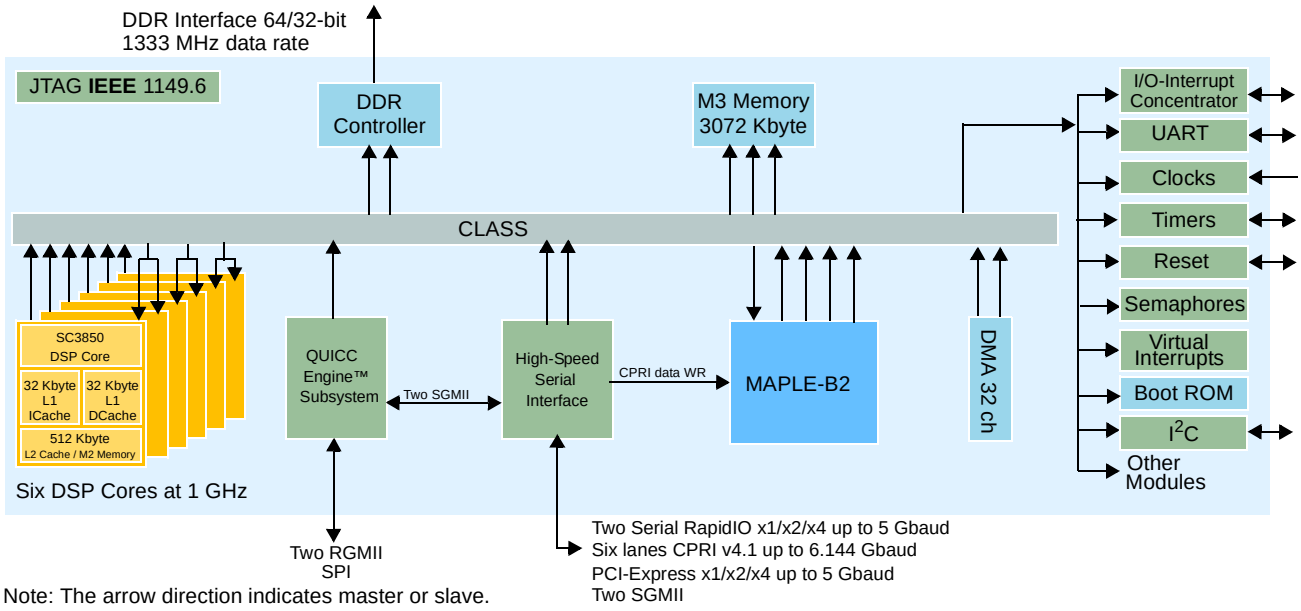

Figure 1. MSC8157 Block Diagram

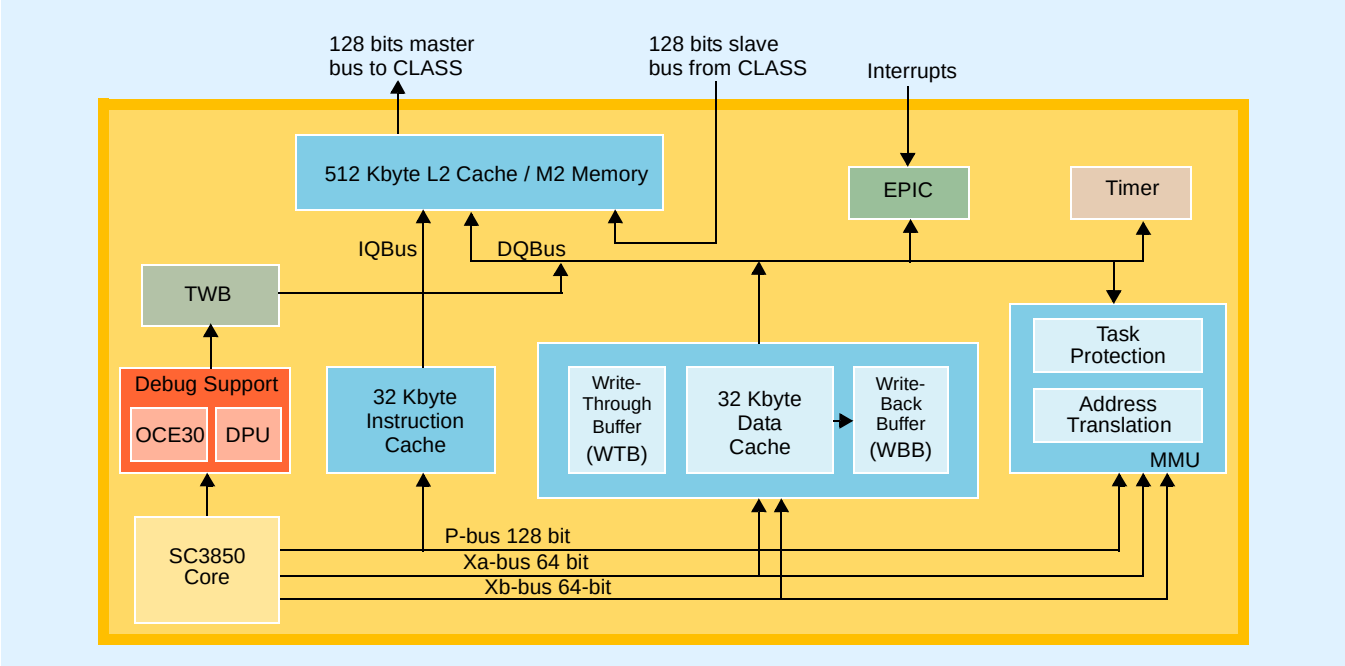

Figure 2. StarCore SC3850 DSP Subsystem Block Diagram

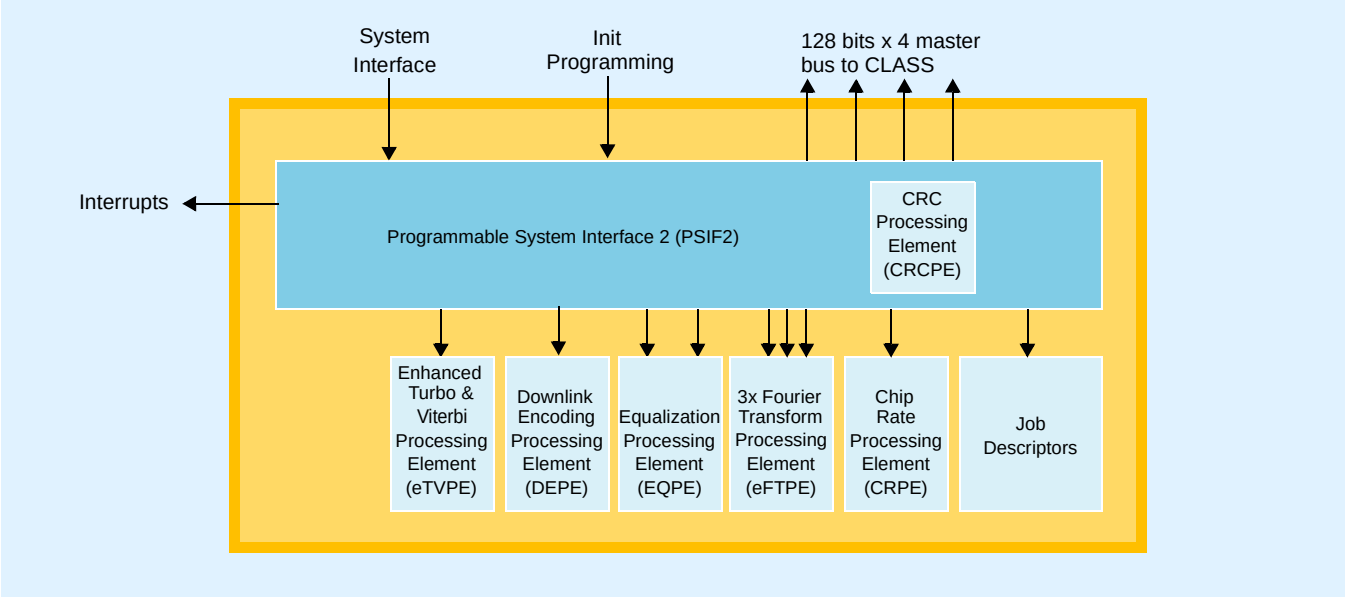

Figure 3. MAPLE-B2 Block Diagram

1.2 Critical Performance Metrics

- Offered with a core frequency of 1 GHz, supports:
  - Eight 16 × 16 or 8 × 8 multipliers, enabling up to 48000 MMACS at 1 GHz with six SC3850 cores. A multiply-accumulate operation includes a multiply-add instruction with the associated data move and pointer update. This is double MMACS versus the pervious generation SC3400 DSP core.
  - The six cores deliver a performance equivalent to a single core running at 6 GHz.
- The MAPLE-B2 supports:
  - Turbo decoding including rate matching supporting up to 330 Mbps for 3GLTE, up to 350 Mbps, and up to 260 Mbps for UMTS for WiMAX at 8 full iterations.
  - Turbo encoding: information bits encoding including rate matching up to 1.8 Gbps for 3GLTE and WiMAX and up to 900 Mbps for UMTS.
  - Viterbi decoding up to 150 Mbps for K=9, zero tailing and up to 200 Mbps for K=7 tail biting.
  - FFT/iFFT processing supporting up to 1500 Msps[1].
  - DFT/iDFT processing supporting up to 900 Msps[2].
  - CRC check and insertion supporting up to 10 Gbps.
  - MMSE/IRC Equalization. Up to 90 M[scps] for 4 × 2 and 30 M[scps] for 4 × 4 equalization.
  - ML-based Equalization. Up to 80 M[scps] for 4 × 2 and 50 M[scps] for 4 × 4 equalization.
  - Matrix Inversion. Up to 75 M[invps] for 2 × 2 matrices 25 M[invps] for 4 × 4 matrices
  - UMTS downlink spreading, scrambling, gain and combining of up to 512 Physical Channels including MIMO, STTD, TSTD and Closed Loop Mode 1 operation per channel.Chip rate despreading/spreading and descrambling/scrambling up to 360 R99 users.

1.Assuming no DFT/iDFT acceleration. For details, see the MAPLE-B2 features on page 8.
2.Assuming no FFT/iFFT acceleration. For details, see the MAPLE-B2 features on page 8.

  - UMTS uplink batch interpolation, despreading, descrambling, combining and frequency correction for up to 384 Physical Channels with up to 2144 total fingers from up to 24 antenna streams with max 512 chips delay spread.
  - UMTS uplink low latency DCPCCH and E-DPCCH interpolation, despreading, descrambling of up to 400 Physical channels with up to 3200 EOL total fingers from up to 24 antenna streams.
  - UMTS Path searcher and RACH correlations in frequency domain.
  - UMTS Frequency Domain Equalization acceleration
- Dual RISC core QUICC Engine subsystem operating at up to 500 MHz provides parallel packet processing independent of the DSP cores, allowing the cores to process data while the RISC engines manage the data flow and packetization.
- Power supplies:
  - Core power: 1 V nominal
  - I/O power: 1.0 V, 1.5 V, and 2.5 V nominal
- Flip Chip-Plastic Ball Grid Array (FC-PBGA), 783-ball, 1 mm pitch, 29 mm × 29 mm

1.3 Device Level Features

This multicore DSP delivers a high level of performance and integration, combining six fully-programmable StarCore DSP cores, each running at up to 1 GHz with an architecture highly optimized for wireless applications. The MAPLE-B2 supports hardware acceleration for forward error correction schemes including Turbo or Viterbi decoding, Turbo encoding and rate matching, MIMO MMSE and ML equalization schemes, matrix operations, CRC insertion and check, DFT/iDFT and FFT/iFFT calculations, and Chip Rate acceleration. It also includes a second generation quad-RISC based Programmable System Interface (PSIF2), which has a CRC accelerator and DMA capabilities that can offload some of the data flow management from the cores. An internal dual-RISC-based QUICC Engine subsystem supports multiple networking protocols to guarantee reliable data transport over packet networks while significantly off loading such processing from the DSP cores. The MSC8157 embeds large internal memory and supports a variety of advanced interface types, including two RapidIO interfaces, six CPRI lanes for glueless antenna connection, two gigabit Ethernet interfaces for network communications, a PCI-Express controller and a DDR controller for high-speed, industry-standard memory interface.

1.4 Module Level Features

- StarCore DSP subsystem. The DSP subsystem includes:
  - StarCore SC3850 core
    - Running at up to 1 GHz
    - Up to 8000 16-bit or 8-bit MMACS. A MAC operation includes a multiply-accumulate command with the associated data moves and a pointer update.
    - Backwards binary compatible with the SC140 and SC3400 architectures.
    - Data Arithmetic and Logic Unit (DALU) containing 4 ALUs, each capable of performing 2 16 × 16 multiply accumulate operations
    - Address Generating Unit (AGU) containing 2 Address Arithmetic Units (AAU)
    - Up to six instructions executed in a single clock cycle: 4 DALU and 2 AGU instructions
    - Variable-length Execution Set (VLES) execution model.
    - 16 data registers, 40 bits each; 27 address registers, 32 bits each.
    - Hardware support for fractional and integer data types.
    - Four hardware loops with near-zero cycle overhead
    - Very rich 16-bit wide orthogonal instruction set.
    - Application specific instructions for Viterbi and Multimedia processing.
    - Special SIMD (Single instruction, multiple data) instructions working on 2-word or 4-byte operands packed in a register, enabling to perform 2 to 4 operations per instruction (8 to 16 operations per VLES)
    - Dedicated instructions for FFT acceleration
    - User and Supervisor privilege levels, supporting a protected SW model
    - Instructions and features to improve control code performance
    - Precise exceptions for memory accesses enabling good RTOS support and Soft Error corrections
    - Branch Target Buffer (BTB) for acceleration of change of flow operations
  - L1 ICache:
    - 32 Kbytes
    - 8 ways with 16 lines of 256 bytes per way
    - Multi-task support
    - Real-time support through locking flexible boundaries
    - Line pre-fetch capability
    - Software coherency support
    - Software pre-fetch support by core instructions
  - L1 DCache:
    - 32 Kbytes
    - 8 ways with 16 lines of 256 bytes per way
    - Capable of serving two data accesses in parallel (XA, XB)
    - Multi-task support
    - Real-time support through locking flexible boundaries
    - Software coherency support
    - Writing policy programmable per memory segment as either write-back or write-through
    - 0.25 Kbytes Write-back Buffer (WBB)
    - Six 64-bit entry WTB

  - Line pre-fetch capability
  - Software pre-fetch, synchronize, and flush support by core instructions
- Unified L2 Cache/M2 Memory:
  - 512 Kbyte
  - 8 ways with 1024 indexes and a 64 byte line
  - Physically addressed
  - Dynamically configured as a DMA accessible M2 Memory
  - Maximum user flexibility for real time support through address partitioning of the cache
  - Support various write policies and methods to reduce cache inclusiveness
  - Multi-channel, two dimensional software pre-fetch support
  - Software coherency support with seamless transition from L1 cache coherency operation.
- Memory management unit (MMU):
  - Highly flexible memory mapping capability
  - Provides virtual to physical address translation
  - Provides task protection
  - Supports multi-tasking
  - Supports precise interrupts. Enabling to have an open RTOS.
- Debug and Profiling Unit (DPU) block:
  - Supports the debugging and profiling of the platform in cooperation with the OCE Block
  - Supports various breakpoint and event counting options
  - Supports real-time tracing to the main memory with the Trace Write Buffer (TWB)
- Extended programmable interrupt controller (EPIC)
  - 256 interrupts
  - 32 priority levels with NMI support
- Two general-purpose 32-bit timers
- Low-power design with the following modes of operation:
  - Wait processing state for peripheral operation
  - Stop processing state
  - Power down processing state
- ECC/EDC support.

- Chip-level arbitration and switching system (CLASS)
  - A full fabric that arbitrates between the DSP cores and other CLASS masters to the core M2 memory, shared M3 memory, DDR SDRAM controller, MAPLE-B2, and the device configuration control and status registers (CCSRs).
  - High bandwidth.
  - Non-blocking allows parallel accesses from multiple initiators to multiple targets.
  - Fully pipelined.
  - Low latency.
  - Per target arbitration highly optimized to the target characteristics using prioritized round-robin arbitration.
  - Reduces data flow bottlenecks and enables high-bandwidth internal data transfers.

- Internal memory. The 6624 Kbyte for MSC8157 internal memory space includes:
  - 32 Kbyte L1 ICache per core.
  - 32 Kbyte L1 DCache per core.
  - 512 Kbyte unified L2 Cache/M2 Memory per core.
  - 3072 Kbyte shared triple-bank, triple-port M3 memory. Power supply of two banks (2048 Kbyte) can be turned off to reduce power dissipation.
  - 96 Kbyte boot ROM accessible from the cores.
- Clocks
  - Three input clocks:
    - Global input clock.
    - Two differential input clocks (one per each SERDES PLL).
  - Six PLLs:
    - Three system PLLs
    - Two SERDES PLLs
    - DDR Controller PLL
  - Clock ratios selected during reset via reset configuration pins.
  - Clock modes user-configurable after reset.
- Second Generation Multi Accelerator Platform Engine for Baseband (MAPLE-B2)
  - Two PGC units: one for eTVPE and one for EQPE. The PGCs permits the user to remove power for the eTVPE and EQPE internally, either statically or dynamically, which can also reduce power consumption when this processing is not needed.
  - Separate power for the Chip Rate Processing Element (CRPE). This can be disabled for power reduction if the CRPE is not required.
  - Turbo decoding for WiMAX, UMTS and 3GLTE systems using an eTVPE module:
    - Turbo decoder, rate-dematcher and HARQ combining acceleration
    - Each decoder scalable with 1, 2, or 4 Radix 4 dual-recursion engines
    - Binary and duo-binary codes
    - Trellis termination and tail biting
    - Various rate de-matching functions support for rate 1/3 code including sub-block de-interleaving and de-interlacing
    - Max Log Map or Linear Log Map (MAX*)
    - Non Linear Dynamics extrinsic factorization
    - Programmable number of iterations
    - Multiple stop conditions: CRC check, hard output compare and a-posteriori quality indication
    - SIMD type of operation utilizing high level of hardware parallelism to provide high throughput and low latency channel decoding capabilities
  - Turbo encoding for WiMAX OFDMA, 3GLTE DL/UL-SCH and UMTS systems using DEPE module:
    - Information bits encoding and rate matching up to 1.8 Gbps for 3GLTE and WiMAX
    - Code block CRC attachment and filler bits insertion for 3GLTE
    - Bit randomization for WiMAX
    - Transport block CRC attachment in 3GLTE in case of single code block.
    - Information bits encoding and rate matching up to 900 Mbps for UMTS

- HS-DSCH and E-DCH (TDD and FDD) Turbo encoding and rate matching.
- CRC attachment for Transport Block ≤ 5090.
- Optional bit scrambling for Transport Block ≤ 5090 (FDD only).
- Transport Block generation assist in system memory using bit write granularity
- Transport Block segmentation assist using bit read granularity.

— Viterbi decoding for various technologies using eTVPE[1] module:
- Supports K =5,7,9
- Fully programmable polynomials
- Various rates/puncturing cases

— DFT/iDFT and FFT/iFFT processing using three eFTPE modules:
- Variable length FFT/iFFT processing of 128, 256, 512, 1024, 1536 and 2048 points.
- Variable length DFT/iDFT processing of the form, up to 1200 points: 12, 24, 36, 48, 60, 72, 96, 108, 120, 144, 180, 192, 216, 240, 288, 300, 324, 360, 384, 432, 480, 540, 576, 600, 648, 720, 768, 864, 900, 960, 972, 1080, 1152 and 1200 points
- Variable input data size, supporting 16 bit {8I,8Q} or 32 bit {16I,16Q}
- Programmable guard band insertion and removal for iFFT and FFT processing.
- Programmable Cyclic Prefix insertion and removal.
- Pre-Multiplication (“array multiplication”) support by programmable complex values vector.
- Post-Multiplication support of all samples by programmable complex values vector.
- Phase rotation of input samples.
- Input data complex conjugate and re-ordering (1 to N samples reversed to N to 1)
- Zero padding of input data
- UMTS scrambled pilot samples generation in frequency domain
- Programmable scaling method, supporting one of the following methods:
- Automatic adaptive scaling using overflow detection between transform stages, and optional programmable overall scaling factor for the output data
- User defined scaling between transform stages
- Automatic or programmable input scale up for input data with small values, to increase calculation precision.

— CRC check and insertion using CRCPE:
- CRC check & report for UL processing
- CRC insertion for DL processing
- Up to 10 Gbps, supporting the following polynomials:
  - CRC24 with polynomial $D^{24} + D^{23} + D^6 + D^5 + D + 1$
  - CRC24 with polynomial $D^{24} + D^{23} + D^{18} + D^{17} + D^{14} + D^{11} + D^{10} + D^7 + D^6 + D^5 + D^4 + D^3 + D + 1$
  - CRC16 with polynomial $D^{16} + D^{12} + D^5 + 1$
  - CRC16 with polynomial $D^{16} + D^{15} + D^2 + 1$
  - CRC32 with polynomial $D^{32} + D^{26} + D^{23} + D^{22} + D^{16} + D^{12} + D^{11} + D^{10} + D^8 + D^7 + D^5 + D^4 + D^2 + D + 1$

1.Viterbi and Turbo decoding share memories and share throughput; 100% throughput of Viterbi and 100% throughput of Turbo cannot be achieved simultaneously.

- CRC18 with polynomial $D^{18} + D^{17} + D^{14} + D^{13} + D^{11} + D^{10} + D^8 + D^7 + D^6 + D^3 + D^2 + 1$
- CRC12 with polynomial $D^{12} + D^{11} + D^{10} + D^8 + D^5 + D^4 + 1$
- CRC6 with polynomial $D^6 + D^5 + D^3 + D^2 + D + 1$

— MMSE (Minimum Mean Square Error) / ZF (Zero Forcing)/ IRC (Interference Rejection Combining) Equalization
  – Estimation of signal by MMSE/ZF/IRC equalizer using following inputs:
  – observations, channel estimation, noise and transmitted layers covariance matrices and previously detected layer (for cancellation)
  – Inputs precision 32 bit {16I,16Q} with block floating point 8 bit scaling factor.
  – Supporting various Rx Antenna (1,2,4,8) and MIMO layers (1,2,3,4) configurations
  – Optional Channel Estimation interpolation with user defined weights.
  – Embedded support for advanced receivers with iterative interference cancellation schemes with internal single layer cancellation, rank reduction, layer discarding and MIMO layers covariance matrix.
  – Optional support for full noise & interference covariance matrix, with variable granularity, up to different matrix per sub-carrier (RE).
  – Flexible output format supporting 32 bit {16I,16Q} with optional block floating point representation using 8 bit scaling factor per element or per group of elements.
— Maximum Likelihood estimation implemented with QRD-M tree search
  – Estimation of signal by QRD-M equalizer using following inputs:
  – observations, channel estimation, noise variance.
  – Supporting various Rx Antenna (1,2,4,8) and MIMO layers (1,2,3,4) configurations.
  – Optional Channel Estimation interpolation with user defined weights.
  – Configurable search width, with M up to 64, providing performance-latency trade-off.
  – LLR output generation.
— Matrix Inversion
  – Support for up to 4×4 matrix inversion.
  – Programming model optimized for batch job of multiple matrix inversions.
  – High precision floating-point arithmetic
  – Input samples are received in 32 bit {16I,16Q} block floating point (BLF) with 8-bit scale factor.
  – Internal calculations performed using custom floating-point (FLP) format: 40 bit {20I,20Q} mantissa and 8-bit exponent.
— Downlink Chip Rate Processing:
  – Capacity of up to 512 Physical Channels including MIMO, STTD, TSTD and Closed Loop Mode 1 operation per channel.
  – Input data precision of 16 bit {8I,8Q} complex symbols.
  – Spreading with SF 4,8,16,32,64,128, and 256 using internally generated channelization codes.
  – Scrambling using internally generated, up to 32 independent codes, including support for compressed mode codes.
  – Supporting SF 1 special channels with spreading, scrambling bypass

- Programmable complex gains per Physical Channel, with differentiation between data and control information, supporting various slot formats.
- Physical channels combining and flexible assignment to up to 16 virtual antenna's.
- Optional Beam Forming operation on combined Physical Channels.
- Output data precision of 32 bit {16I,16Q} complex chips.

— Uplink Batch Processing - for data and control channels with variable spreading factors
- Capacity of up to 384 Physical Channels with up to 2144 total fingers from up to 24 antenna streams with max 512 chips delay spread.
- Optional pre-de-spreading support with up to 80 Physical Channels with SF 4
- Input data precision of 16 bit {8I,8Q} complex chips.
- Optional Internal interpolation of x2 oversampled input stream, up to x16 resolution using programmable 8 tap polyphase filter.
- Despreading with SF 2,4,8,16,32,64,128,256 using internally generated channelization codes.
- Descrambling by short or long codes, with up to 384 different, internally generated, scrambling codes.
- Optional fingers combining using programmable weights.
- Optional frequency correction functionality using programmable correction factor.
- Multiple output formats:
  - 16 bit fixed point or custom 22 bit (16-bit mantissa and 6-bit exponent) floating point formats for fingers combining option.
  - complex 32 bit {16I,16Q} for fingers combining bypass option.

— Uplink Fast Processing - for (E)DPCCH processing
- Capacity of up to 400 Physical channels with up to 3200 total fingers from up to 24 antenna streams.
- Input data precision of 16 bit {8I,8Q} complex chips.
- Optional Internal interpolation of x2 oversampled input stream, up to x16 resolution using programmable 8 tap polyphase filter.
- Descrambling by short or long codes with internally generated scrambling codes.
- Despreading using SF 256 for DPCCH and E-DPCCH channels.
- Optional correlation with pilot sequence.
- Programmable slot format and early/on-time/late processing for various fields of control channels.
- Output 16 bit I and 16 bit Q.
- Internal commands FIFO for flexible updates of fingers and channels association.
- Latency of 68 chips including processing and write back of results to system memory

— PN code generator
- Short or Long codes generation based on programmable init values
- Generates scrambling code or scrambling code multiplied by Hadamard code with programmable spreading factor and OVSF.
- Two output formats:
- 16 bit {8I,8Q} format, with throughput of up to 4 Gsamples/s
- 2 bit {1I, 1Q} format, with throughput of up to 32 Gsamples/s
- Easily initialized and configured with minimal intervention:
- Software-friendly buffer descriptor handshake mechanism and task assignment

  - Externally accessible memories and registers for debug purposes
  - Internal, high throughput, DMA capabilities to fetch the input data and output the results to system memory
  - Internal memory used for all module processing
- Multi-core support:
  - Multiple configurable descriptor rings with support for high and low priority tasks
- System notification:
  - Can generate RapidIO doorbells or interrupts on task completion
- Programmable customization including processing management and scheduling:
  - Second Generation of Programmable System Interface (PSIF2)

- DDR Controller supporting:
  - Up to 667 MHz clock rate (1333 MHz data rate).
  - Supports DDR3 devices
  - Programmable timing
  - Support for a 64-bit data interface (72 bits including ECC), up to 1333 MHz data rate
  - Support for a 32-bit data interface (40 bits including ECC), up to 1333 MHz data rate
  - Full ECC support for single-bit error correction and multi-bit error detection up to the maximum specified data rates
  - Two banks of memory via two chip selects. Each chip select supports up to 2 Gbytes, but memory total cannot exceed 2 Gbytes.
  - DRAM chip configurations from 64 Mbits to 4 Gbits with x8/x16 data ports
  - Supports the following burst lengths:
    - 4 beat burst (fixed)
    - On the Fly
    - 8 beat burst (fixed)
  - Sleep mode support for self-refresh SDRAM
  - On-die termination support
  - Supports auto refreshing
  - Support for SODIMMs
- High-Speed Serial Interface (HSSI)
  - Ten multiplexed SerDes lanes
  - Serial RapidIO Subsystem
    - Two Serial RapidIO ports supporting x1/x2/x4 operation up to 5 Gbaud with a RapidIO enhanced messaging unit (eMSG) and two RapidIO DMA units.
    - Each x1/x2/x4 Serial RapidIO endpoint operates at 1.25/2.5/3.125/5 Gbaud and complies with the following parts of Specification 2.1 of the RapidIO trade association interconnect specification:
      - Part I (input and output logical specifications)
      - Part II (message passing logical specification)
      - Part III (common transport specification)
      - Part VI (physical layer 1x LP-serial specification)
      - Part VIII (error management extension specification)

- Each Serial RapidIO port supports read, write, messages, doorbells, data streaming and maintenance accesses:
  - Small and large transport information field only
  - All priorities flow
  - Pass-through between the two ports that allows cascading devices using the Serial RapidIO and enabling message/data path between the two Serial RapidIO ports without core intervention. A message/data that is not designated for the specific device passes through it to the next device.
- RapidIO Enhanced Messaging Unit supports:
  - RapidIO Interconnect Specification 1.3, Part 2: Message Passing Logical Specification.
  - RapidIO Interconnect Specification 1.3, Part 10: Data Streaming Logical Specification.
  - RapidIO Interconnect Specification 2.1, Part 10: Stream Management Flow Control. Basic stream management flow control (XON/XOFF) using extended header message format.
  - 64 outbound queues allowing multi-core environment.
  - 16 concurrent inbound reassembly operations. One additional reserved reassembly for inbound unit 0 to carry session management protocol.
  - Multi unicast.
- Each RapidIO DMA unit supports:
  - Four high-speed/high-bandwidth channels accessible by local and remote masters
  - Basic DMA operation modes (direct, simple chaining)
  - Extended DMA operation modes (advanced chaining and stride capability)
  - Programmable bandwidth control between channels
  - Up to 256 bytes for DMA sub-block transfers to maximize performance over the RapidIO interface
  - Three priority levels supported for source and destination transactions

— Common Public Radio Interface (CPRI) Controller
- Supports v4.1 of the CPRI standard
- Up to 6 lanes
- Supports 1.2288 Gbaud, 2.4576 Gbaud, 3.072 Gbaud, 4.9152 Gbaud and 6.144 Gbaud
- Supports scrambling
- Daisy-chain capability that allows cascading devices according to pre-determined user configuration. Chaining can be done for each lane using the CPRI controller. Chaining lanes does not require core intervention or internal device bandwidth overhead.
- Input power can be disabled for system power reduction if CPRI is not required.

— PCI-Express Controller
- Complies with the *PCI Express™ Base Specification, Revision 2.0*
- Supports root complex (RC) and endpoint (EP) configurations
- 32- and 64-bit address support
- x4, x2, and x1 link support
- Supports 2.5 Gbaud, 5.0 Gbaud.
- Supports accesses to all PCI Express memory and I/O address spaces (requestor only)

  - Supports posting of processor-to-PCI Express and PCI Express-to-memory write
  - Supports strong and relaxed transaction ordering rules
  - PCI Express configuration registers (type 0 in EP mode, type 1 in RC mode)
  - Baseline and advanced error reporting support
  - One virtual channel (VC0)
  - 256-byte maximum payload size (MAX_PAYLOAD_SIZE)
  - Supports three inbound general-purpose translation windows and one configuration window
  - Supports four outbound translation windows and one default window
  - Supports eight non-posted and four posted PCI Express transactions
  - Supports up to six priority 0 internal platform reads and eight priority 0 to 2 internal platform writes. (The maximum number of outstanding transactions at any given time is eight.)
  - Credit-based flow control management
  - Supports PCI Express messages and interrupts

- DMA Controller
  - 32 unidirectional channels, providing up to 16 memory-to-memory channels.
  - Buffer descriptor programing model.
  - Up to 1024 buffer descriptors per channel direction provide a total of 32 Kbyte buffer descriptors. Buffer descriptors can reside in M2, M3 or DDR memory.
  - Priority-based time-multiplexing between channels, using four internal priority groups with round-robin arbitration between channels on equal priority group.
  - Earliest deadline first (EDF) priority scheme that assures task completion on time.
  - Flexible channel configuration with all channels supporting all features.
  - A flexible buffer configuration, including:
    - Simple buffers
    - Cyclic buffers
    - Single address buffers (I/O device).
    - Incremental address buffers
    - Chained buffers
    - 1D to 4D buffers, optimized for video applications
    - 1D or 2–4D complex buffers, a combination of buffer types
  - Two external DMA request (DREQ) and two $\overline{\text{DONE}}$ signal lines that allow an external device to trigger DMA transfers.
  - High bandwidth
  - Optimized for DDR SDRAM
- The QUICC Engine subsystem includes dual RISC processors and 48-Kbyte multi-master RAM to handle the Ethernet and SPI interfaces, thus off loading the tasks from the cores. The three communication controllers support:
  - Two Ethernet controllers supporting Gigabit operation
  - SPI controller
- Ethernet Controllers
  - Two Ethernet physical interfaces, each of which supports:
    - 1000 Mbps SGMII protocol using a 4-pin SerDes interface
    - 1000 Mbps RGMII protocol

  - MAC-to-MAC connection in all modes
  - Full-duplex operations
  - Full-duplex flow control feature (**IEEE** Std. 802.3x™)
  - Receive flow control frames
  - Detection of all erroneous frames as defined by **IEEE** Std. 802.3®-2002
  - Multi-buffer data structure
  - Diagnostic modes: Internal and external loopback mode and echo mode
  - Serial management interface MDC/MDIO
  - Transmitter network management and diagnostics
  - Receiver network management and diagnostics
  - VLAN Support
  - **IEEE** Std. 802.1p/Q™ QoS
  - Eight Tx/Rx queues
  - Queuing decision for IP/MAC/UDP filtering based on MAC destination addresses, IP destination address, and UDP destination port
  - Programmable maximum frame length
  - Enhanced MIB statistics
  - Optional shift of data buffer by two bytes for L3 header alignments
  - Extended features
    - IP header checksum verification and calculation
    - Parsing of frame headers and adding a frame control block at the frame head, containing L3 and L4 information for CPU acceleration
- Serial peripheral interface (SPI)
  - Four-signal interface (SPIMOSI, SPIMISO, SPICLK and SPISEL)
  - Full-duplex operation
  - Works with 32-bit data characters, or with a range from 4-bit to 16-bit data characters
  - Supports back-to-back character transmission and reception
  - Supports master or slave SPI mode
  - Supports multiple-master environment
  - Continuous transfer mode for automatic scanning of a peripheral
  - Maximum clock rate is (QUICC Engine clock)/8 in master mode and (QUICC Engine clock)/4 in slave mode (not in back-to-back operation)
  - Independent programmable baud rate generator
  - Programmable clock phase and polarity
  - Local loopback capability for testing
  - Open-drain outputs support multimaster configuration
  - Communication with Ethernet PHY for configuration and status (MIIMCOM-MII management communication protocol)
  - Multi-MIIMCOM environment with up to 32 PHYs
  - Programmable clock gap between two characters in master mode
  - Controlled by the DSP cores and the QUICC Engine RISC processors according to user configuration.
- I/O Interrupt Concentrator consolidates all chip maskable interrupt and non-maskable interrupt sources and routes them to $\overline{\text{INT\_OUT}}$, $\overline{\text{NMI\_OUT}}$, and the cores.

- UART
  - Bit rate up to 6.25 Mbps
  - Two signals for transmit data and receive data
  - Full-duplex operation
  - Standard mark/space non-return-to-zero (NRZ) format
  - 13-bit baud rate selection
  - Programmable 8-bit or 9-bit data format
  - Separately enabled transmitter and receiver
  - Programmable transmitter output polarity
  - Separate receiver and transmitter interrupt requests
  - Receiver framing error detection
  - Hardware parity checking
  - 1/16 bit-time noise detection
  - Single-wire and loop operations
- Timers
  - Two general-purpose 32-bit timers for RTOS support per SC3850 core
  - Four TMR modules, each with four 16-bit timers; cascadable timers; count up/down; programmable count modulo; count once or repeatedly; counters are preloadable; compare registers can be preloaded; counters can share available inputs; separate prescaler for each counter; each counter has capture and compare capability; any of the following clock sources: system clock or external clock input
  - Two TIMER_32B modules, each with four 32-bit timers; cascadable timers; count up/down; programmable count modulo; count once or repeatedly; counters are preloadable; compare registers can be preloaded; counters can share available inputs; separate prescaler for each counter; each counter has capture and compare capability; any of the following clock sources: system clock or external clock input.
  - Eight software watchdog timer (SWT) modules
- Eight programmable hardware semaphores, locked by simple write access without need for read-modify-write operation by the DSP core.
- Virtual interrupts
  - Generation of 32 virtual interrupts by a simple write access
  - Generation of virtual $\overline{\text{NMI}}$ by a simple write access
- I^2C interface
  - Two-wire interface
  - Multi-master operational
  - Calling address identification interrupt
  - START and STOP signal generation/detection
  - Acknowledge bit generation/detection
  - Bus busy detection
  - Programmable clock frequency
  - On-chip filtering for spikes on the bus
- General-purpose input/output (GPIO) ports:
  - 32 GPIO ports
  - Each GPIO port can either serve the on-device peripherals or act as a programmable I/O pin

  - Sixteen GPIO pins can be configured as external interrupt inputs
  - All ports are bidirectional
  - All ports are set as GPIO inputs at system reset
  - All port values can be read while the pin is connected to an internal peripheral
  - All ports have open-drain output capability
- Boot interface options:
  - Ethernet
  - Serial RapidIO interface
  - I^2C
  - SPI
- JTAG. Test Access Port (TAP) and Boundary Scan Architecture designed to comply with **IEEE** Std. 1149.6™.
- Reduced power dissipation
  - Very low power CMOS design
  - Low-power standby modes
  - Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)
- Technology: The MSC8157 device is manufactured using CMOS 45 nm SOI technology.
- Flip Chip-Plastic Ball Grid Array (FC-PBGA), 783-ball, 1 mm pitch, 29 mm × 29 mm

2 Developer Environment

Freescale supplies a complete set of DSP development tools for the MSC8157 device. The tools provide easier and more robust ways for designers to develop optimized DSP systems. Whether the application targets a 3G-LTE, WCDMA/HSPA, or WiMAX system, the development environment gives the designers everything they need to exploit the advanced capabilities of the MSC8157 architecture.

2.1 Tools

The MSC8157 tool components include the following:

- *Eclipse Integrated development environment (IDE).* Easy-to-use graphical user interface and project manager for configuring and managing multiple build configurations.
- *C and C++ compiler with in-line assembly.* The developer can generate highly optimized DSP code by exploiting the StarCore multiple-ALU architecture, with parallel fetch sets and high code density.
- *Librarian.* The developer can create application-specific DSP libraries for modularity.
- *Linker.* The developer can efficiently produce executables from object code and partition memory according to the application architecture; the linker supports code overlay.
- *Multi-Core Debugger.* Seamlessly integrated real-time, non-intrusive, multi-mode, multi-core, and multi-DSP debugger handles highly optimized DSP algorithms. The developer can choose to debug in source code, assembly code, or mixed mode. Supports RTOS-aware debugger.
- *Royalty-free RTOS.* Included with package and includes a graphical user interface (GUI) called Kernel Aware that shows task information, interrupts, and other processing elements.

- *Software Simulator*. Full chip simulation (FCS) that allows the developer to design an application and run it on the simulator before running it on the silicon. FCS is integrated under integrator developer environment (IDE), the simulator provides customers with tools to create projects and debug them as they would on silicon (high speed simultaneous transfers). In addition, there is an SC3850 subsystem performance accurate (PACC) simulator that is approximately 95% cycle accurate.
- *Profiler*. The developer can analyze and identify program design inefficiencies.
- *High Speed Run Control*. USB TAP high speed host-target interface allows users to program in Flash memory, ROM, and cache.
- *Host Platform Support*. Microsoft Windows and Solaris.
- *Development Board*. The application development system (ADS).
- *Kit for MSC8157*. A complete system for developing/debugging real-time hardware and software.

2.2 Application Software

Freescale offers a broad range of DSP applications through its third-party application software partners. Applications and software modules are listed in **Table 1**.

Table 1. Application Software Modules

Application	Modules
Baseband	3G-LTE evolving kernels library.
	Optimized FFT kernels, MMSE, QR Decomposition and other matrix multiplication operations.
	WCDMA including symbol rate and chiprate library.
	WiMAX solution supporting Wave 1 features with future extension to Wave 2 and beyond.
Device Drivers and Example Code	MAPLE-B2 driver, DMA driver, Serial RapidIO driver, PCI-Express, CPRI, Ethernet driver, UART driver, memory allocation, and interrupt handling.
StarCore Libraries	Rich set of StarCore software libraries, including: Math (Part 1 and 2), Signal, Complex vector, Control function, Frequency domain, Filter, Common, Image Processing, Communication, and Matrix.

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