

MC13850 Evaluation Board Quick Start — 1960 MHz

INTRODUCTION

This evaluation board design demonstrates one possible design at 2.75 V and 5 and 10 mA that satisfies competing requirements for NF, IP3, gain, return losses and current consumption with unconditional stability. By changing any of the requirements, the performance for a particular parameter can be improved to meet a particular spec requirement.

This circuit was designed to provide NF of 1.8 dB, S21 gain of 15 dB, OIP3 of 24 dBm at 1960 MHz in High IP3 mode.

OIP3 > 19 dBm is preserved in bypass mode for high input signal conditions when the LNA is bypassed to lower gain and current draw.

Return losses are also preserved in bypass mode for excellent matching

The MC13850 is a general purpose Low Noise Amplifier in a MLP 2x2x0.6 mm package using Freescale's advanced RF SiGe BiCMOS process.

The LNA is bias stabilized for variations in device and temperature.

NOTE: Tables 1 and 2 list measured parameters on three typical evaluation boards and are meant as a guide to the RF performance possible for this application circuit. Variations in matching component performance may result in variation in evaluation board performance results.

Table 1. Evaluation Board Measurements (1960 MHz, $V_{CC} = 2.75$ V, Frequency Spacing = 200 kHz)

Serial #	IP3 Mode	Input Power (dBm)	Output Power (dBm)	Power Gain (dB)	Output IP3 (dBm)	Input IP3 (dBm)	Output P _{1dB} (dBm)	Input P _{1dB} (dBm)	NF (dB)	DC I _{CC} (mA)
1	Lo	-30	-14.97	15.03	23.33	8.3	3.8	-11	1.55	5.11
1	Hi	-30	-15.01	14.99	24.49	9.5	3.8	-11	1.80	11.06
1	Byp	-30	-33.6	-3.6	20.2	23.8	—	—	3.01	4.1 nA
1	Standby	-30	-44.76	-14.76	—	—	—	—	—	3.4 nA
2	Lo	-30	-15.09	14.91	20.81	5.9	2.9	-12	1.47	4.55
2	Hi	-30	-15.04	14.96	25.06	10.1	3.4	-12	1.79	9.76
2	Byp	-30	-33.6	-3.6	20	23.6	—	—	3.46	4.56 nA
2	Standby	-30	-44.47	-14.47	—	—	—	—	—	4.5 nA
3	Lo	-30	-15.19	14.81	19.66	4.85	3.8	-11	1.52	4.34
3	Hi	-30	-15.26	14.74	24.71	9.97	4.7	-10	1.77	9.15
3	Byp	-30	-33.86	-3.86	19.74	23.6	—	—	3.55	5.29 nA
3	Standby	-30	-45.5	-15.5	—	—	—	—	—	5.6 nA

Table 2. S-Parameters (1960 MHz, $V_{CC} = 2.75$ V)

Serial #	IP3 Mode	S11 (dB)	S21 (dB)	S12 (dB)	S22 (dB)
1	Lo	-12.52	15.13	-21.08	-14.81
1	Hi	-12.62	15.02	-22.47	-15.9
1	Byp	-9.56	-3.8	-3.9	-7.3
1	Standby	-2.27	-15.9	-15.4	-2.22
2	Lo	-11.76	14.96	-20.87	-14.32
2	Hi	-12.27	14.93	-22.49	-15.86
2	Byp	-9.97	-3.7	-3.8	-7.62
2	Standby	-2.37	-15.6	-15.2	-2.24
3	Lo	-13.57	14.9	-21.0	-10.91
3	Hi	-14.44	15.0	-22.6	-12.91
3	Byp	-10.02	-3.9	-4.1	-7.26
3	Standby	-2.25	-16.6	-16.2	-1.98

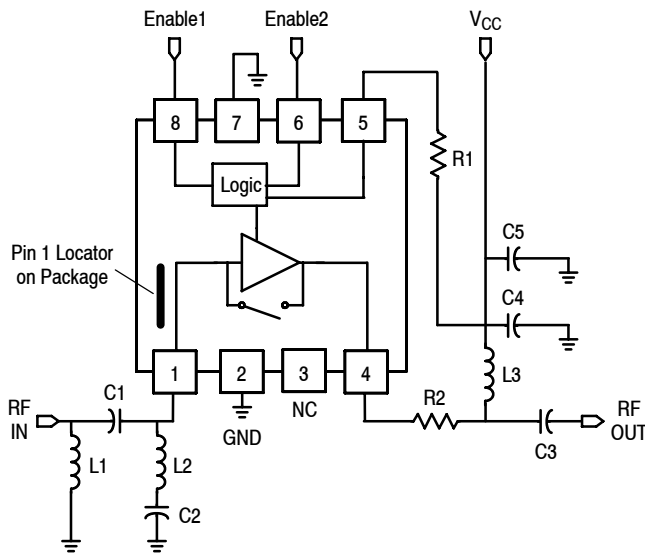


Figure 1. MC13850 1960 MHz Schematic

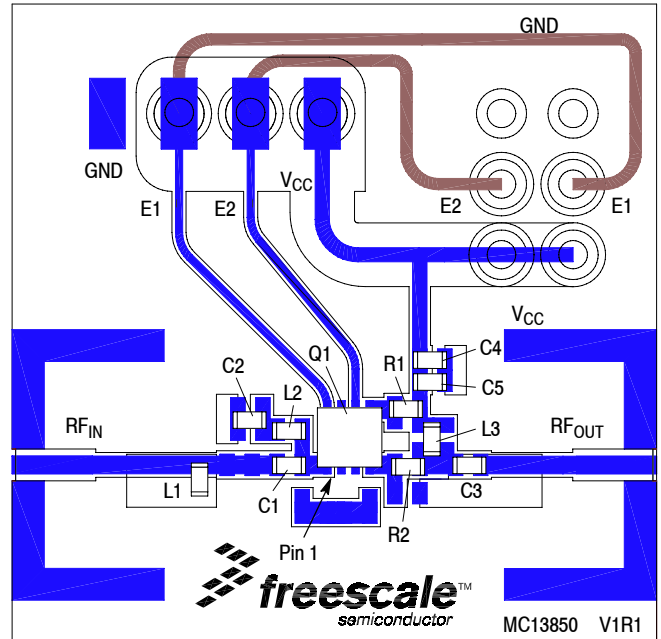


Figure 2. MC13850 1960 MHz Evaluation Circuit Component Layout

Table 3. Evaluation Circuit Component Designations and Values

Component	Value	Case	Manufacturer	Comments
C1	27 pF	402	Murata	DC Block, Input match
C2	0.1 μ F	402	Murata	DC Block
C3	27 pF	402	Murata	DC Block, Output match
C4	33 pF	402	Murata	1960 MHz short
C5	0.1 μ F	402	Murata	Low freq bypass
L1	33 nH	402	Murata	Input match
L2	3.3 nH	402	Murata	Input match
L3	2.7 nH	402	Murata	Output match, bias decouple
R1	330 Ω	402	KOA	Bias feed to logic
R2	5 Ω	402	KOA	Lower gain, increase stability
Q1	MC13850	MLP 2x2	Freescale	SiGe LNA

Table 4. Truth Table

Enable Pins	Low IP3	High IP3	Bypass	Standby
E1	1	1	0	0
E2	1	0	1	0
Current Draw	5 mA	10 mA	<20 μ A	<20 μ A

The board can be biased using only the V_{CC} and GND pins. The jumpers can be moved for the different modes of operation.

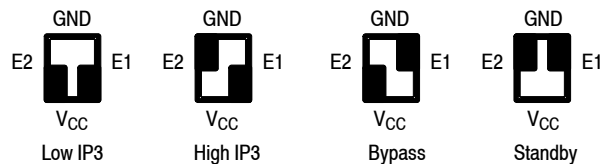


Figure 3. Jumper Positions

There are four modes of operation, Low IP3, High IP3 with higher current drain and higher IP3, bypass and standby.

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Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
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