

# MC13850 Evaluation Board Quick Start — 470–860 MHz

## INTRODUCTION

This evaluation board design demonstrates one possible design at 2.75 V and 5 and 10 mA that satisfies competing requirements for NF, IP3, gain, return losses and current consumption with unconditional stability. By changing any of the requirements, the performance for a particular parameter can be improved to meet a particular spec requirement.

This design uses the same broadband match for 470–860 MHz for UHF and ISM applications.

This circuit was designed to provide NF < 1.4 dB, S21 gain > 24 dB, OIP3 of 16 dBm at 470 MHz in High IP3 mode.

This circuit was also designed to provide NF < 1.4 dB, S21 gain > 19 dB, OIP3 of 17 dBm at 860 MHz in High IP3 mode.

OIP3 > 18 dBm is preserved in bypass mode for high input signal conditions when the LNA is bypassed to lower gain and current draw.

Return losses are also preserved in bypass mode for excellent matching.

The MC13850 is a general purpose Low Noise Amplifier in a MLPD 2x2 mm package and uses Freescale's advanced RF SiGe BiCMOS process.

The LNA is bias stabilized for variations in device and temperature.

NOTE: Tables 1 and 2 list measured parameters on three typical evaluation boards and are meant as a guide to the RF performance possible for this application circuit. Variations in matching component performance may result in variation in evaluation board performance results.

**Table 1. Evaluation Board Measurements** (470–860 MHz, V<sub>CC</sub> = 2.75 V, Frequency Spacing = 200 kHz)

Serial #	IP3 Mode	f (MHz)	Input Power (dBm)	Output Power (dBm)	Power Gain (dB)	Output IP3 (dBm)	Input IP3 (dBm)	Output P <sub>1dB</sub> (dBm)	Input P <sub>1dB</sub> (dBm)	NF (dB)	DC I <sub>CC</sub> (mA)
1	High	470	-30	-5.64	24.36	16.36	-8	9.9	-14.5	1.26	8.73
1	High	860	-30	-10.93	19.07	17.87	-1.2	9.6	-9.5	1.27	8.73
1	Low	470	-30	-8.67	21.33	10.03	-11.3	6.8	-14.5	1.34	4.23
1	Low	860	-30	-12.61	17.39	13.09	-4.3	8.6	-8.8	1.2	4.23
1	Bypass	470	-30	-37.04	-7.04	20.66	27.7	—	—	9.5	0.37 μA
1	Bypass	860	-30	-36.3	-6.3	18.5	24.8	—	—	5.2	0.37 μA
1	Standby	470	-30	-58.65	-28.65	—	—	—	—	—	0.023 μA
1	Standby	860	-30	-54.41	-24.41	—	—	—	—	—	0.023 μA
2	High	470	-30	-5.57	24.43	16.33	-8.1	9.5	-14.9	1.37	8.51
2	High	860	-30	-11.05	18.95	17.76	-1.19	9.2	-9.8	1.34	8.51
2	Low	470	-30	-8.33	21.67	10.47	-11.2	7.0	-14.7	1.42	4.31
2	Low	860	-30	-12.63	17.37	13.27	-4.1	8.6	-8.8	1.24	4.31
2	Bypass	470	-30	-36.86	-6.86	20.74	27.6	—	—	9.4	1.2 μA
2	Bypass	860	-30	-36.28	-6.28	18.42	24.7	—	—	5.2	1.2 μA
2	Standby	470	-30	-58.33	-28.33	—	—	—	—	—	0.03 μA
2	Standby	860	-30	-54.41	-24.41	—	—	—	—	—	0.03 μA
3	High	470	-30	-5.58	24.42	16.42	-8	9.4	-15.0	1.36	9.09
3	High	860	-30	-11.08	18.92	17.87	-1.05	8.9	-10.0	1.35	9.09
3	Low	470	-30	-8.29	21.71	10.71	-11	7.4	-14.3	1.22	4.56
3	Low	860	-30	-12.55	17.45	13.9	-3.55	8.3	-9.2	1.23	4.56
3	Bypass	470	-30	-36.92	-6.92	20.91	27.83	—	—	9.5	0.12 μA
3	Bypass	860	-30	-36.18	-6.18	18.62	24.8	—	—	5.2	0.12 μA
3	Standby	470	-30	-58.56	-28.56	—	—	—	—	—	0.16 μA
3	Standby	860	-30	-54.33	-24.33	—	—	—	—	—	0.16 μA

**Table 2. S-Parameters** (470-860 MHz,  $V_{CC} = 2.75$  V)

Serial #	f (MHz)	IP3 Mode	S11 (dB)	S21 (dB)	S12 (dB)	S22 (dB)
1	High	470	-9.90	24.10	-30.4	-10.24
1	High	860	-22.20	19.50	-29.0	-7.32
1	Low	470	-4.87	21.4	-25	-6.56
1	Low	860	-13.1	17.9	-26.2	-5.34
1	Bypass	470	-4.17	-6.76	-6.79	-11.67
1	Bypass	860	-5.82	-5.84	-5.7	-8.29
1	Standby	470	-0.82	-28.05	-27.79	-3.11
1	Standby	860	-0.947	-23.67	-23.44	-2.24
2	High	470	-10.72	24.17	-30.7	-10.16
2	High	860	-21.51	19.44	-29.2	-7.10
2	Low	470	-5.3	21.60	-28.4	-6.56
2	Low	860	-13.4	17.94	-27.2	-5.25
2	Bypass	470	-4.09	-6.67	-6.7	-11.87
2	Bypass	860	-6.01	-5.82	-5.71	-8.1
2	Standby	470	-0.83	-27.7	-27.53	-3.19
2	Standby	860	-0.99	-23.57	-23.48	-2.17
3	High	470	-11.18	24.14	-30.77	-10.27
3	High	860	-20.23	19.41	-29.29	-7.24
3	Low	470	-5.6	21.72	-28.67	-6.69
3	Low	860	-14.61	18.0	-27.3	-5.38
3	Bypass	470	-4.29	-6.69	-6.74	-11.72
3	Bypass	860	-6.24	-5.77	-5.65	-8.16
3	Standby	470	-0.87	-28.10	-27.05	-3.11
3	Standby	860	-1.05	-23.56	-23.47	-2.14

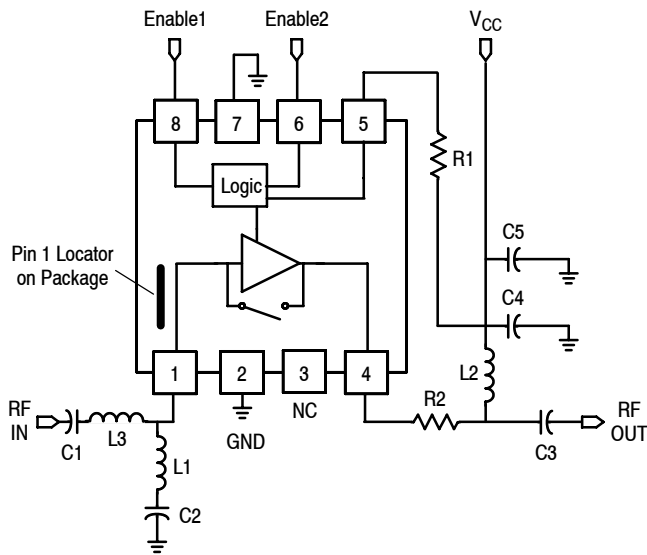


Figure 1. MC13850 470-860 MHz Schematic

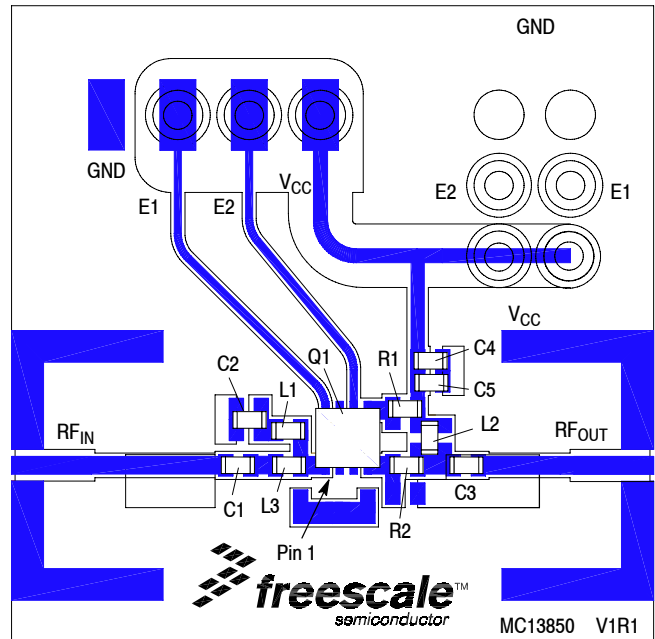


Figure 2. MC13850 470-860 MHz Evaluation Circuit Component Layout

Table 3. Evaluation Circuit Component Designations and Values

Component	Value	Case	Manufacturer	Comments
C1	27 pF	402	Murata	DC Block, Input match
C2	0.1 $\mu$ F	402	Murata	Low freq bypass
C3	5 pF	402	Murata	DC Block, Output match
C4	47 pF	402	Murata	900 MHz short
C5	0.1 $\mu$ F	402	Murata	Low freq bypass
L1	47 nH	402	Murata	Input match
L2	18 nH	402	Murata	Output match, bias decouple
L3	4.3 nH	402	Murata	Input match
R1	330 $\Omega$	402	KOA	Logic circuit bias
R2	51 $\Omega$	402	KOA	Lower gain, improve return losses
Q1	MC13850	MLP 2x2	Freescale	SiGe LNA

Table 4. Truth Table

Enable Pins	Low IP3	High IP3	Bypass	Standby
E1	1	1	0	0
E2	1	0	1	0
Current Draw	5 mA	10 mA	<20 $\mu$ A	<20 $\mu$ A

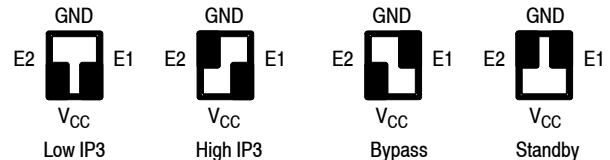


Figure 3. Jumper Positions

The board can be biased using only the  $V_{CC}$  and GND pins. The jumpers can be moved for the different modes of operation.

There are four modes of operation, Low IP3, High IP3 with higher current drain and higher IP3, bypass and standby.

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