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MC13850 Evaluation Board Quick Start — High IP3 900 MHz

INTRODUCTION

This evaluation board design demonstrates one possible design at 2.75 V and 5 and 10 mA that satisfies competing requirements for NF, IP3, gain, return losses and current consumption with unconditional stability. By changing any of the requirements, the performance for a particular parameter can be improved to meet a particular spec requirement.

In addition to this higher IP3 900 MHz design, there is also a 900 MHz design without the feedback capacitance.

This circuit was designed to provide NF < 1.6 dB, S21 gain > 17 dB, OIP3 of 24 dBm at 900 MHz in High IP3 mode.

OIP3 > 23 dBm is preserved in bypass mode for high input signal conditions when the LNA is bypassed to lower gain and current draw.

Return losses are also preserved in bypass mode for excellent matching.

The MC13850 is a general purpose Low Noise Amplifier in a MLP 2x2x0.6 mm package and uses Freescale's advanced RF SiGe BiCMOS process.

The LNA is bias stabilized for variations in device and temperature.

NOTE: Tables 1 and 2 list measured parameters on three typical evaluation boards and are meant as a guide to the RF performance possible for this application circuit. Variations in matching component performance may result in variation in evaluation board performance results.

Table 1. Evaluation Board Measurements (900 MHz, V_{CC} = 2.75 V, Frequency Spacing = 200 kHz)

Serial #	IP3 Mode	Input Power (dBm)	Output Power (dBm)	Power Gain (dB)	Output IP3 (dBm)	Input IP3 (dBm)	Output P_{1dB} (dBm)	Input P_{1dB} (dBm)	NF (dB)	DC I_{CC} (mA)
1	Lo	-30	-13.34	16.66	12.76	-3.9	10.2	-6.5	1.40	4.28
1	Hi	-30	-12.89	17.11	24.91	7.8	13.1	-4.0	1.54	9.09
1	Byp	-30	-34.04	-4.04	24.16	28.2	—	—	4.21	4 nA
1	Standby	-30	-46	-16	—	—	—	—	16.10	4.6 nA
2	Lo	-30	-13.35	16.65	13.55	-3.1	14.2	-2.5	1.46	4.47
2	Hi	-30	-12.71	17.29	25.39	8.1	13.8	-3.5	1.55	9.06
2	Byp	-30	-34.1	-4.1	23.45	27.55	—	—	4.61	1.25 μA
2	Standby	-30	-46.1	-16.1	—	—	—	—	15.40	0.09 μA
3	Lo	-30	-13.79	16.21	14.51	-1.7	13.2	-3.0	1.43	4.83
3	Hi	-30	-12.9	17.1	25.6	8.5	13.6	-3.5	1.58	10.02
3	Byp	-30	-34.6	-4.6	22.9	27.5	—	—	4.95	0.8 μA
3	Standby	-30	-46.1	-16.1	—	—	—	—	16.10	0.5 μA

Table 2. S-Parameters (900 MHz, V_{CC} = 2.75 V)

Serial #	IP3 Mode	S11 (dB)	S21 (dB)	S12 (dB)	S22 (dB)
1	Lo	-10.24	16.9	-19.1	-11.82
1	Hi	-9.71	17.45	-22.3	-13.72
1	Byp	-9.76	-3.82	-3.80	-28.65
1	Standby	-1.25	-15.37	-15.31	-4.81
2	Lo	-13.24	16.61	-19.31	-10.31
2	Hi	-10.93	17.21	-22.33	-12.32
2	Byp	-8.82	-3.97	-3.95	-31.4
2	Standby	-1.23	-15.62	-15.64	-5.34
3	Lo	-13.43	16.54	-19.6	-10.91
3	Hi	-10.51	17.06	-22.8	-12.56
3	Byp	-8.59	-4.05	-4.03	-32.7
3	Standby	-1.24	-15.46	-15.44	-5.54

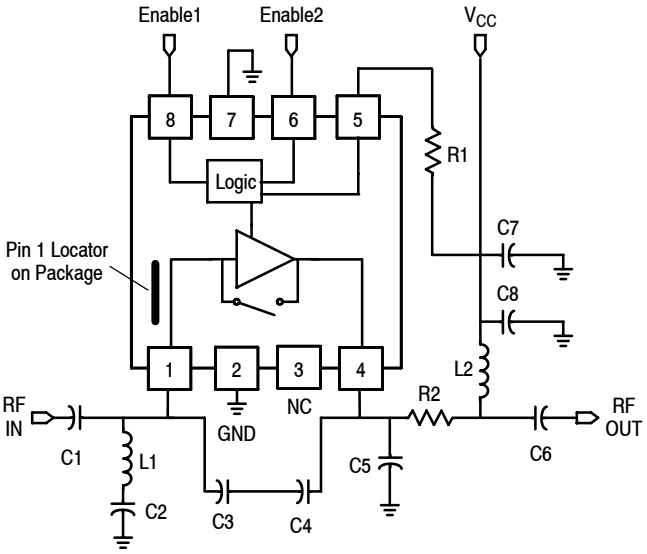

Figure 1. MC13850 900 MHz High IP3 Schematic

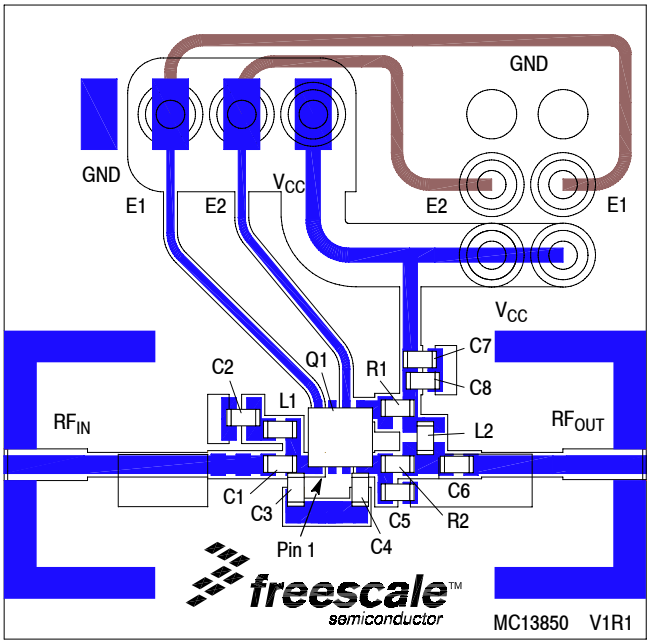

Figure 2. MC13850 900 MHz High IP3 Evaluation Circuit Component Layout

Table 3. Evaluation Circuit Component Designations and Values

Component	Value	Case	Manufacturer	Comments	Impact
C1	100 pF	402	Murata	DC Block, Input match	S11, NF
C2	0.1 μF	402	Murata	DC Block, Input match	
C3	0.5 pF	402	Murata	IP3 improvement	IP3
C4	0.5 pF	402	Murata	IP3 improvement	IP3
C5	1.0 pF	402	Murata	Output match	S22
C6	5.1 pF	402	Murata	Output match	S22, S11
C7	0.1 μF	402	Murata	Bypass	IP3
C8	47 pF	402	Murata	Bypass	IP3
L1	9.1 nH	402	Murata	Input match	S11, gain, NF
L2	5.6 nH	402	Murata	Output match	S22, S11, gain
R1	330 Ω	402	KOA	Bias feed to logic	
R2	10 Ω	402	KOA	Lower gain, increase stability	
Q1	MC13850	MLP 2x2	Freescale	SiGe LNA	

Table 4. Truth Table

Enable Pins	Low IP3	High IP3	Bypass	Standby
E1	1	1	0	0
E2	1	0	1	0
Current Draw	5 mA	10 mA	<20 μA	<20 μA

The board can be biased using only the V_{CC} and GND pins. The jumpers can be moved for the different modes of operation.

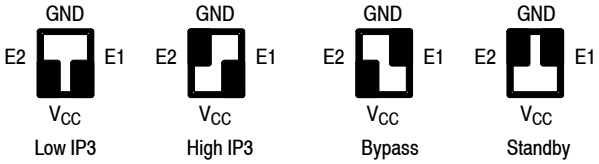

Figure 3. Jumper Positions

There are four modes of operation, Low IP3, High IP3 with higher current drain and higher IP3, bypass and standby.

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