

MC13851 Evaluation Board Quick Start — 1960 MHz

INTRODUCTION

This evaluation board design demonstrates one possible design at 2.75 V that satisfies competing requirements for NF, IP3, gain, return losses and current consumption. By changing any of the requirements, the performance for a particular parameter can be improved to meet a particular spec requirement.

This circuit was designed to provide NF < 1.4 dB, S21 gain > 17.5 dB using R1 = 1.2 kΩ and 1.5 kΩ.

Bias resistor R1 is used to adjust for the desired current drain and IP3 performance.

Gain or NF can be improved with matching changes to meet specific requirements.

Resistor R3 is used to de-Q output inductor L2 and adjust gain and return losses. Lowering the value of R3 lowers gain and improves return losses.

The LNA is bias stabilized for variations in device and temperature.

NOTE: Tables 1 and 2 list measured parameters on three typical evaluation boards and are meant as a guide to the RF performance possible for this application circuit. Variations in matching component performance may result in variation in evaluation board performance results.

Table 1. Evaluation Board Measurements (1960 MHz, V_{CC} = 2.75 V, Frequency Spacing = 200 kHz, Non-Linear Measurements at P_{in} = -30 dBm)

Serial #	R1	Mode	Input Power (dBm)	Output Power (dBm)	Power Gain (dB)	Output IP3 (dBm)	Input IP3 (dBm)	Output Ref P _{1dB} (dBm)	Input Ref P _{1dB} (dBm)	NF (dB)	I _{CC} (mA)
1	1.2k	Active	-30.00	-11.36	18.64	16.24	-2.4	8.64	-10.0	1.4	4.71
1	1.2k	Bypass	-30.00	-34.57	-4.57	20.93	25.5	—	—	4.53	0.88 μA
2	1.2k	Active	-30.00	-11.45	18.55	15.35	-3.2	6.75	-11.8	1.34	5.4
2	1.2k	Bypass	-30.00	-35.72	-5.72	20.28	26	—	—	5.38	38 nA
3	1.2k	Active	-30.00	-11.01	18.99	16.49	-2.5	9.49	-9.5	1.36	4.49
3	1.2k	Bypass	-30.00	-34.59	-4.59	21.41	26	—	—	4.59	0.79 μA
1	1.5k	Active	-30.00	-11.44	18.56	17.46	-1.1	8.56	-10.0	1.36	3.7
1	1.5k	Bypass	-30.00	-34.60	-4.60	20.90	25.5	—	—	4.56	0.88 μA
2	1.5k	Active	-30.00	-11.74	18.26	16.81	-1.45	6.76	-11.5	1.34	4.15
2	1.5k	Bypass	-30.00	-35.72	-5.72	20.28	26	—	—	5.44	38 nA
3	1.5k	Active	-30.00	-11.30	18.70	17.05	-1.65	8.80	-9.9	1.35	3.52
3	1.5k	Bypass	-30.00	-34.60	-4.60	21.40	26	—	—	4.78	0.79 μA

Table 2. S-Parameters (1960 MHz, V_{CC} = 2.75 V)

Serial #	R1	Mode	S11 (dB)	S21 (dB)	S12 (dB)	S22 (dB)
1	1.2k	Active	-12.96	18.49	-24.3	-8.15
1	1.2k	Bypass	-11.87	-4.64	-4.44	-15.77
2	1.2k	Active	-8.13	18.15	-25.7	-26
2	1.2k	Bypass	-10.22	-5.86	-5.54	-11.56
3	1.2k	Active	-10.21	18.69	-24.7	-9.77
3	1.2k	Bypass	-11.62	-4.68	-4.44	-17.15
1	1.5k	Active	-11.3	18.22	-24.4	-7.62
1	1.5k	Bypass	-11.9	-4.72	-4.46	-15.92
2	1.5k	Active	-6.6	17.89	-24.9	-21.56
2	1.5k	Bypass	-10.0	-5.67	-5.34	-11.83
3	1.5k	Active	-8.97	18.42	-24.9	-8.92
3	1.5k	Bypass	-11.81	-4.71	-4.44	-17.21

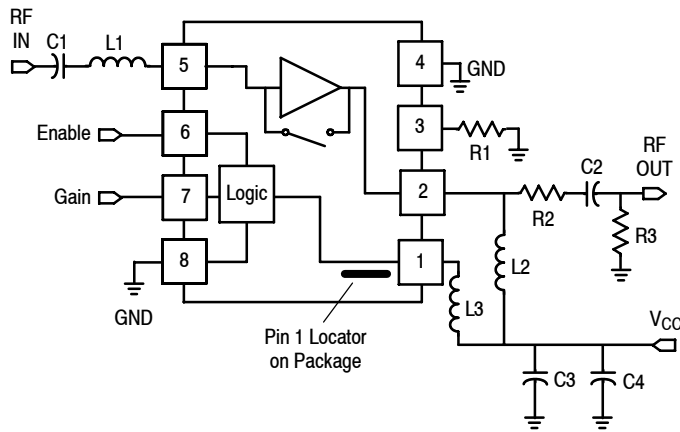


Figure 1. MC13851 1960 MHz Schematic

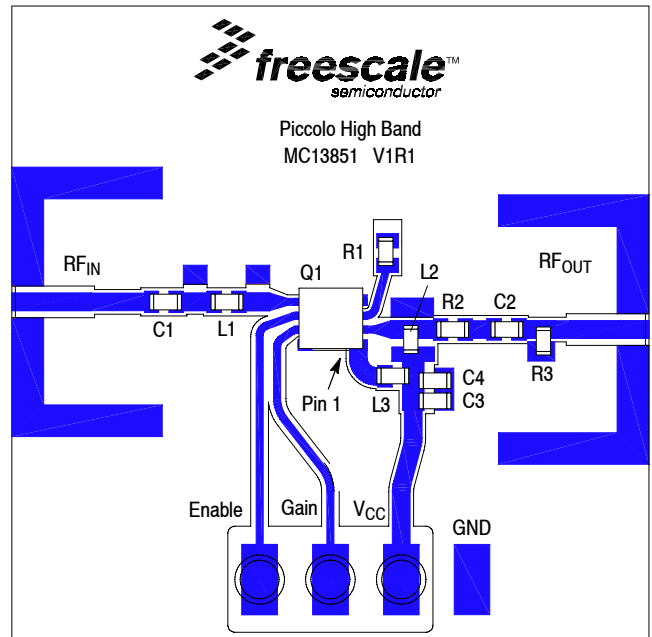


Figure 2. MC13851 1960 MHz Evaluation Circuit Component Layout

Table 3. Evaluation Circuit Component Designations and Values

Component	Value	Case	Manufacturer	Comments
C1	2.4 pF	402	Murata	Input match
C2	0.9 pF	402	Murata	Output match
C3	33 pF	402	Murata	RF bypass
C4	0.01 μ F	805	Murata	Low freq bypass
L1	5.1 nH	402	Murata	Input match
L2	3.3 nH	402	Murata	Output match
L3	270 nH	402	Murata	Bias couple to logic
R1	1.2, 1.5 k Ω	402	KOA	LNA bias
R2	10 Ω	402	KOA	Stability
R3	620	402	KOA	De-Q L2, adjust gain, RLs
Q1	MC13851	MLP8	Freescale	eSiGe LNA

Table 4. Truth Table

Pin Function	Pin Name	Enable		Disable	
		Low Gain	High Gain	Low Gain	High Gain
Logic Circuit Bias V_{CC}	V_{CC}	1	1	1	1
Toggles Gain Mode (Active or Bypass)	Gain	0	1	0	1
Toggles LNA On/Off	Enable	1	1	0	0

Notes: 1. Logic state "1" equals V_{CC} voltage. Logic state of "0" equals ground potential.

2. V_{CC} is inductively coupled to LNA Out pin and V_{CC} pin.

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2010. All rights reserved.