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MC13851 Evaluation Board Quick Start — 2140 MHz

INTRODUCTION

This evaluation board design demonstrates one possible design at 2.75 V that satisfies competing requirements for NF, IP3, gain, return losses and current consumption. By changing any of the requirements, the performance for a particular parameter can be improved to meet a particular spec requirement.

This circuit was designed to provide NF < 1.5 dB, S21 gain > 17 dB using R1 = 1.2 kΩ and 1.5 kΩ.

Bias resistor R1 is used to adjust for the desired current drain and IP3 performance.

Gain or NF can be improved with matching changes to meet specific requirements.

Resistor R3 is used to de-Q output inductor L2 and adjust gain and return losses. Lowering R3 lowers gain and improves return losses.

The LNA is bias stabilized for variations in device and temperature.

NOTE: Tables 1 and 2 list measured parameters on three typical evaluation boards and are meant as a guide to the RF performance possible for this application circuit. Variations in matching component performance may result in variation in evaluation board performance results.

Table 1. Evaluation Board Measurements (2140 MHz, V_{CC} = 2.75 V, Frequency Spacing = 200 kHz, Non-Linear Measurements at P_{in} = -30 dBm)

Serial #	R1	Mode	Input Power (dBm)	Output Power (dBm)	Power Gain (dB)	Output IP3 (dBm)	Input IP3 (dBm)	Output Ref P_{1dB} (dBm)	Input Ref P_{1dB} (dBm)	NF (dB)	I_{CC} (mA)
1	1.2k	Active	-30.00	-12.63	17.37	17.72	0.35	8.37	-9.0	1.5	5.11
1	1.2k	Bypass	-30.00	-34.56	-4.56	20.94	25.5	—	—	4.55	1.55 nA
2	1.2k	Active	-30.00	-12.19	17.81	16.61	-1.2	7.91	-9.9	1.44	4.53
2	1.2k	Bypass	-30.00	-34.84	-4.84	21.16	26	—	—	4.78	3.6 nA
3	1.2k	Active	-30.00	-12.16	17.84	17.14	-0.7	7.94	-9.9	1.43	4.59
3	1.2k	Bypass	-30.00	-34.76	-4.76	21.24	26	—	—	4.89	7.6 nA
1	1.5k	Active	-30.00	-12.86	17.14	19.44	2.3	8.24	-8.9	1.46	4.01
1	1.5k	Bypass	-30.00	-34.55	-4.55	21.45	26	—	—	4.53	1.55 nA
2	1.5k	Active	-30.00	-12.55	17.45	17.35	-0.1	7.95	-9.5	1.43	3.52
2	1.5k	Bypass	-30.00	-34.84	-4.84	20.66	25.5	—	—	4.81	3.6 nA
3	1.5k	Active	-30.00	-12.43	17.57	18.07	0.5	8.07	-9.5	1.46	3.6
3	1.5k	Bypass	-30.00	-34.80	-4.80	21.20	26	—	—	4.82	7.6 nA

Table 2. S-Parameters (2140 MHz, V_{CC} = 2.75 V)

Serial #	R1	Mode	S11 (dB)	S21 (dB)	S12 (dB)	S22 (dB)
1	1.2k	Active	-12.06	17.36	-24.9	-9.84
1	1.2k	Bypass	-16.56	-4.56	-4.45	-25.57
2	1.2k	Active	-10.03	17.7	-24.3	-11.43
2	1.2k	Bypass	-12.47	-4.94	-4.74	-18.9
3	1.2k	Active	-9.92	17.72	-24.9	-12.73
3	1.2k	Bypass	-11.57	-4.89	-4.7	-17.9
1	1.5k	Active	-11.1	17.10	-24.6	-9.52
1	1.5k	Bypass	-16.3	-4.54	-4.44	-26.75
2	1.5k	Active	-8.8	17.49	-23.6	-10.75
2	1.5k	Bypass	-12.3	-4.89	-4.73	-19.20
3	1.5k	Active	-8.86	17.51	-23.5	-11.77
3	1.5k	Bypass	-11.61	-4.9	-4.76	-18

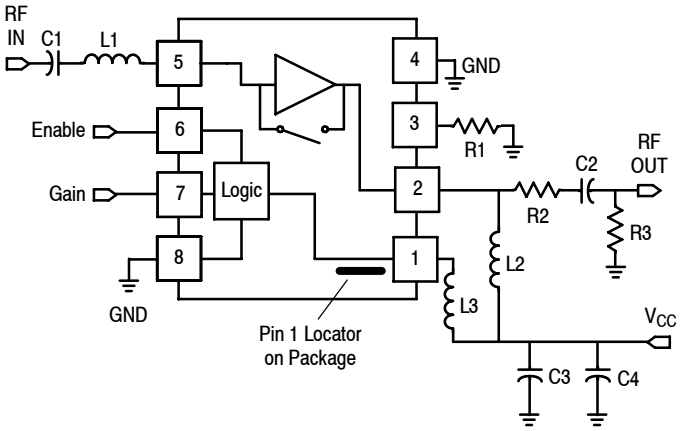

Figure 1. MC13851 2140 MHz Schematic

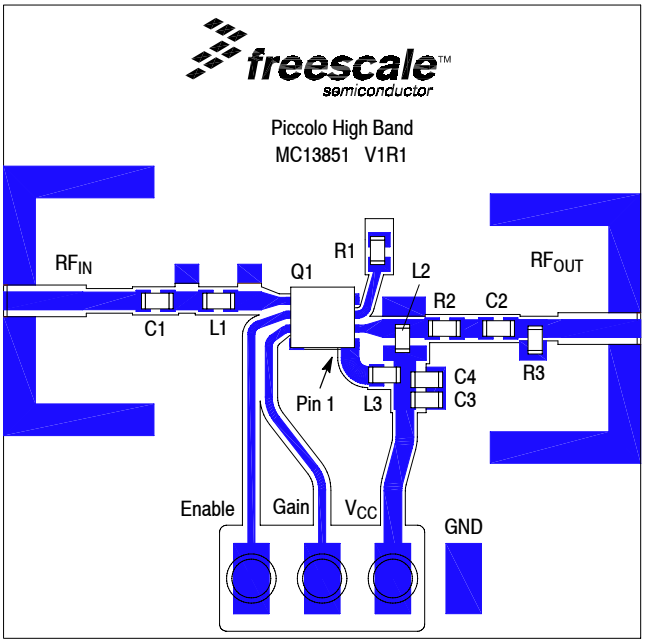

Figure 2. MC13851 2140 MHz Evaluation Circuit Component Layout

Table 3. Evaluation Circuit Component Designations and Values

Component	Value	Case	Manufacturer	Comments
C1	2.4 pF	402	Murata	Input match
C2	0.9 pF	402	Murata	Output match
C3	33 pF	402	Murata	RF bypass
C4	0.01 μF	805	Murata	Low freq bypass
L1	4.7 nH	402	Murata	Input match
L2	2.7 nH	402	Murata	Output match
L3	270 nH	402	Murata	Bias couple to logic
R1	1.2, 1.5 kΩ	402	KOA	LNA bias
R2	10 Ω	402	KOA	Stability
R3	620	402	KOA	De-Q L2, adjust gain, RLs
Q1	MC13851	MLP8	Freescale	eSiGe LNA

Table 4. Truth Table

Pin Function	Pin Name	Enable		Disable	
		Low Gain	High Gain	Low Gain	High Gain
Logic Circuit Bias V_{CC}	V_{CC}	1	1	1	1
Toggles Gain Mode (Active or Bypass)	Gain	0	1	0	1
Toggles LNA On/Off	Enable	1	1	0	0

Notes: 1. Logic state “1” equals V_{CC} voltage. Logic state of “0” equals ground potential.
2. V_{CC} is inductively coupled to LNA Out pin and V_{CC} pin.

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