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MC13852 Evaluation Board Quick Start — 900 MHz

INTRODUCTION

This evaluation board design demonstrates one possible design at 2.75 V and 4 or 5 mA that satisfies competing requirements for NF, IP3, gain, return losses and current consumption with unconditional stability. By changing any of the requirements, the performance for a particular parameter can be improved to meet a particular spec requirement.

This circuit was designed to provide NF < 1.3 dB, S21 gain > 18 dB using R1 = 1.2 kΩ and 1.5 kΩ.

OIP3 is preserved in bypass mode for high input signal conditions when the LNA is bypassed to lower gain and current draw.

Return losses are also preserved in bypass mode for excellent matching.

Gain or NF can be improved with matching changes to meet specific requirements.

Input return loss can be improved by increasing L1 to 33 nH, with NF increasing by 0.25 dB.

Resistor R3 is used to de-Q output inductor L2 and adjust gain and return losses. Lowering R3 lowers gain and improves return losses.

Bias resistor R1 is used to adjust for the desired current drain and IP3 performance.

The LNA is bias stabilized for variations in device and temperature.

NOTE: Tables 1 and 2 list measured parameters on three typical evaluation boards and are meant as a guide to the RF performance possible for this application circuit. Variations in matching component performance may result in variation in evaluation board performance results.

Table 1. Evaluation Board Measurements (900 MHz, V_{CC} = 2.75 V, Frequency Spacing = 200 kHz, Non-Linear Measurements at P_{in} = -30 dBm)

Serial #	R1	Mode	Input Power (dBm)	Output Power (dBm)	Power Gain (dB)	Output IP3 (dBm)	Input IP3 (dBm)	Output Ref P_{1dB} (dBm)	Input Ref P_{1dB} (dBm)	NF (dB)	I_{CC} (mA)
1	1.2k	Active	-30	-11.38	18.62	13.82	-4.8	9.92	-8.7	1.19	5.46
1	1.2k	Bypass	-30	-35.6	-5.60	21	26.6	—	—	6.03	6.8 μA
2	1.2k	Active	-30	-11.47	18.53	14.33	-4.2	9.53	-9.0	1.19	5.55
2	1.2k	Bypass	-30	-35.7	-5.7	20.8	26.5	—	—	6.22	34 nA
3	1.2k	Active	-30	-11.28	18.72	14.42	-4.3	9.52	-9.2	1.21	6.2
3	1.2k	Bypass	-30	-35.8	-5.8	21.2	27	—	—	6.2	135 nA
1	1.5k	Active	-30	-11.73	18.27	13.17	-5.1	10.27	-8.0	1.18	4.45
1	1.5k	Bypass	-30	-35.57	-5.57	21.03	26.6	—	—	6.04	6.8 μA
2	1.5k	Active	-30	-11.91	18.09	13.19	-4.9	9.89	-8.2	1.19	4.45
2	1.5k	Bypass	-30	-35.70	-5.70	20.80	26.5	—	—	6.21	34 nA
3	1.5k	Active	-30	-11.58	18.42	13.02	-5.4	9.42	-9.0	1.18	4.94
3	1.5k	Bypass	-30	-35.80	-5.80	21.20	27	—	—	6.22	135 nA

Table 2. S-Parameters (900 MHz, V_{CC} = 2.75 V)

Serial #	R1	Mode	S11 (dB)	S21 (dB)	S12 (dB)	S22 (dB)
1	1.2k	Active	-9.09	18.56	-28	-12.87
1	1.2k	Bypass	-11.83	-5.55	-5.57	-27.2
2	1.2k	Active	-8.39	18.45	-28.2	-13.72
2	1.2k	Bypass	-10.82	-5.76	-5.77	-24.1
3	1.2k	Active	-9.04	18.62	-28.1	-13.46
3	1.2k	Bypass	-10.77	-5.74	-5.78	-24.2

Serial #	R1	Mode	S11 (dB)	S21 (dB)	S12 (dB)	S22 (dB)
1	1.5k	Active	-7.8	18.21	-27.9	-12.07
1	1.5k	Bypass	-11.8	-5.55	-5.57	-27.30
2	1.5k	Active	-7.1	18.07	-27.8	-12.72
2	1.5k	Bypass	-10.8	-5.74	-5.79	-24.31
3	1.5k	Active	-7.78	18.33	-27.6	-12.57
3	1.5k	Bypass	-10.73	-5.77	-5.78	-24.67

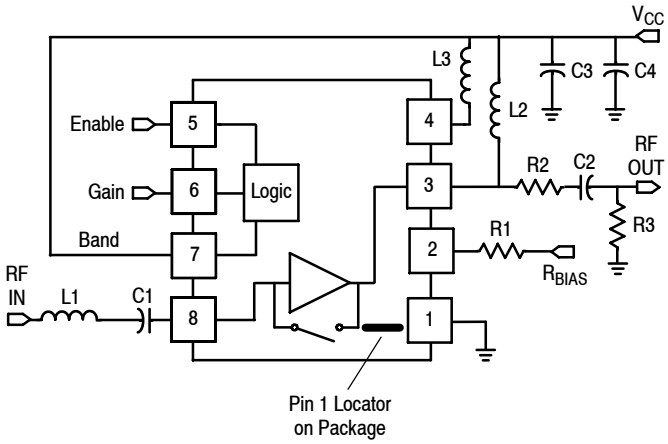

Figure 1. MC13852 900 MHz Schematic

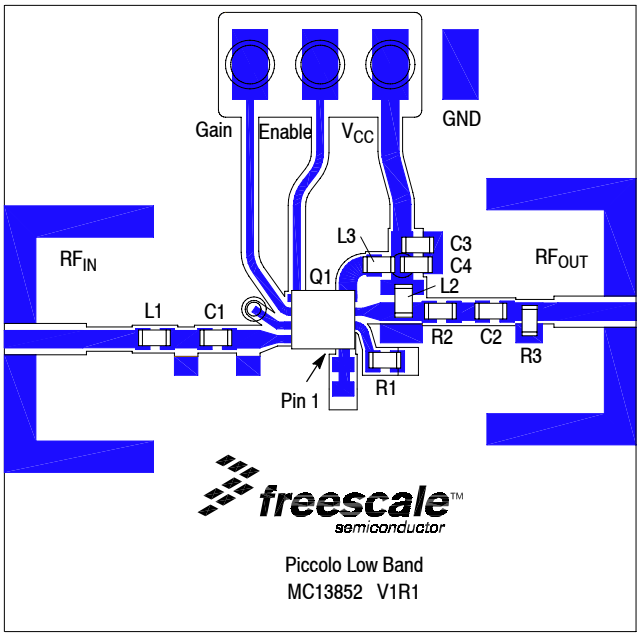

Figure 2. MC13852 900 MHz Evaluation Circuit Component Layout

Table 3. Evaluation Circuit Component Designations and Values

Component	Value	Case	Manufacturer	Comments	Impact
C1	3.9 pF	402	Murata	DC Block, Input match	S11, NF
C2	2.4 pF	402	Murata	DC Block, Output match	S22, gain
C3	0.1 uF	402	Murata	Low freq bypass	IP3
C4	33 pF	402	Murata	Bypass	IP3
L1	12 nH	402	Murata	Input match	S11, NF
L2	10 nH	402	Murata	Output match, bias decouple	S22, S11
L3	270 nH	402	Murata	Bias couple to logic	
R1	1.2 kΩ	402	KOA	Bias set point	
R2	20 Ω	402	KOA	Stability, lower gain	
R3	200 Ω	402	KOA	L2 de-Q	S22, S11, gain
Q1	MC13852	MLF 2x2	Freescale	SiGe LNA	

Table 4. Truth Table

Pin Function	Pin Name	Enable		Disable	
		Low Gain	High Gain	Low Gain	High Gain
Logic Circuit Bias V_{CC}	V_{CC}	1	1	1	1
Toggles Gain Mode (Active or Bypass)	Gain	0	1	0	1
Toggles LNA On/Off	Enable	1	1	0	0
Selects the LNA	Band	1	1	1	1

Notes: 1. Logic state “1” equals V_{CC} voltage. Logic state of “0” equals ground potential.
2. V_{CC} is inductively coupled to LNA Out pin and V_{CC} pin.

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