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Errata to i.MX51 Multimedia Applications Processor Reference Manual Rev. 1

This errata describes corrections to the *i.MX51 Reference Manual*, Revision 1. For convenience, the section number and page number of the errata item in the reference manual are provided.

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2.1, 2-5

In Table 2-1, “i.MX51 System Memory Map”, added a new row under “AIPS_TZ#2- Off Platform” after the 9th row as follows:

Table 2-1 i.MX51 System Memory Map (continued)

AP		Size	Region
Start Address	End Address		
83FD_C000	83FD_FFFF	16K	HSC

42.1.2, 42-3

Added a note after Table 42-1 as follows:

NOTE

Refer to Section 42.1.5, “High-Speed Communication Functionality” in order to understand the IPUv3EX - HSC architecture for camera and display port configuration.

42.1.5, 42-17

Added a new section, “High-Speed Communication Functionality”, after Section 42.1.4, “Modes of Operation” as follows:

42.1.5 High-Speed Communication (HSC) Functionality

The HSC bridge provides optional translation from the legacy parallel interfaces supported by the IPUv3EX. According to the architecture, the i.MX51 requires a special HSC configuration to operate in legacy mode which bypasses the HSC block.

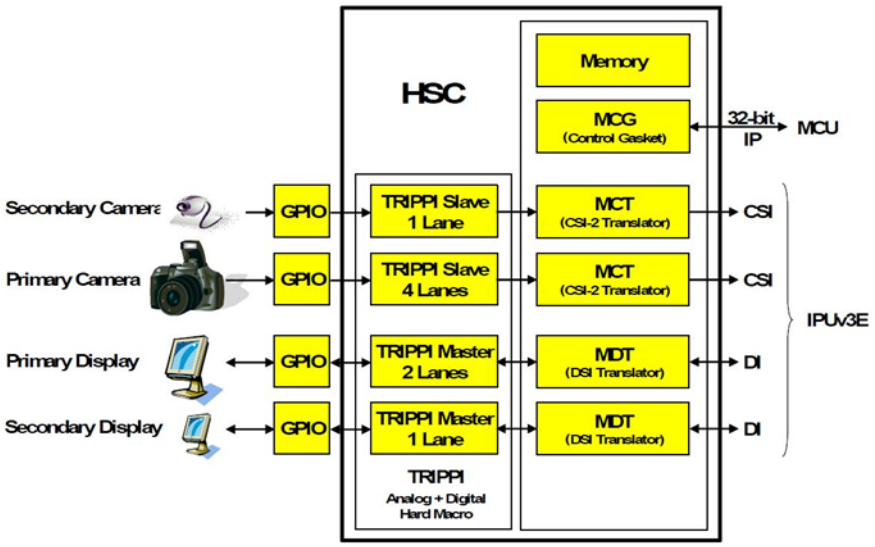

Figure 42-2. HSC Block Diagram

The HSC includes four bridges, two for cameras and two for displays.

Table 42-6 shows the HSC block description.

Table 42-6. Block Description

Block	Description
CSI-2 Translator (MCT)	Implements the protocol layer of the CSI-2 standard
DSI Translator (MDT)	Implements the protocol layer of the DSI standard
Transceiver Imaging Physical Protocol Interface (TRIPPI)	Implements the physical layer specified by the D-PHY standard
Control Gasket (MCG)	Provides configuration and control functions for the HSC

The HSC bypass configuration for CSI requires the following register settings:

Table 42-7 shows the HSC memory map and bypass settings.

Table 42-7. Memory Map and Bypass Settings

Abbreviation	Offset	Register	Access	Reset Value	By-Pass Value
MCD	0x0000	MCG Control Designation Register	R/W	0x0000_0000	0x0000_0F00
MCCMC	0x00D8	MCG CCM Control Register	R/W	0x0000_0000	0x0000_000C
MXT_CONF	0x0800	MXT Configuration Register	R/W	0x0000_0000	0xF003_008B

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