Hardware resets are held off until completion of the curr
herency. The processor resets at the end of the bus cycle
or after the bus monitor has timed out. The bus monitor
not, for the period of time that the BMT bits are set to.

The following reset sources reset all internal registers to
double bus fault, loss of clock. Execution of a RESET ir
the exception of the MCR registers. The MCR register in
are not affected by execution of a RESET instruction.

## 12. External Reset

On page 3-60, Figure 3-39, the $\overline{\text{RESET}}$ signal negates fo
not one. Note that $\overline{\text{RESET}}$ is not actively negated, and it

## 13. Power-On Reset

On page 3-61, Figure 3-40. Power-Up Reset Timing Dia
ternal control signals, and can begin toggling as soon a
operating. For crystal mode and external clock with VCO
stable value, the 328*TCLKIN delay is counted down, a
delay. For external clock mode without VCO, the 328*TC
are recognized.

## 14. RESET Instruction and CIC/QDMM

Add to the last paragraph on page 3-61: The RESET instr
or data.

## 15. CIC and QDMM Register Address

In Figure 4-1 on page 4-3, the QDMM end address is $0

## 16. Internal IMB Arbitration

On page 4-6, first paragraph, change the first sentence to
bus masters on the MC68349 to access the inter-modul

## 17. Additional Note for External Clock

On page 4-9, Table 4-1, External Clock Mode with PLL:
falling edge of the EXTCLK input clock. Maximum skew
signals is specified in Section 11 Electrical Characteristi

## 18. Recommended XFC Capacitor Va

On page 4-13, second paragraph, and page 10-2, last
0.01µF to 0.1µF applies specifically to crystal mode oper
phase detector reference frequencies > 1MHz start with
at 16.0MHz the recommended XFC capacitance is app
higher standard value available.

MOTOROLA

*Microprocessor and Memory Technologies Group*

*ADDENDUM TO*

# MC68349 Dragon 1 High Processor User's Manua

**May 5, 1995**

This addendum to the initial release of the MC6834 text, plus additional information not included in the or is maintained on the AESOP BBS, which can be (512)891-3650. Configure modem for up to 14.4K should support VT100 emulation. Internet acce [129.38.233.1] or through the World Wide Web at ht

## 1. Additional Note on MBAR Decod

Add to the CPU Space Cycles description on page block from $3FF00-3FFFF to the SIM module. An in for any access to this range, but selection of specific

Accesses to the MBAR register at long word $3FF0 cycles. Users should directly access only the MBAR LPSTOP broadcast access to $3FFFE. The remainir should not be accessed

## 2. Additional Notes on CPU Space

On page 3-33, Figure 3-22, the BKPT field for the Bre the T bit is on bit 1. The Interrupt Acknowledge LEV

## 3. Breakpoints

On page 3-33, the first paragraph implies that eith breakpoint can be used to insert an instruction. As nc can be used to insert an instruction on the breakpoir

## 4. Interrupt Latency

Add to the Interrupt Acknowledge Bus Cycles sectio from $\overline{IRQx}$ assert to prefetch of the first instruction instruction length in clocks (using 2-clock memory tables, this gives 34+71 (DIVS.L with worst-case < applications requiring shorter interrupt response tim modes and/or avoiding use of longer instructions (sp

## 5. Interrupt Hold Time and Spurious I

Add to the Interrupt Acknowledge Bus Cycles section c level sensitive and must remain asserted until the corresp exception may result or the interrupt may be ignored ent are autovectored using either the AVEC signal or the A interrupt arbitration cycle on the IMB if the external inter

## 6. Additional Note on Internal Autove

Add to the Autovector Interrupt Acknowledge Cycle se autovectored either by the AVEC register programming started and terminated internally. The interrupting devic resulting operation is undefined.

## 7. Additional Notes on Retry Termina

On page 3-44, Table 3-8: When $\overline{HALT}$ and $\overline{BERR}$ are ass bus cycle, relative timing of $\overline{HALT}$ and $\overline{BERR}$ must be c mination case #3. This can be done by asserting $\overline{HALT}$ a control which edge each is recognized on, or asynchro 47B] ns before $\overline{BERR}$ to guarantee recognition on or be

## 8. Active Negate on Bus Arbitration

The 68349 actively pulls up all tri-stateable bus pins oth arbitration. This pullup function is not guaranteed to res reduce rise time on these signals when using weak exte

## 9. Additional Note on Bus Arbitration

For the bus arbitration description beginning on page 3-5 ters for this device is external request via $\overline{BR}$ (highest p channels 1 and 2 relative to each other is selected by th

## 10. Additional Note on Bus Arbitratio

For the bus arbitration description beginning on page 3 when a higher priority request is recognized. For examp results in a sequence of four bus cycles to complete the until the completion of the fourth bus cycle. A single addr a dual address DMA transfer, the read and write portions tion between the read and write bus cycles. Also, if diffe for the source and destination, arbitration can occur be must be made to the smaller port for each operand acce for a TAS instruction is also indivisible to guarantee data erand transfer of a multi-operand operation such as a M

## 11. Additional Notes on RESET Intera

Add to the Reset Operation description beginning page

This document contains information on a product under development. Motor

## 21. Additional Note for Global Chip S

On page 4-18, section 4.2.4.2: When operating as a glo
either the MBAR or to internal peripheral module registe

## 22. Additional Note on PORTA/B Outp

Add to the External Bus Interface Operation description
sition after the S4 falling edge for the internal write to th
tions at roughly the same time DS negates for the data
specified in the Electrical Specifications.

## 23. Typo in Chip Selects

On page 4-20, first paragraph, the last sentence should
register, not the module base address register.

## 24. MBAR Register Reset Values

On page 4-23, the reset values for MBAR bits 31-12 are

## 25. MBAR AS7 Bit and IACK Cycles

On page 4-24, the second code sequence initializes th
dress decode for the internal 4K register block from res
vents the register block decode of $FFFFFxxx from inte
possibly corrupting the vector number returned. Normal
ules is not affected by this change.

Early versions of the MC68330 User's Manual (original
Rev. 1 releases) did not show AS7 set. Code which was
be checked for this problem when porting to the MC68
MC68330 and/or MC68340 designs.

## 26. Additional Note on VCO Overshoo

On page 4-32 place the following note under the Y-bits

A VCO overshoot can occur when increasing the opera
register. The effects of this overshoot can be controlled

1. Write the X bit to zero. This will reduce the previous
2. Write the Y bits to the desired frequency divided by
3. After the VCO lock has occurred, write the X bit to
   clock frequency to the desired frequency.

Steps 1 and 2 may be combined.

## 27. Typo on Base Address 2

On page 4-33, the chip select register bits for Base Add

## 19. VCO Frequency Limit

On page 4-13, last paragraph: although changing the X
no affect the VCO frequency, since the divider these bits
W or Y bits does change the VCO frequency, and the ma
when programming these bits.

## 20. CLKOUT and VCO Frequency Pro

On pages 4-14 and 4-15, the column for W=1:Z=0:X=1
column is 2x the frequency in the X=0 column immediate
ing pages. Note that although a complete table is shown
frequency limits must be observed when programming th
cy (CLKOUT) of 25.16MHz can be selected with W:X:Y:Z
However, programming W:X:Y:Z=1:0:47:1 to achieve th
quency of greater than 100MHz, which is outside the s
which violates current 25MHz electrical specs is shown


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## Table 4-2. System Frequencies

| Y | CLKOUT (kHz) | | | | VCO (kHz) |
|---|---|---|---|---|---|
| | W = 0 | | | | W = 0 |
| | Z = 0 | | Z = 1 | | Z = x |
| | X = 0 | X = 1 | X = 0 | X = 1 | X = x |
| 0 | 16 | 33 | 131 | 262 | 524 |
| 1 | 33 | 66 | 262 | 524 | 1049 |
| 2 | 49 | 98 | 393 | 786 | 1573 |
| 3 | 66 | 131 | 524 | 1049 | 2097 |
| 4 | 82 | 164 | 655 | 1311 | 2621 |
| 5 | 98 | 197 | 786 | 1573 | 3146 |
| 6 | 115 | 229 | 918 | 1835 | 3670 |
| 7 | 131 | 262 | 1049 | 2097 | 4194 |
| 8 | 147 | 295 | 1180 | 2359 | 4719 |
| 9 | 164 | 328 | 1311 | 2621 | 5243 |
| 10 | 180 | 360 | 1442 | 2884 | 5767 |
| 11 | 197 | 393 | 1573 | 3146 | 6291 |
| 12 | 213 | 426 | 1704 | 3408 | 6816 |
| 13 | 229 | 459 | 1835 | 3670 | 7340 |
| 14 | 246 | 492 | 1966 | 3932 | 7864 |
| 15 | 262 | 524 | 2097 | 4194 | 8389 |
| 16 | 279 | 557 | 2228 | 4456 | 8913 |
| 17 | 295 | 590 | 2359 | 4719 | 9437 |
| 18 | 311 | 623 | 2490 | 4981 | 9961 |
| 19 | 328 | 655 | 2621 | 5243 | 10486 |
| 20 | 344 | 688 | 2753 | 5505 | 11010 |
| 21 | 360 | 721 | 2884 | 5767 | 11534 |
| 22 | 377 | 754 | 3015 | 6029 | 12059 |
| 23 | 393 | 786 | 3146 | 6291 | 12583 |
| 24 | 410 | 819 | 3277 | 6554 | 13107 |
| 25 | 426 | 852 | 3408 | 6816 | 13631 |
| 26 | 442 | 885 | 3539 | 7078 | 14156 |
| 27 | 459 | 918 | 3670 | 7340 | 14680 |
| 28 | 475 | 950 | 3801 | 7602 | 15204 |
| 29 | 492 | 983 | 3932 | 7864 | 15729 |
| 30 | 508 | 1016 | 4063 | 8126 | 16253 |
| 31 | 524 | 1049 | 4194 | 8389 | 16777 |



## Table 4-2. System Frequencies from 3

| Y | CLKOUT (kHz) | | | | VCO (kHz) |
|---|---|---|---|---|---|
| | W = 0 | | | | W = 0 |
| | Z = 0 | | Z = 1 | | Z = x |
| | X = 0 | X = 1 | X = 0 | X = 1 | X = x |
| 32 | 541 | 1081 | 4325 | 8651 | 17302 |
| 33 | 557 | 1114 | 4456 | 8913 | 17826 |
| 34 | 573 | 1147 | 4588 | 9175 | 18350 |
| 35 | 590 | 1180 | 4719 | 9437 | 18874 |
| 36 | 606 | 1212 | 4850 | 9699 | 19399 |
| 37 | 623 | 1245 | 4981 | 9961 | 19923 |
| 38 | 639 | 1278 | 5112 | 10224 | 20447 |
| 39 | 655 | 1311 | 5243 | 10486 | 20972 |
| 40 | 672 | 1343 | 5374 | 10748 | 21496 |
| 41 | 688 | 1376 | 5505 | 11010 | 22020 |
| 42 | 705 | 1409 | 5636 | 11272 | 22544 |
| 43 | 721 | 1442 | 5767 | 11534 | 23069 |
| 44 | 737 | 1475 | 5898 | 11796 | 23593 |
| 45 | 754 | 1507 | 6029 | 12059 | 24117 |
| 46 | 770 | 1540 | 6160 | 12321 | 24642 |
| 47 | 786 | 1573 | 6291 | 12583 | 25166 |
| 48 | 803 | 1606 | 6423 | 12845 | 25690 |
| 49 | 819 | 1638 | 6554 | 13107 | 26214 |
| 50 | 836 | 1671 | 6685 | 13369 | 26739 |
| 51 | 852 | 1704 | 6816 | 13631 | 27263 |
| 52 | 868 | 1737 | 6947 | 13894 | 27787 |
| 53 | 885 | 1769 | 7078 | 14156 | 28312 |
| 54 | 901 | 1802 | 7209 | 14418 | 28836 |
| 55 | 918 | 1835 | 7340 | 14680 | 29360 |
| 56 | 934 | 1868 | 7471 | 14942 | 29884 |
| 57 | 950 | 1901 | 7602 | 15204 | 30409 |
| 58 | 967 | 1933 | 7733 | 15466 | 30933 |
| 59 | 983 | 1966 | 7864 | 15729 | 31457 |
| 60 | 999 | 1999 | 7995 | 15991 | 31982 |
| 61 | 1016 | 2032 | 8126 | 16253 | 32506 |
| 62 | 1032 | 2064 | 8258 | 16515 | 33030 |
| 63 | 1049 | 2097 | 8389 | 16777 | 33554 |

NOTES:

1. Some W/X/Y/Z bit combinations shown may select a CLK which violates current 25MHz electrical specs is shown i **Section 11 Electrical Characteristics** for CLKOUT and
2. Any change to W or Y results in a change in the VCO frequ

MOVE.L NUMBYTE,DMABTC1(A0) should be MOVE

## 49. Serial Oscillator Problems with DI

Add to the Crystal Input or External Clock (X1) section o
1MHz) with excessive undershoot on $\overline{\text{DREQ1}}$ can result
lator X1 pin, damping out oscillation. Avoid routing $\overline{\text{DREQ}}$
use termination techniques such as series termination o
of the signal and accompanying undershoot.

## 50. Additional Note on $\overline{\text{RTSx}}$ operatio

Add to the $\overline{\text{RTSA}}$ and $\overline{\text{RTSB}}$ descriptions on page 8-6: T
logic “0” when set, and a logic “1” when cleared.

$\overline{\text{RTSx}}$ can be set (output logic level 0) by any of the follo

- Writing a “1” to the corresponding bit in the OPSET
- Issuing an “Assert RTS” command using command
- If RxRTS=1, set by receiver FIFO transition from FU

$\overline{\text{RTSx}}$ can be cleared (output logic level 1) by any of the

- Hardware reset of the serial module
- Writing a “1” to the corresponding bit in the OPRESI
- Issuing a “Negate RTS” command using command
- If RxRTS=1, cleared by receiver FIFO transition fror
- If TxRTS=1, cleared by completion of last character

## 51. Serial Frequency Restriction - Suf

Beginning with the current "A" suffix MC68349 productio
internal clock synchronization has been revised to relax
using the internal baud rate generators. The revised CL
specifications - no change to existing designs will be req
shown here are preliminary, and subject to change with

Previously, a minimum 8.3MHz CLKOUT frequency was
with the default 3.6864MHz serial crystal. In the new s
been modified to allow the minimum CLKOUT frequency
selected. Operation and specifications for external cloc

The table below shows the resulting minimum CLKOUT
that applications using the VCO clock modes - crystal
131KHz minimum CLKOUT frequency.

## 28. Additional Notes on Cache Operat

In applications which use the CIC in mixed-mode (i.e. a
BADDRx register for each cache block also. If the MD
instruction cache portion of the CIC, the corresponding c
dress to map them to a temporary unused memory regio
use the ENAB bit instead of the MD bits to enable/disabl
turning the cache back on if any previously executed co

## 29. Bus Error Stack Frame

On page 5-51, in the next-to-last paragraph, delete “(the
and the SSW is located at SP+12)”. The stack space allo
internal count register and SSW remains the same. The
counter location SP+10 and SP+12 will contain invalid
frames, look at the first nibble of the faulted exception fo
the four-word frame, and $2 for the six-word frame.

## 30. Typo in Reference

On page 5-57, Table 5-9: The SSW is described in secti

## 31. DSO Timing

On page 5-61, Figure 5-27, DSO transitions one clock la

## 32. Typo on BDM RSREG Command

On page 5-68, Section 5.7.2.8.6, RSREG command bit

## 33. Additional Notes on DMA Feature

In the feature set listed on page 7-1, bullet six is “Opera
fers”. This packing is for transfers between different por
e.g. Byte <> Word transfers. The DMA controller does no
problem of residual bytes left in the controller when a ch

## 34. Additional Note on Internal Reque

Add to the Internal Request Generation section beginnin
and $\overline{\text{DONEx}}$ are not active as outputs during transfers.
channel operation if asserted - pull up if not used.

## 35. Additional Note on Cycle Steal

For the cycle steal mode description starting on the botto
have to be held off until after the channel is started. If $\overline{\text{DR}}$
by setting the channel start bit, an internal $\overline{\text{DREQ}}$ asserti
DMA cycle to start.


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## 36. Additional Note on DMA Transfer

Add to the External Request Generation section beginni
synchronization and IMB bus arbitration activity before
sertion will preempt the next CPU bus cycle if it is recogr
bus cycle, unless the current cycle is not the last cycle o
Operand transfers and RMC read/write sequences are i
not be arbitrated from the CPU until the complete opera
sizing results in multiple bus cycles.

For a $\overline{\text{DREQx}}$ assertion during an idle bus period, bus sta
clock falling edge which $\overline{\text{DREQx}}$ is recognized on. Th
$\overline{\text{DREQx}}$ is recognized on to the falling edge that $\overline{\text{AS}}$ for
table for various memory speeds.

**DREQ Latency (Clocks) vs. Bu**

| Access Type | Maximum | | | | |
|---|---|---|---|---|---|
| | 32-Bit Bus Clocks/Bus Cycle | | | | Clo |
| | 2 | 3 | 4 | 5 | 2 |
| Longword | 5 | 6 | 7 | 8 | 7 |
| RMC (TAS) | 10 | 12 | 14 | 16 | 10 |

## 37. Additional Note on Burst Transfer

On page 7-5, replace the 2nd paragraph of 7.3.2.1 Exte
negated one clock before the end of the last DMA bus c
being generated. Also, $\overline{\text{DREQx}}$ must be negated two cloc
an idle clock between that transfer and the following CP

## 38. Additional Note on Cycle steal DM

Add to the External Cycle Steal Mode description on pa
ently. However, for some 2-clock accesses using cycle s
incomplete overlap of the DMA transfer with internal IM
single address 2-clock transfers and 2) dual address tra
completely overlapped for all other cases.

## 39. Additional Note on Cycle Steal Sta

For the external cycle steal mode description on page
held off until after the channel is started. If $\overline{\text{DREQx}}$ is alr
the channel start bit, an internal $\overline{\text{DREQx}}$ assertion is gen
to start.

## 40. $\overline{\text{DREQx}}$ Negation on Burst

On page 7-8, Figure 7-5, and on page 7-10, Figure 7-7,
(one clock earlier than shown) to prevent another DMA
7-5 on Burst Transfer $\overline{\text{DREQx}}$ Negation.

## 41. $\overline{\text{DREQ}}$ Assert Time

On page 7-21, Figure 7-13: The second $\overline{\text{DREQx}}$ assertio
antee recognition on 2 consecutive clock falling edges.
1 should be deleted.

## 42. Fast Termination and Burst Requ

On the last paragraph of page 7-21, delete the referenc
incorrectly - it actually shows operation with fast termina
second $\overline{\text{DREQx}}$ signal should be held for 2 consecutive
1 clock edge. Note 1 of Figure 7-14 should be deleted.

## 43. Typo in DAPI

On page 7-26, for DAPI = 1, the DAR is incremented ac

## 44. Additional note on DMA limited ra

On page 7-27, in the BB-Bus Bandwidth Field: The DMA
is the bus master (each channel has its own counter).
relinquish the bus before completion of the active count
Higher priority requests could come from 1) the other
CPU32 core (if either the interrupt mask level in the SR
channel's ISM level), or 3) an external bus request. Wh
releases the bus, and the “idle” count increments regard

## 45. Configuration Error

The Configuration Error description paragraph at the top
error results when 1) either the SAR or DAR contains a
in the CCR, or 2) the BTC register does not match the la

## 46. Additional Note on DMA Interrupt

Add to the Interrupt Register description on page 7-31: W
interrupt level, channel 1 is higher priority than channel

## 47. Single Address Enable

7-33 SE-Single Address Enable: The note “used for in
MC68349 does not support intermodule single address t
to “0”.

## 48. Code Examples - Immediate Addr

On pages 7-40 through 7-45 make the following change a
and NUMBYTE (change to immediate addressing mode

MOVE.L SARADD,DMASAR1(A0) should be MOVE.

MOVE.L DARADD,DMADAR1(A0) should be MOVE.



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## 62. Data Setup Time for 3.3V

On page 11-8, electrical specification #27 (Data Setup changed from 5ns to 8ns.

## 63. Bus Arbitration Notes

On page 11-15, Figure 11-6, specification #47A should incorrectly shows it measured to the rising edge of S5, c

## 64. Serial Module Specs

Note 1 on page 11-20 should reference synchronous op

## 65. MC68349 Ordering Information

Currently available part numbers are listed in the table b

| Supply Voltage | Package Type | Frequency (MHz) |
|---|---|---|
| 5.0 V | Plastic Quad Flat Pack<br>FT Suffix | 0 – 16.78<br>0 – 16.78<br>0 – 25 |
| 3.3 V | Plastic Quad Flat Pack<br>FT Suffix | 0 – 16.78 |

## 66. Package Dimensions

The package dimension drawing on page 12-4 should b

**Minimum CLKOUT Fr**

| baud rate | CLKOUT $F_{min}$ |
|---|---|
| 50 | 3250Hz* |
| 75 | 4850Hz* |
| 110 | 7090Hz* |
| 134.5 | 8660Hz* |
| 150 | 9650Hz* |
| 200 | 12.9kHz* |
| 300 | 19.3kHz* |
| 600 | 38.5kHz* |
| 1050 | 67.3kHz* |
| 1200 | 76.9kHz* |

The minimum CLKOUT frequency is calculated using th

$$CLKOUT(min) = 1/((1/(baud\_rate*sample\_rate)-T_{setu}$$

where Sample_rate = 48 for 76.8Kbaud and 32 for other

$$CLKOUT(min) =1/((1/(baud\_rate*32)-30ns)/2)(50-384$$

$$1/((1/(baud\_rate*48)-30ns)/2)(76.8K\ baud)$$

Note that with this revision, replacing the serial crystal wi longer affects the minimum CLKOUT frequency for a sp synchronized. Also, the logic for the CTSx inputs uses th should be kept above 76.9KHz to avoid affecting CTSx

## 52. 68349 Serial Module RTS Differen

Add to the description for receiver-controlled RTS oper MC68681, the RTSx signal does not have to be manually flow capability on the receiver.

## 53. Additional Note on Serial multidro

Add to the Multidrop Mode section beginning on page 8- the transmitter to manipulate the A/D bit, as generally i the previous character completes transmission (i.e. TxE pends it to the data character when the character is tra shift register. Once this transfer occurs (as indicated b changed without affecting the character in progress. Th bit for the next character would be:

1.) poll TxRDY until asserted (or interrupt on TxRDY
2.) set/clear A/D bit in MR1 for new character
3.) write character to transmit buffer (TB)

4.) A/D bit can be changed only after TxRDY assert

No other bits in MR1 should be modified when changing

## 54. MC68349 BSDL File

An electronic copy of the BSDL file for the MC68349 114 on the AESOP BBS - refer to the beginning of this docu

## 55. Additional Note on Oscillator Lay

Add to the Processor Clock Circuitry (page 10-1) and S short connections and place external oscillator compone through or near the oscillator circuit, especially high fre note above on $\overline{\text{DREQ1}}$ and serial oscillator for page 8-5 use a separate trace for ground to the oscillator so that i

## 56. Recommended 32KHz Oscillator C

On page 10-2, Figure 10-2, the component values show vide enough loop gain for all crystals. For a more gen shown below. A 10M resistor can be substituted for the

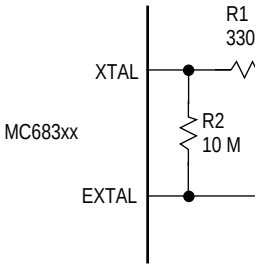



**Figure 10-2. Sampl**

## 57. Corrections to 8/16-Bit DMA Cont

On page 10-10, the logic driving $\overline{\text{OE}}$ on the 74F245 in Fi though not detailed, the byte enables for the memory bl tention between the upper and lower bytes of the data b

## 58. Clock VIH

On page 11-5 DC Electrical Specifications, the Clock In and X1 inputs.

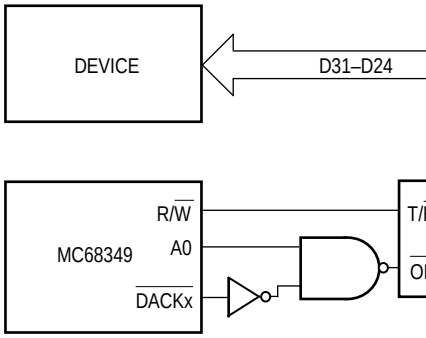



**Figure 10-12. Circuit for Interfacing in Single-Addres**

## 59. Operating IDD Limits

On page 11-5, the spec operating (RUN) currents are sh

| Product | Frequency | Max Idd |
|---|---|---|
| MC68349FT16V | 16.78MHz | 110mA@3.6V |
| MC68349FT16 | 16.78MHz | 170mA@5.25 |
| MC68349CFT16* | 16.78MHz | 175mA@5.25 |
| MC68349FT25 | 25.16MHz | 230mA@5.25 |

* Extended temperature device.

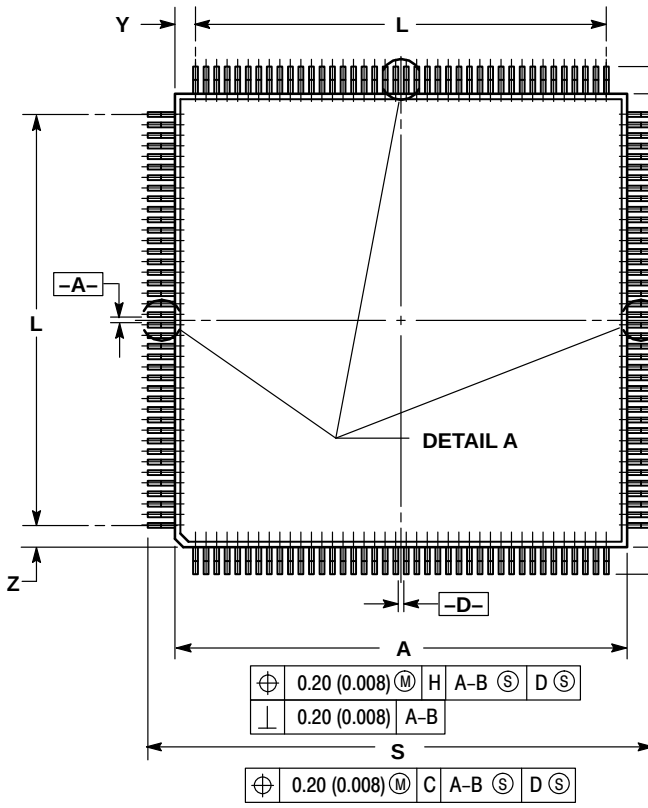
## 60. Input Clock Duty Cycle in Externa

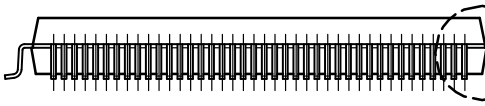
On page 11-6, Note 7 at the bottom of the page: The inp mode can be used when the VCO is not turned off during the input clock is used for clocking the SIM, and must n External Clock Mode Without PLL.

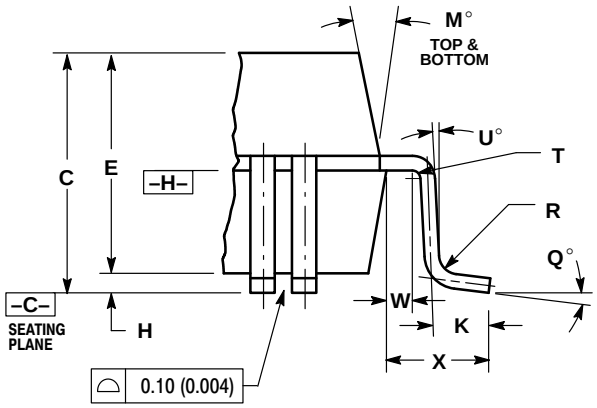
## 61. Typos on Clock Skew Notes

Page 11-7, Note 11: Delete the second sentence "Cloc clock signals". The clock skew is 10-40ns between co CLKOUT.

Note 12: The last sentence should say "Clock skew is me The PLL phase locks the falling edge of CLKOUT to the






DETAIL C

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Case 86

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