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**MOTOROLA***Microprocessor and Memory
Technologies Group***MC68349**

UPDATE TO MC68349 Dragon 1 High Performance Integrated Processor User's Manual and Addendum

November 3, 1995

1. Negation of $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ for Retry Sequence and Late Retry Sequence.

Figure 3-31 and Figure 3-32 on pages 3-48 and 3-49 respectively, should show $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ being negated one-half clock cycle earlier. The corrected drawings are shown in Figure 1 and Figure 2 of this document.

2. Typo in Channel Status Register (CSR) description.

The last sentence for the IRQ bit description on page 7-28 should be changed to "The STR bit in the CCR cannot be set when this bit is set; all error status bits must be cleared before the STR bit can be set."

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SEMICONDUCTOR PRODUCT INFORMATION

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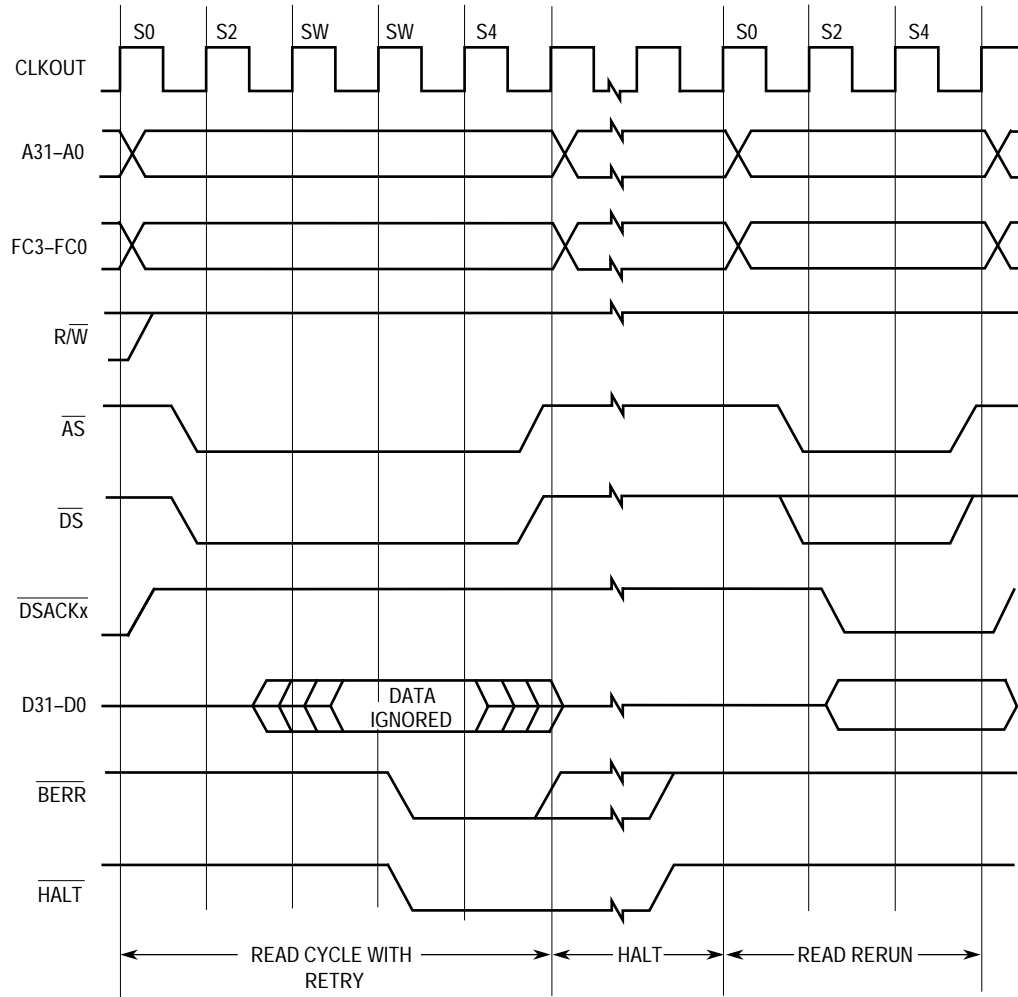


Figure 1. Retry Sequence Timing

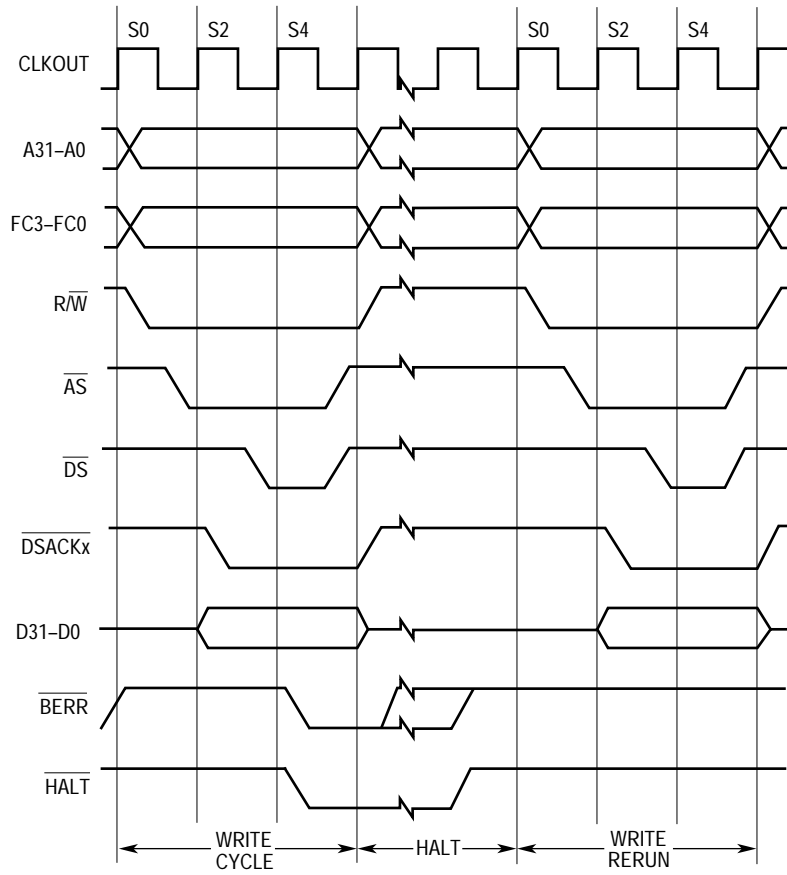



Figure 2. Late Retry Sequence Timing



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