Advance Information

MPC185HWRM
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MPC185
Hardware Reference Manual

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This document describes how to design a system with the MPC185 and the MPC8260 or the MPC107. It describes pertinent electrical and physical characteristics of the MPC185; for functional characteristics of the processor, refer to the *MPC185 Security Co-Processor User's Manual*.

This document contains the following topics:

To locate any published errata or updates for this document, refer to the web site at http://www.motorola.com/semiconductors.

1 Overview

The MPC185 is a flexible and powerful addition to any networking or computing system using the Motorola PowerQUICC II™ line of integrated communications processors, or any system supporting the 60x bus protocol. The MPC185 is designed to offload computational intensive security functions, such as key generation and exchange, authentication, and bulk encryption from the host PowerPC™ processor.

The MPC185 is optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, and SSL/TLS. In addition, the Motorola family of security co-processors are the only devices on the market capable of executing elliptic curve cryptography, which is especially important for secure wireless communications.

MPC185 features include the following:

- Two public-key execution units (PKEUs) that support the following:
  - RSA and Diffie-Hellman
    - Programmable field size up to 2048 bits
  - Elliptic curve cryptography
    - F_2m and F(p) modes
    - Programmable field size up to 511 bits
- Two Data Encryption Standard execution units (DEUs)
  - DES, 3DES
  - Two-key (K1, K2, K1) or three-key (K1, K2, K3)
  - ECB and CBC modes for both DES and 3DES
- Two Advanced Encryption Standard units (AESUs)
  - Implements the Rijndael symmetric-key cipher
  - Implements ECB, CBC, and counter modes
- One ARC four execution unit (AFEU)
  - Implements a stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- Two message digest execution units (MDEUs)
  - SHA-1 with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- One Kasumi execution unit for 3GPP systems (KEU)
  - Implements F8 algorithm for encryption and F9 algorithm for authentication
- One random number generator (RNG)
- 60x compliant external bus interface, with master/slave logic
  - 32-bit address/64-bit data
  - 100 MHz operation
- Four crypto-channels, each supporting multi-command descriptor chains
  - Static and/or dynamic assignment of crypto-execution units via an integrated controller
  - Buffer size of 2 Kbytes for each execution unit, with flow control for large data sizes
- 32 Kbytes of internal scratchpad memory for key, IV, and context storage
- 1.5-V core power supply, 3.3-V and 2.5-V I/O
- 256 MAP BGA, 17 x 17 mm package body size

2 System Architecture

The MPC185 is designed to integrate easily into any system using the 60x bus protocol. The MPC185 is ideal in any system using a Motorola PowerQUICC II communications processor (as shown in Figure 1) or a PowerPC processor and memory controller. The ability of the MPC185 to be a master on the 60x bus, allows the co-processor to offload the data movement bottleneck normally associated with slave devices. The external processor accesses the MPC185 through its device drivers using system memory for data storage. The MPC185 resides in the memory map of the processor; therefore, when an application requires cryptographic functions, it simply creates descriptors for the MPC185 which define the cryptographic function to be performed and the location of the data. The MPC185 60x-mastering capability permits the host processor to set up a crypto-channel with a few short register writes, leaving the MPC185 to perform reads and writes on system memory to complete the required task.

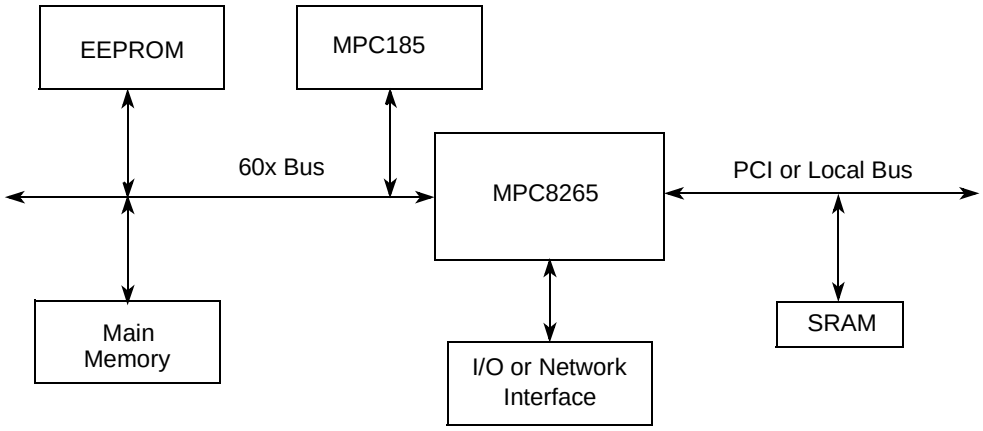


Figure 2-1. MPC185 Connected to PowerQUICC II 60x Bus

Figure 2-2 shows a configuration with the MPC185 communicating with the host processor using a PCI bridge, such as the MPC107.

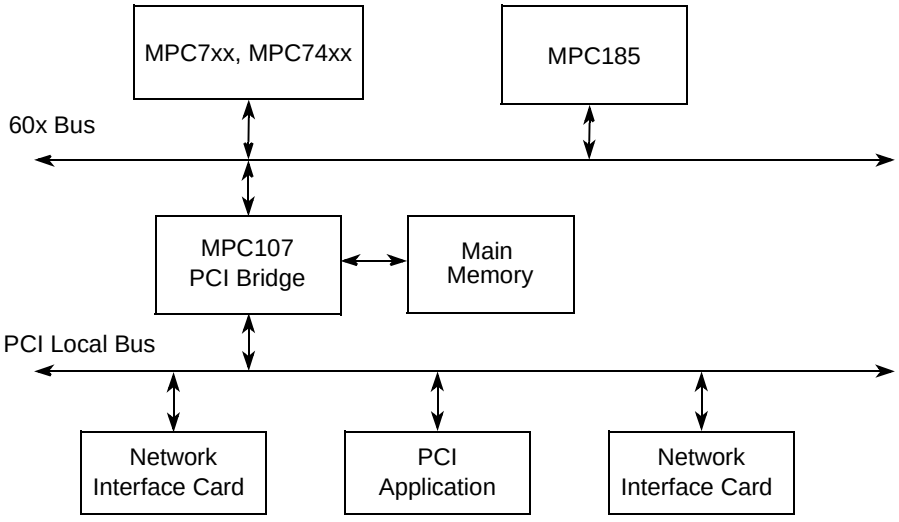


Figure 2-2. MPC185 Connected to a Host CPU using a Bridge

3 Pin Assignments

The MPC185 pin assignments are shown in Table 1.

Table 1. MPC185 Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	A10	A9	A8	A2	A1	A0	TT2	TT0	TSIZ0	$\overline{\text{TBST}}$	$\overline{\text{TS}}$	$\overline{\text{TEA}}$	$\overline{\text{WT}}$	BASE3	$\overline{\text{IRQ}}$	TCK	**A**
B	A13	A12	A11	A5	A4	A3	TT3	TT1	TSIZ1	$\overline{\text{AACK}}$	$\overline{\text{LB}}$ CLAIM	$\overline{\text{BR}}$	$\overline{\text{CI}}$	$\overline{\text{GBL}}$	$\overline{\text{RESET}}$	$\overline{\text{TRST}}$	**B**
C	AP1	A15	A14	A7	A6	AP0	TT4	TSIZ3	TSIZ2	$\overline{\text{ABB}}$	NC	BASE4	BASE2	BASE1	BASE0	TMS	**C**
D	A17	A16	AP2	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	PLL Bypass	3.3 V	3.3 V	XLBCL KMODE	XLB MODE	TDI	**D**
E	A20	A19	A18	3.3 V	1.5 V	1.5 V	1.5 V	1.5 V	1.5 V	1.5 V	1.5 V	1.5 V	3.3 V	NC	SE	TDO	**E**
F	A23	A22	A21	3.3 V	1.5 V	VSS	VSS	VSS	VSS	VSS	VSS	1.5 V	3.3 V	$\overline{\text{DBB}}$	PLL Range	CLK	**F**
G	A25	A24	AP3	3.3 V	1.5 V	VSS	VSS	VSS	VSS	VSS	VSS	1.5 V	3.3 V	AVSS	TPA	AVDD	**G**
H	A28	A27	A26	3.3 V	1.5 V	VSS	VSS	VSS	VSS	VSS	VSS	1.5 V	3.3 V	DP0	D1	D0	**H**
J	A31	A30	A29	3.3 V	1.5 V	VSS	VSS	VSS	VSS	VSS	VSS	1.5 V	3.3 V	D4	D3	D2	**J**
K	D63	D62	DP7	3.3 V	1.5 V	VSS	VSS	VSS	VSS	VSS	VSS	1.5 V	3.3 V	D7	D6	D5	**K**
L	D61	D60	D59	3.3 V	1.5 V	VSS	VSS	VSS	VSS	VSS	VSS	1.5 V	3.3 V	DP1	D9	D8	**L**
M	D58	D57	D56	3.3 V	1.5 V	1.5 V	1.5 V	1.5 V	1.5 V	1.5 V	1.5 V	1.5 V	3.3 V	D12	D11	D10	**M**
N	D55	D54	DP6	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	D15	D14	D13	**N**
P	D53	D52	D47	D46	DP5	D39	D38	DP4	$\overline{\text{ARTRY}}$	NC	DP3	D25	D24	DP2	D17	D16	**P**
R	D51	D50	D45	D44	D43	D37	D36	D35	$\overline{\text{S\_DBG}}$	$\overline{\text{M\_DBG}}$	D28	D27	D26	D20	D19	D18	**R**
T	D49	D48	D42	D41	D40	D34	D33	D32	$\overline{\text{TA}}$	$\overline{\text{BG}}$	D31	D30	D29	D23	D22	D21	**T**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	

4 Signal Descriptions

Table 2 provides the pinout listing for the package. A bar over a signal name indicates that the signal is active low—for example, $\overline{\text{AACK}}$ and $\overline{\text{ABB}}$. Active-low signals are referred to as asserted (active) when they are low and negated when they are high.

Table 2. Pin Descriptions

Signal Name	Pin Locations	Signal Type	Description
60x Signals			
A[0:31]	A6, A5, A4, B6, B5, B4, C5, C4, A3, A2, A1, B3, B2, B1, C3, C2, D2, D1, E3, E2, E1, F3, F2, F1, G2, G1, H3, H2, H1, J3, J2, J1	I/O	60x address bus—When the MPC185 is a master, these signals function as the 60x address bus to the system memory controller. When the MPC185 is a slave, these address signals are decoded internally to address the individual modules.
$\overline{\text{AACK}}$	B10	I/O	60x address acknowledge—A 60x bus slave asserts this signal to indicate that it identified the address tenure. Assertion of this signal terminates the address tenure.
$\overline{\text{ABB}}$	C10	O	60x address bus busy—The MPC185 asserts this signal for the duration of the address bus tenure. Following an $\overline{\text{AACK}}$, which terminates the address bus tenure, the MPC185 negates $\overline{\text{ABB}}$ for a fraction of a bus cycle and then stops driving this signal.
AP[0:3]	C6, C1, D3, G3	I/O	Address parity—The 60x master that drives the address bus also drives the address parity signals. The value driven on address parity signal should give odd parity (odd number of ones) on the group of signals that it represents.
$\overline{\text{ARTRY}}$	P9	I	60x address retry—Assertion of this signal indicates that the bus transaction should be retried by the 60x bus master.
BASE[0:4]	C15, C14, C13, A14, C12	I	Base address select—These 5 bits set the initial base address for the MPC185 and address the upper 5 bits of the 32-bit address range. After reset the base address may be reprogrammed anywhere in the address space via software. As an example, if BASE[0:4] = 00001, the initial base address for Talos is 0x0800_0000.
$\overline{\text{BG}}$	T10	I	60x bus grant—The external arbiter asserts this signal to grant 60x bus ownership to the MPC185.
$\overline{\text{BR}}$	B12	O	60x bus request—The MPC185 asserts this signal to request ownership of the 60x bus.
$\overline{\text{CI}}$	B13	O	Cache inhibit—Programmable signal which indicates whether the transaction should be cached or not. Assertion of $\overline{\text{CI}}$ indicates that the transaction should not be cached.

Table 2. Pin Descriptions (continued)

Signal Name	Pin Locations	Signal Type	Description
D[0:63]	H16, H15, J16, J15, J14, K16, K15, K14, L16, L15, M16, M15, M14, N16, N15, N14, P16, P15, R16, R15, R14, T16, T15, T14, P13, P12, R13, R12, R11, T13, T12, T11, T8, T7, T6, R8, R7, R6, P7, P6, T5, T4, T3, R5, R4, R3, P4, P3, T2, T1, R2, R1, P2, P1, N2, N1, M3, M2, M1, L3, L2, L1, K2, K1	I/O	60x data bus—In write transactions the 60x bus master drives the valid data on this bus. In read transactions the 60x slave drives the valid data on this bus.
$\overline{\text{DBB}}$	F14	O	60x data bus busy—The MPC185 asserts this signal for the duration of the data bus tenure. Following a $\overline{\text{TA}}$, which terminates the data bus tenure, the MPC185 negates DBB for a fraction of a bus cycle and then stops driving this signal.
DP[0:7]	H14, L14, P14, P11, P8, P5, N3, K3	I/O	60x data parity—The 60x agent that drives the data bus also drives the data parity signals. The value driven on data parity signal should give odd parity (odd number of ones) on the group of signals that it represents.
$\overline{\text{GBL}}$	B14	O	Global—Assertion of this signal by the 60x master indicates that the transfer is global and it should be snooped by caches in the system.
$\overline{\text{IRQ}}$	A15	O	Interrupt request—Interrupt signal that indicates that one of the modules has asserted its hardware interrupt to indicate that service is needed by the system.
$\overline{\text{LBCLAIM}}$	B11	O	Local bus claim—Indicates that the slave claims the transaction and is responsible for driving $\overline{\text{TA}}$ during the data tenure.
$\overline{\text{MDBG}}$	R10	I	60x data bus grant—The system arbiter asserts this signal to grant 60x data bus ownership to the MPC185.
$\overline{\text{RESET}}$	B15	I	Asynchronous reset—All registers are reset immediately. Upon release of $\overline{\text{RESET}}$, the MPC185 will automatically clear all locations in the internal general purpose RAM.
$\overline{\text{SDBG}}$	R9	I	Slave data bus grant—Indicates that the MPC107 has granted a 60x slave the data bus and that the slave can use the data bus to transfer data to the 60x processor.
$\overline{\text{TA}}$	T9	I/O	Transfer acknowledge—Indicates that a 60x data beat is valid on the data bus. For 60x single-beat transfers, assertion of this signal indicates the termination of the transfer. For 60x burst transfers, $\overline{\text{TA}}$ is asserted four times to indicate the transfer of four data beats, with the last assertion indicating the termination of the burst transfer.

Table 2. Pin Descriptions (continued)

Signal Name	Pin Locations	Signal Type	Description
$\overline{\text{TBST}}$	A10	I/O	60x bus transfer burst—The 60x bus master asserts this signal to indicate that the current transaction is a burst transaction (transfers four double words).
$\overline{\text{TEA}}$	A12	I/O	Transfer error acknowledge—Assertion of this signal indicates a bus error.
$\overline{\text{TS}}$	A11	I/O	60x bus transfer start—Assertion of this signal indicates the beginning of a new address bus tenure. The arbiter asserts this signal to a slave to begin an address tenure. When the arbiter senses this pin being asserted by an external 60x bus master, it will respond to the address bus tenure as required.
TSIZ[0:3]	A9, B9, C9, C8	I/O	60x transfer size—The 60x bus master drives these pins with a value indicating the quantity of bytes transferred in the current transaction.
TT[0:4]	A8, B8, A7, B7, C7	I/O	60x bus transfer type—The 60x bus master drives these pins during the address tenure to specify the type of the transaction.
$\overline{\text{WT}}$	A13	O	Write through—The state of this pin indicates whether the transaction should be cached using write-through or copy-back mode. Assertion of $\overline{\text{WT}}$ indicates that the transaction should be cached using the write-through mode.
Miscellaneous Signals			
XLBCLKMODE	D14	I	60X local bus clock mode—This input should be tied high if the external CPU has a core clock to system clock ratio of 2:1 or higher. It should be tied low if the ratio is 1:1 or 1.5:1.
XLBMODE	D15	I	60X local bus mode—This input should be tied high when the MPC185 is connected to an MPC8260 or Harrier and low when connected to an MPC107.
SE	E15	I	Scan enable—For manufacturing test only. This input should always be tied low.
PLL Range	F15	I	PLL range 0 (OVSS) = 66–100 MHz PLL band 1 (OVDD) = 33–66 MHz PLL band If operating slower than 33 MHz, the PLL must be disabled using the PLL bypass pin (D11).
PLL Bypass	D11	I	PLL Bypass 0 (OVSS) = PLL disabled 1 (OVDD) = PLL enabled
CLK	F16	I	System clock
TPA	G15	O	Test pad analog—This pin must have no connection
TCK	A16	I	Test Clock—If JTAG is not used, this pin should be tied to VSS.
$\overline{\text{TRST}}$	B16	I	Test Reset—If JTAG is not used, this pin should be tied to VSS.
TMS	C16	I	Test Mode Select—If JTAG is not used, this pin should be tied to OVDD.
TDI	D16	I	Test Input—If JTAG is not used, this pin should be tied to OVDD.
TDO	E16	O	Test output—If JTAG is not used, this pin should be NC.

Table 2. Pin Descriptions (continued)

Signal Name	Pin Locations	Signal Type	Description
NC	C11, E14, P10		No connection
Powers and Grounds			
OVDD 3.3 V, 2.5 V	D4, E4, F4, G4, H4, J4, K4, L4, M4, N4, N5, N6, N7, N8, N9, N10, N11, N12, N13, M13, L13, K13, J13, H13, G13, F13, E13, D13, D12, D10, D9, D8, D7, D6, D5	I	I/O supply voltage
IVDD 1.5 V	E5, F5, G5, H5, J5, K5, L5, M5, M6, M7, M8, M9, M10, M11, M12, L12, K12, J12, H12, G12, F12, E12, E11, E10, E9, E8, E7, E6	I	Core voltage
VSS GND	F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11	I	Ground
AVDD	G16	I	Analog PLL supply voltage (+1.5 V)
AVSS	G14	I	Analog PLL ground

5 Pin Connections

Table 3 shows pin connections to the MPC8260 and MPC107.

Table 3. Pin Connections

Signal Name	Pin Locations	MPC8260 Connection	MPC107 Connection
60x Signals			
A[0:31]	A6, A5, A4, B6, B5, B4, C5, C4, A3, A2, A1, B3, B2, B1, C3, C2, D2, D1, E3, E2, E1, F3, F2, F1, G2, G1, H3, H2, H1, J3, J2, J1	A[0:31]	A[0:31]
$\overline{\text{AACK}}$	B10	$\overline{\text{AACK}}$	$\overline{\text{AACK}}$
$\overline{\text{ABB}}$	C10	$\overline{\text{ABB}}$	NC
AP[0:3]	C6, C1, D3, G3	AP[0:3]	Pull up to OVDD or pull down to VSS
$\overline{\text{ARTRY}}$	P9	$\overline{\text{ARTRY}}$	$\overline{\text{ARTRY}}$
BASE[0:4]	C15, C14, C13, A14, C12	Implementation-specific	Implementation-specific
$\overline{\text{BG}}$	T10	$\overline{\text{BG}}$, $\overline{\text{EXT\_BG2}}$, $\overline{\text{EXT\_BG3}}$	$\overline{\text{BG\_0}}$, $\overline{\text{BG\_1}}$
$\overline{\text{BR}}$	B12	$\overline{\text{BR}}$, $\overline{\text{EXT\_BR2}}$, $\overline{\text{EXT\_BR3}}$	$\overline{\text{BR\_0}}$, $\overline{\text{BR\_1}}$
$\overline{\text{CI}}$	B13	If $\overline{\text{CI}}$ is not used, this pin should be tied to OVDD	
D[0:63]	H16, H15, J16, J15, J14, K16, K15, K14, L16, L15, M16, M15, M14, N16, N15, N14, P16, P15, R16, R15, R14, T16, T15, T14, P13, P12, R13, R12, R11, T13, T12, T11, T8, T7,. T6, R8, R7, R6, P7, P6, T5, T4, T3, R5, R4, R3, P4, P3, T2, T1, R2, R1, P2, P1, N2, N1, M3, M2, M1, L3, L2, L1, K2, K1	D[0:63]	D[0:63]
$\overline{\text{DBB}}$	F14	$\overline{\text{DBB}}$	NC
DP[0:7]	H14, L14, P14, P11, P8, P5, N3, K3	DP[0:7]	DP[0:7]
$\overline{\text{GBL}}$	B14	$\overline{\text{GBL}}$	$\overline{\text{GBL}}$
$\overline{\text{IRQ}}$	A15	$\overline{\text{IRQ\_}x}$	$\overline{\text{IRQ\_}x}$
$\overline{\text{LBCLAIM}}$	B11	NC	$\overline{\text{LBCLAIM}}$
$\overline{\text{MDBG}}$	R10	$\overline{\text{DBG}}$, $\overline{\text{EXT\_DBG2}}$, $\overline{\text{EXT\_DBG3}}$	$\overline{\text{DBG\_0}}$, $\overline{\text{DBG\_1}}$
$\overline{\text{RESET}}$	B15	Implementation-specific	
$\overline{\text{SDBG}}$	R9	$\overline{\text{CPU\_DBG}}$	$\overline{\text{DBG\_LB}}$
$\overline{\text{TA}}$	T9	$\overline{\text{TA}}$	$\overline{\text{TA}}$
$\overline{\text{TBST}}$	A10	$\overline{\text{TBST}}$	$\overline{\text{TBST}}$
$\overline{\text{TEA}}$	A12	$\overline{\text{TEA}}$	$\overline{\text{TEA}}$

Table 3. Pin Connections

Signal Name	Pin Locations	MPC8260 Connection	MPC107 Connection
$\overline{TS}$	A11	$\overline{TS}$	$\overline{TS}$
TSIZ[0:3]	A9, B9, C9, C8	TSIZ[0:3]	VSS, TSIZ[0:2]
TT[0:4]	A8, B8, A7, B7, C7	TT[0:4]	TT[0:4]
$\overline{WT}$	A13	If $\overline{WT}$ is not used, this pin should be tied to OVDD	
Miscellaneous Signals			
XLBCLKMODE	D14	This input should be tied high if the external CPU has a core clock to system clock ratio of 2:1 or higher and low if the ratio is 1:1 or 1.5:1	
XLBMODE	D15	This input should be tied high when the MPC185 is connected to an MPC8260 or Harrier and low when connected to an MPC107	
SE	E15	This pin should be tied to VSS	
PLL Range	F15	PLL range 0 (OVSS) = 66–100 MHz PLL band 1 (OVDD) = 33–66 MHz PLL band If operating slower than 33 MHz, the PLL must be disabled using the PLL bypass pin (D11).	
PLL Bypass	D11	PLL Bypass 0 (OVSS) = PLL disabled 1 (OVDD) = PLL enabled	
CLK	F16	Implementation-specific	
TPA	G15	This pin must have no connection	
TCK	A16	If JTAG is not used, this pin should be tied to VSS	
$\overline{TRST}$	B16	If JTAG is not used, this pin should be tied to VSS	
TMS	C16	If JTAG is not used, this pin should be tied to OVDD	
TDI	D16	If JTAG is not used, this pin should be tied to OVDD	
TDO	E16	If JTAG is not used, this pin should be NC	
NC	C11, E14, P10		
Powers and Grounds			
3.3 V, 2.5 V	D4, E4, F4, G4, H4, J4, K4, L4, M4, N4, N5, N6, N7, N8, N9, N10, N11, N12, N13, M13, L13, K13, J13, H13, G13, F13, E13, D13, D12, D10, D9, D8, D7, D6, D5		
1.5 V	E5, F5, G5, H5, J5, K5, L5, M5, M6, M7, M8, M9, M10, M11, M12, L12, K12, J12, H12, G12, F12, E12, E11, E10, E9, E8, E7, E6		
GND	F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11		
AVDD	G16 (+1.5 V)		
AVSS	G14		

1. The MPC107 has only 3 TSIZ pins, TSIZ[0:2]. These pins map to the MPC185 pins TSIZ[1:3], while TSIZ[0] on the MPC185 must be grounded.

6 Electrical and Thermal Characteristics

The electrical and thermal characteristics are addressed in this section. Topics include the absolute maximum ratings, package thermal characteristics, operating conditions and DC electrical characteristics, AC timing characteristics, and IEEE 1149.1 AC timing specifications.

6.1 Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Characteristic	Name	Absolute Min	Absolute Max	Unit
Power supply voltage—core	V_{DD}	–0.5	+2.0	V
Power supply voltage—I/O	V_{DDQ}	–0.5	+4.1	V
Storage temperature	—	–55	+125	°C
Static input pin voltage	—	–0.5	+4.1	V

Note: V_{DDQ} must not exceed V_{DD} by more than 2.2 V at any time.

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

6.2 Package Thermal Characteristics

Table 5 shows the thermal resistances for the 256-pin MBGA package.

Table 5. Package Thermal Characteristics

Rating		Symbol	Max	Unit	Notes
Junction-to-ambient (@ 200 ft/min)	Single–layer board Four–layer board	R	40 25	°C/W	1, 2
Junction-to-board (bottom)		R	17	°C/W	3
Junction-to-case (top)		R	9	°C/W	4

Notes:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, board population, and board thermal resistance.
2. Per SEMI G38-87
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC-883 Method 1012.1).

6.3 Operating Conditions and DC Electrical Characteristics

Table 6 shows the operating conditions and DC electrical characteristics of the MPC185.

Table 6. Electrical Operating Conditions

Characteristic	Name	Min	Typ	Max	Unit	Notes
Power supply voltage—core	V_{DD}	1.35	—	1.65	V	
Power supply voltage—I/O	V_{DDQ}	2.3	—	3.6	V	
Input low voltage (V_{DD} = Min)	V_{IL}	–0.3	—	0.8	V	1
Input high voltage (V_{DD} = Max)	V_{IH}	1.8	—	V_{DDQ} + 0.3	V	2
AC supply current (I/O power not included)	I_{DD}	—	—	600	mA	
Standby supply current	I_{SS}	—	—	250	mA	
Input leakage current @ $V_{DD} \geq V_{in} \geq V_{SS}$	I_{leak}	—	—	±5	µA	
Three-state input current @ $V_{DD} \geq V_{in} \geq V_{SS}$	I_Z	—	—	10	µA	

Notes:
1. Undershoot: $V_{IL} \leq -1.5$ V for $t < 20\%\ t_{KHKH}$.
2. Overshoot: $V_{IH} \leq V_{DD} + 1.0$ V (not to exceed 4.6 V) for $t < 20\%\ t_{KHKH}$.

6.4 AC Timing Characteristics

Table 7 shows the AC timing specifications for use with a PowerQUICC II. All timings assume a 40-pF load.

Table 7. AC Electrical Characteristics - PowerQUICC II

Condition	Name	Min	Max	Unit
Clock frequency	F_{clock}	—	83	MHz
Clock cycle time	t_{KHKH}	12	—	nS
Clock-to-signal valid delay	t_{KHQV}	—	5.5	nS
Clock-to-signal hold	t_{KHQX}	1.3	—	
Input setup time to clock-bused signals	t_{DVKH}	2.4	—	nS
Input hold time clock	t_{KHDX}	0.3	—	nS

Table 8 shows the AC timing specifications for use with an MPC107 or other 60x bridge/memory controller. All timings assume a 15-pF load.

Table 8. AC Electrical Characteristics - 60x Bridge/Memory Controller

Condition	Name	Min	Max	Unit
Clock frequency	F_{clock}	—	100	MHz
Clock cycle time	t_{KHKH}	10	—	nS
Clock-to-signal valid delay	t_{KHQV}	—	4.35	nS
Clock-to-signal hold	t_{KHQX}	0.7	—	
Input setup time to clock-bused signals	t_{DVKH}	2.0	—	nS
Input hold time clock	t_{KHDX}	0.1	—	nS

6.5 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 9 shows the IEEE 1149.1 AC timing specifications for the MPC185.

Table 9. IEEE 1149.1 (JTAG) AC Timing Specifications

Condition	Name	Min	Max	Unit
TCK cycle time	t_{THTH}	60	—	nS
TCK clock high time	t_{TH}	25	—	nS
TCK clock low time	t_{TL}	25	—	nS
TDO access time	t_{TLQV}	1	10	nS
$\overline{\text{TRST}}$ pulse width	t_{TSRT}	40	—	nS
Setup times capture TDI TMS	t_{CS} t_{DVTH} t_{MVTH}	5 5 5	—	nS
Hold times capture TDI TMS	t_{CH} t_{THDX} t_{THMX}	13 14 14	—	nS

7 Package Description

The following sections provide the package parameters and mechanical dimensions.

7.1 Case Outline Package Dimensions

Figure 3 and Figure 4 show the case outline package dimensions.

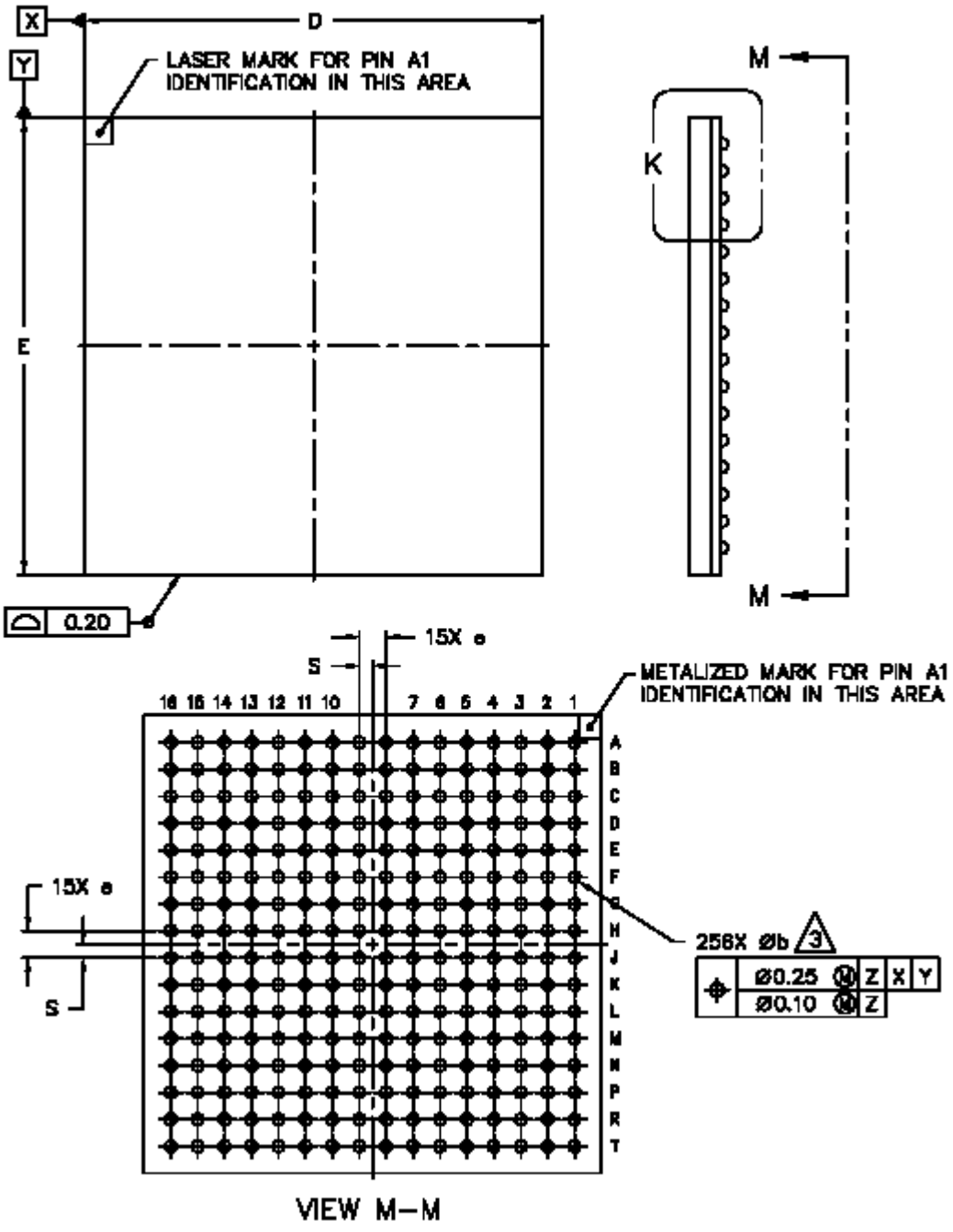
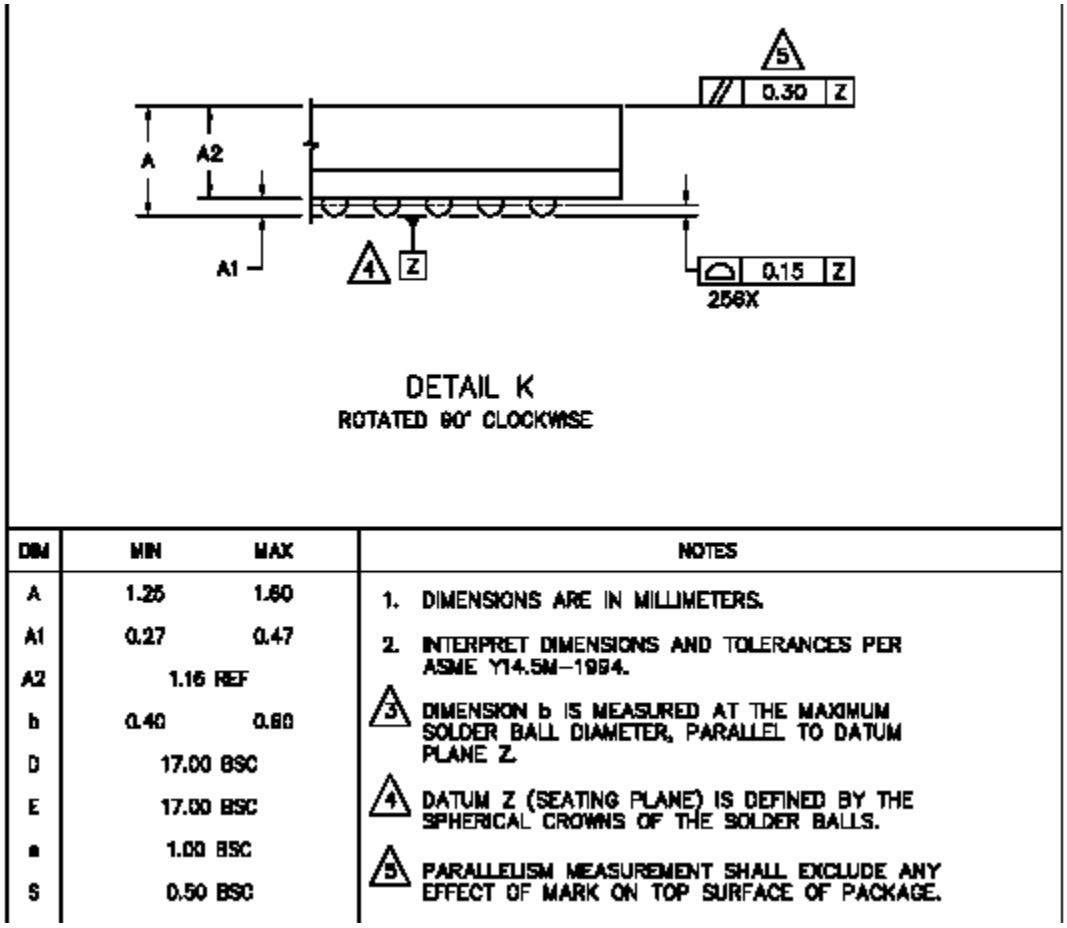


Figure 3. Case Dimensions



DIM	MIN	MAX
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

NOTES

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 4. Details of Case Dimensions

8 Document Revision History

Table 10 provides a revision history for this hardware specification.

Table 10. Document Revision History

Rev. No.	Substantive Change(s)
2.1	Updated Table 2 to show active low signals.
2.2	Nontechnical reformatting.
2.3	Nontechnical reformatting.

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