WITH

MPC8266ADS - PCI - AI

User's Manual

Revision PILOT

MOTOROLA
Semiconductor Products Sector

Chapter 1 General Information

1.1 Introduction

This document is an operation guide for the PQ2PCIAI-ADS board. It contains operational, functional and general information about the MPC8266ADS-PCI-AI. This board is meant to serve as a platform for s/w and h/w development around the MPC8266 processor. Using its on-board resources and a debugger, a developer is able to download code, run it, set breakpoints, display memory and registers and connect proprietary h/w via the expansion connectors, to be incorporated into a desired system with the MPC8266 processor.

This board could also be used as a demonstration tool (i.e., application s/w may be programmed[1] into its Flash memory and ran in exhibitions etc.).

1.2 Abbreviation List

- ADS - the MPC8266ADS-PCI-AI, the subject of this document.
- UPM - User Programmable Machine
- GPCM - General Purpose Chip-select Machine
- GPL - General Purpose Line (associated with a UPM)
- BSCR - Board Control & Status Register.
- BGA - Ball Grid Array
- T/ECOM - T1 or E1 Communication Tool, attachable to this board, via expansion connectors.

1.3 Related Documentation

- MPC8266 PowerQUICC II™ User's Manual
- PCI Local Bus Specification
- PICMG Hot Swap Specification
- PMC-SIERRA[2] 5350 Long Form Data Sheet
- PMC-SIERRA 5350 Errata Notice
- PMC-SIERA 5350 Reference Design
- PMC-SIERA 5350 Reference Design Errata
- LXT970A (by Level One) Data Sheet (http://www.level1.com/product/quickref.html#network)
- LXT970 Demo Board User's Guide (http://www.level1.com/product/quickref.html#network)

[1] Either on or off-board.
[2] Access to documents in this site requires registration.

1.4 Specifications

The MPC8266ADS-PCI-AI specifications are given in Table 1-1 ". MPC8266ADS-PCI-AI Specifications" below

Table 1-1. MPC8266ADS-PCI-AI Specifications

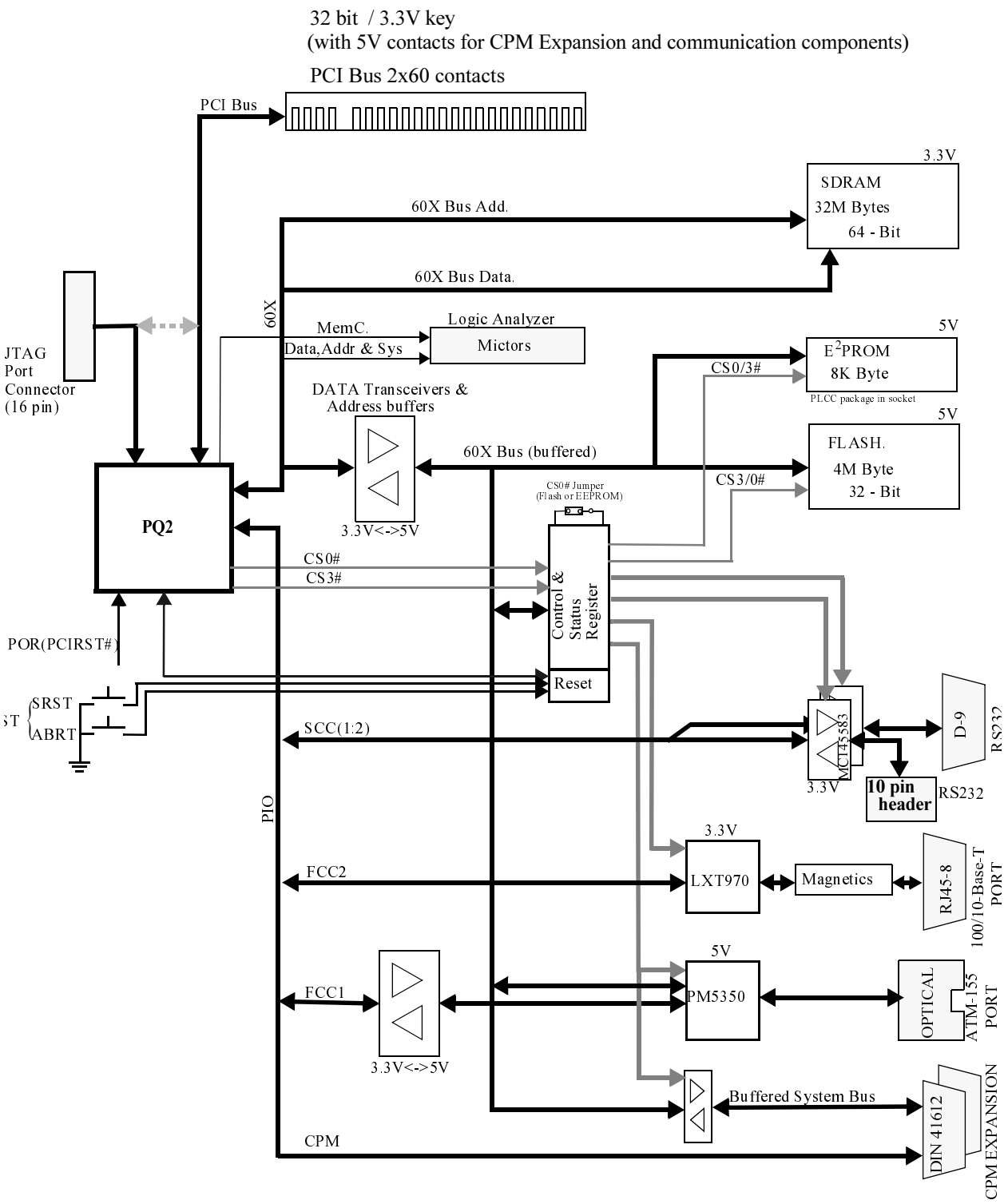
CHARACTERISTICS	SPECIFICATIONS
Power requirements (no other boards attached)	+3.3Vdc @ TBD A (Typ.), 5 A (Max.) +5Vdc @ TBD A (Typ.), 3.5 A (Max.) +12Vdc - @0.5A Max.
Microprocessor	MPC8266 running @ 66 MHz Bus Clock Frequency.
Addressing Total address range on PPC Bus: Flash Memory (PPC Bus) EEPROM Memory (PPC Bus) Synchronous Dynamic RAM (PPC Bus)	 4 Giga Bytes (32 address lines) 4 MByte, 32 bits wide. 8 KByte, 8 bit wide. 32MByte, 64 bits wide.
Operating temperature	10^{O}C - 30^{O}C (room temperature)
Storage temperature	-25^{O}C to 85^{O}C
Relative humidity	5% to 90% (non-condensing)
Dimensions: Length Width Thickness	 12.283" (312 mm) 4.2" (106.68 mm) 0.063" (1.6 mm)

1.5 ADS Features

- 64-bit MPC8266, running @ 66MHz external bus frequency.
- 32 MByte, Unbuffered, Synchronous Dram, residing on 60X bus, controlled by SDRAM machine 1.
- 4 MByte, Flash, buffered from 60X bus. Controlled by GPCM, 5V Programmable.
- 8 KByte, EEPROM, buffered from 60X bus. Controlled by GPCM, 5V Programmable.
- Jumper selectable configuration and boot source (EEPROM or Flash memory).
- Board Control & Status Register - BCSR, Controlling Board's Operation.
- Programmable Power-On-Reset and Hard Reset Configurations via Flash or EEPROM-memory.
- Module Enable Indications for all on-board communication modules.
- High density (MICTOR) Logic Analyzer connectors, for fast logic analyzer connection.
- 155 Mbps ATM UNI on FCC1 with Optical I/f, connected to the MPC8266 via UTOPIA I/F, using the PMC-SIERA 5350.
- 10/100-Base-T Port on FCC2 with T.P. I/F, MII controlled, using Level-One LXT970.
- Dual RS232 port residing on SCC1 & SCC2.
- Module disable (i.e., low-power mode) option for all communication transceivers -BCSR controlled, enabling use of communication ports, off-board via expansion connectors.
- Dedicated MPC8266's communication ports expansion connectors for convenient tools' connection, carrying also necessary bus signals, for transceivers' M/P I/F connection. Use is done with 2 X 128 pin DIN 41612 receptacle connectors.
- External Tools' Identification & status read Capability, via BCSR.
- Soft / Hard[1] Reset Push - Button
- ABORT Push - Button
- Dual-Option MPC8266 Internal Logic supply. Ranges include 1.8V or 2.5V.
- Software Option Switch provides 8 S/W options via BCSR.

[1]Hard reset is applied by depressing BOTH Soft Reset & ABORT buttons.

Figure 1-1. MPC8266ADS-PCI-AI Block Diagram



Chapter 2 Hardware Preparation and Installation

2.1 Introduction

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the PQ2PCIAI-ADS.

2.2 Unpacking Instructions

NOTE

If the shipping carton is damaged upon receipt, request carrier's agent to be present during unpacking and inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of equipment.

CAUTION

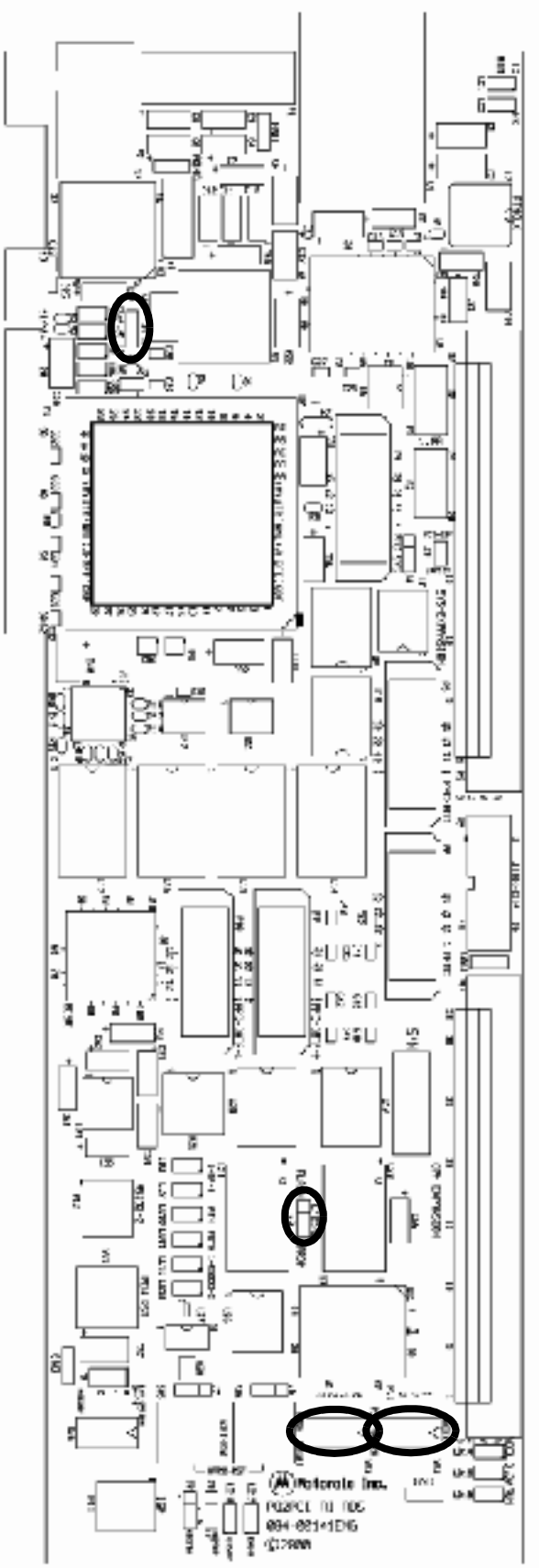
AVOID TOUCHING AREAS OF INTEGRATED CIRCUITRY; STATIC DISCHARGE CAN DAMAGE CIRCUITS.

2.3 Hardware Preparation

To select the desired configuration and ensure proper operation of the MPC8266ADS-PCI-AI board, changes of the Dip-Switch settings may be required before installation. The location of the switches, indicators, Dip-Switches, and connectors is illustrated in Figure 2-1 ". MPC8266ADS-PCI-AI Top Side Part Location Diagram" on page 16. The board has been factory tested and is shipped with Dip-Switch settings as described in the following paragraphs. Parameters can be changed for the following conditions:

- MPC8266's Internal Logic Supply Level (VDDL) Via J1.
- MPC8266's MODCK(1:3). Determining Core's and CPM's PLLs multiplication factor via SW2.
- MPC8266's PCIMODCKH(0:3). Determining PCI PLLs multiplication factor via SW3.
- MPC8266's HARD Reset Configuration Source via J5.

Figure 2-1. MPC8266ADS-PCI-AI Top Side Part Location Diagram

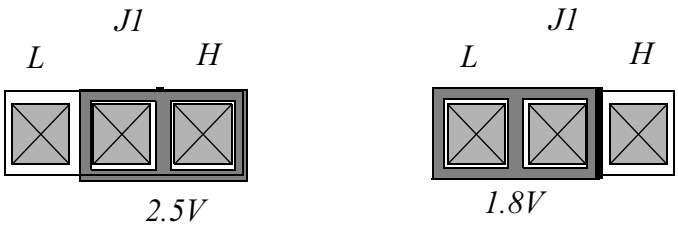


2.3.1 Setting VDDL Level - J1

To support future revisions of the MPC8266, provisions are taken to provide necessary voltage levels on VDDL, to match the process by which the MPC8266 is manufactured. Via J1, two voltage level ranges are provided:

1) When a jumper is placed between positions **1 - 2** of J1, a level of **1.8V** on VDDL is selected.
2) When a jumper is placed between positions **2 - 3** of J1, a level of **2.5V** on VDDL is selected.

Figure 2-2. VDDL Level Selection - J1



WARNING

J1 is Factory Set according to the revision of MPC8266 with which it is assembled. Prior to changing a MPC8266 device, Extra Care should be taken with J1 setup. If a selected Voltage Range is above the specification for the newly inserted MPC8266, PERMANENT DAMAGE might be inflicted to the MPC8266.

2.3.2 Setting MODCK(1:3) for PLLs Multiplication Factor - SW2(#1 - #3)

After (1K cycles) the negation of the Power On Reset signal, the MPC8266 samples the 7 MODCK lines - the lower 3 on MODCK(1-3) and the upper four - MODCKH(0:3) field, is read from the Hard-Reset configuration source, to establish the multiplication factors of the CPM's and Core's PLLs. The levels on **MODCK(1:3)** lines are set using **SW2**, switches **#1 - #3**. When an individual switch is at the **OFF** position its associated MODCK line is pulled-**high** ('1'), while when at the ***ON*** position, the associated MODCK is pulled-***down*** ('0'). SW2 is shown in Figure 2-3 ". SW2 Description" on page 18, while the various combinations for SW2 #1 - #3 and their associated MODCK(1:3) values are shown in Table 2-1 ". MODCK(1:3) Encoding" on page 18.

2.3.3 Setting PCIMODCK - SW2(#4)

The settings of this line, corresponds to the frequency of the PCI bus. When PCI_MODCK is set low, the PLL takes the PCI bus frequency as is. When set high, the PLL divides the PCI bus frequency by two. When an SW2-4 switch is at the **OFF** position, PCI-MODCK line is pulled-**high** ('1'), while when at the ***ON*** position, the PCI-MODCK line is pulled-***down*** ('0'). SW2 is shown in Figure 2-3 ". SW2 Description" on page 18.

Figure 2-3. SW2 Description

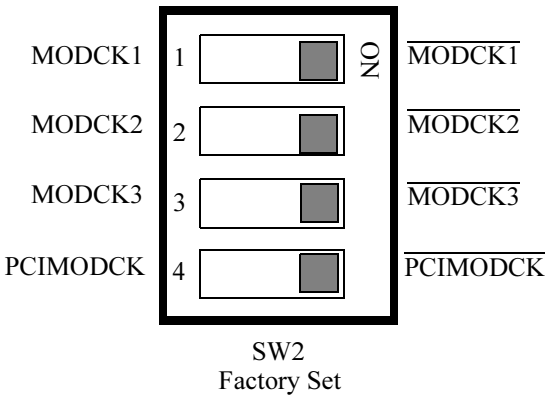


Table 2-1. MODCK(1:3) Encoding

MODCK(1:3)	Switch 1	Switch 2	Switch 3
0	ON	ON	ON
1	ON	ON	OFF
2	ON	OFF	ON
3	ON	OFF	OFF
4	OFF	ON	ON
5	OFF	ON	OFF
6	OFF	OFF	ON
7	OFF	OFF	OFF

2.3.4 Setting Hard - Reset Configuration Source

The Hard - Reset configuration word[1], read by the MPC8266 while HRESET~ is asserted, may be taken from two sources:

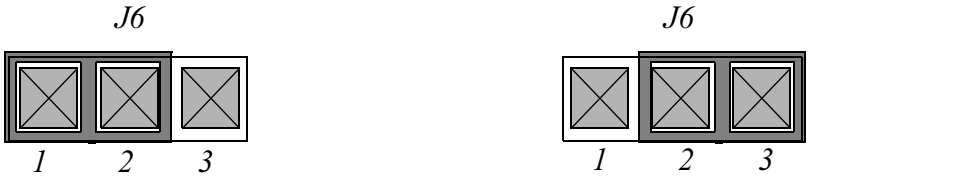
1) Flash Memory
2) EEPROM

For additional information as for the contents of the Hard-Reset configuration word see 4.1.2.4 "Hard Rest Configuration" on page 36.

1) When a jumper is placed between positions **1 - 2** of J6, the Hard Reset configuration word is taken from the ***Flash***.
2) When a jumper is placed between positions **2 - 3** of J6, the Hard Reset configuration word is taken from the ***EEPROM***.

[1]In fact 8 Hard-Reset configuration words are read by a configuration master, however only the first is relevant for a single MPC8266.

Figure 2-4. J6 - Configuration Source Selection



Flash as Configuration Source

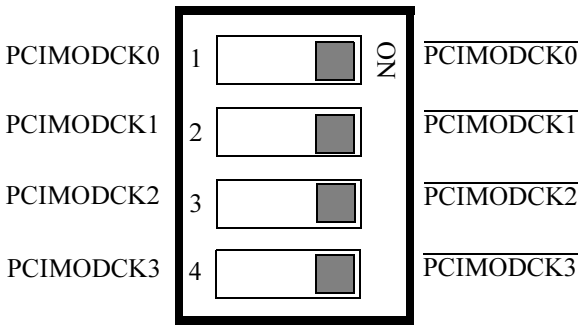
EEPROM as Configuration Source

Factory Setup

2.3.5 Setting PCIMODCKH(0:3) - for PCI PLLs Multiplication Factors - SW3

When an individual switch of SW3 is at the OFF position, its corresponding PCIMODCKH line is pulled-**high** (‘1’) , while when at the ***ON*** position, pulled-***down*** (‘0’).

Figure 2-5. SW3 Description



SW3

Factory Set

Table 2-2. PCIMODCKH(0:3) Encoding (TBD)

MODCK(0:3)	Switch 1	Switch 2	Switch 3	Switch 4
0	ON	ON	ON	ON
1	ON	ON	OFF	OFF
2	ON	OFF	ON	ON
3	ON	OFF	OFF	OFF
4	OFF	ON	ON	ON
5	OFF	ON	OFF	OFF
6	OFF	OFF	ON	ON
7	OFF	OFF	OFF	OFF

2.4 Installation Instructions

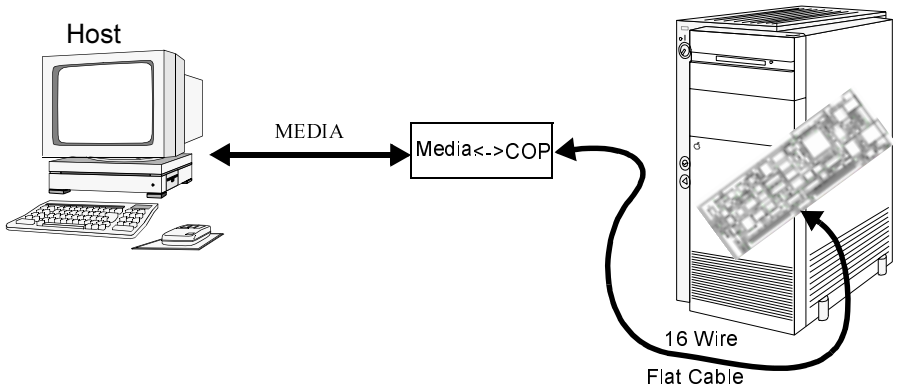
When the MPC8266ADS-PCI-AI has been configured as desired by the user, it can be installed according to the required working environment as follows:

- Host Controlled Operation
- Stand-Alone

2.4.1 Host Controlled Operation

In this configuration the MPC8266ADS-PCI-AI is controlled by a host computer via the COP port, which is a subset of the JTAG port. This configuration allows for extensive debugging using on-host debugger. The host is connected to the ADS by a COP controller provided by a third party.

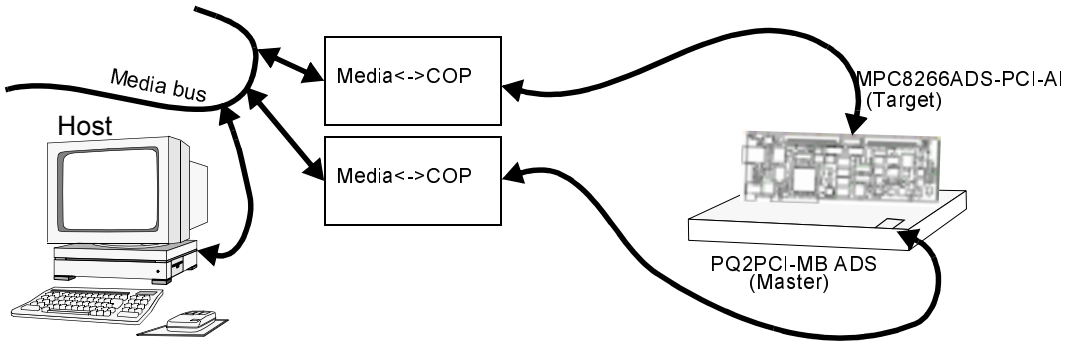
Figure 2-6. Host Controlled Operation Scheme



2.4.2 MPC8266 Master Controlled

In this mode the MPC8266ADS-PCI-AI is controlled by another MPC8266 via the PCI bus. It connects to the MPC8266ADS-PCI which is a motherboard platform, based on the MPC8266, for plugging in PCI cards. In this configuration the PCI Master (On the Motherboard) can be controlled via its COP interface and the Target board (MPC8266ADS-PCI-AI) can be controlled via its COP port or through the PCI bus.

Figure 2-7. MPC8266 Master Controlled

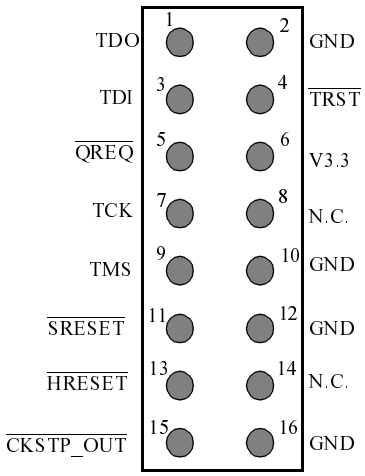


2.4.3 COP/JTAG Connector - P7

The MPC8266ADS-PCI-AI COP interface connector, P7, is a 16 pin, male, Header connector. The connection between the MPC8266ADS-PCI-AI and the COP controller is by a 16 line flat cable, supplied with the COP controller board obtained from a third party developer. Figure 2-8 ". P7 - COP/JTAG Port Connector" below shows the pin configuration of the connector.

An option exists on the ADS for connecting the COP/JTAG signals to the PCI connector according to the PCI standard. To enable this feature a hardware change should be made involving the removal and assembly of 0 ohm resistors on the ADS.

Figure 2-8. P7 - COP/JTAG Port Connector

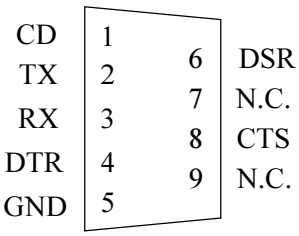


2.4.4 Terminal to MPC8266ADS-PCI-AI RS-232 Connection

A serial (RS232) terminal or any other RS232 equipment, may be connected to the RS-232 connectors P1 and P12. P1 is a 9 pin, female, D-type connector and P12 is a 10 pin, male, Header connector. **P1** is connected to SCC1 of the MPC8266 and ***P12*** *is* connected to SCC2 of the MPC8266.

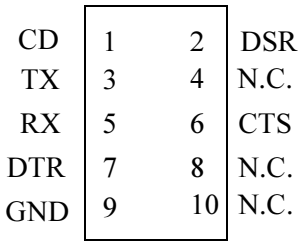
The connectors are arranged in a manner that allows for 1:1 connection with the serial port of an IBM-AT[1] or compatibles, i.e. via a flat cable. The pinout for P1 is shown in Figure 2-9 ". P1 - RS-232 Serial Port Connector" on page 21 and for P12 is shown in Figure 2-10 ". P12 - RS-232 Serial Port Connector" on page 22.

Figure 2-9. P1 - RS-232 Serial Port Connector



[1]IBM-AT is a trademark of International Business Machines Inc.

Figure 2-10. P12 - RS-232 Serial Port Connector



2.4.5 10/100-Base-T Ethernet Port Connection

The 10/100-Base-T port connector - P2, is an 8-pin, 90^{0}, receptacle RJ45 connector. The connection between the 10/100-Base-T port to the network is done by a standard cable, having two RJ45/8 jacks on its ends. The pinout of P2 is described in Table 5-2 ". P2 - Ethernet Port Interconnect Signals" on page 59.

Chapter 3 Operating Instructions

3.1 Introduction

This chapter provides necessary information to use the MPC8266ADS-PCI-AI in host-controlled and MPC8266 Master Controlled configurations. This includes controls and indicators, memory map details, and software initialization of the board.

3.2 Controls and Indicators

The PQ2PCIAI-ADS has the following switches and indicators.

3.2.1 ABORT Switch - SW4

The ABORT switch is normally used to abort program execution, this by issuing a level 0 interrupt to the MPC8266. It is the responsibility of the user to provide means of handling the interrupt, since there is no resident debugger with the PQ2PCIAI-ADS. The ABORT switch signal is debounced, and may be disabled by software.

3.2.2 SOFT RESET Switch - SW5

The SOFT RESET switch SW5 performs Soft reset to the MPC8266 internal modules, maintaining MPC8266's configuration (clocks & chip-selects) and SDRAMs' contents. The switch signal is debounced, and it is not possible to disable it by software.

3.2.3 HARD RESET - Switches - SW4 & SW5

When BOTH switches - SW4 and SW5 are depressed simultaneously, HARD reset is generated to the MPC8266. When the MPC8266 is HARD reset, all its configuration is lost[1], including data stored in the SDRAMs and the MPC8266 has to be re-initialized.

3.2.4 SW2 - MODCK Switch

SW2 is a 4-switch Dip-Switch. For its function see 2.3.2 "Setting MODCK(1:3) for PLLs Multiplication Factor - SW2(#1 - #3)" on page 17 and 2.3.3 "Setting PCIMODCK - SW2(#4)" on page 17.

3.2.5 SW3 - PCIMODCKH Switch

SW3 is a 4-switch Dip-Switch. For its function see 2.3.5 "Setting PCIMODCKH(0:3) - for PCI PLLs Multiplication Factors - SW3" on page 19.

3.2.6 SW6 - Software Options Switch and Hot-Swap Eject Switch

SW6 is a 4-switch Dip-Switch. This switch is connected over SWOPT(0:2) lines which are available at BCSR2, S/W options may be manually selected, according to SW6 state. SW6 is factory set to all ON. Switch #4 in SW6 function is for simulating the Hot-Swap Switch which is available in CompactPCI platforms that support the Hot-Swap function. When SW#4 is at the OFF position, the HotSwap Eject signal of the MPC8266 is pulled-**high** ('1') , while when at the ***ON*** position, it is pulled-***down*** ('0'). An external switch and debounce circuitry can be connected on **J11** described in Figure 3-2 ". J10 - HSEJSW Connector"

[1]Except for Hard-Reset configuration word, which is acquired only once, after PON-Reset.

below, for the purpose of simulating the Eject Switch present in CompactPCI systems.

Figure 3-1. SW6 - Description

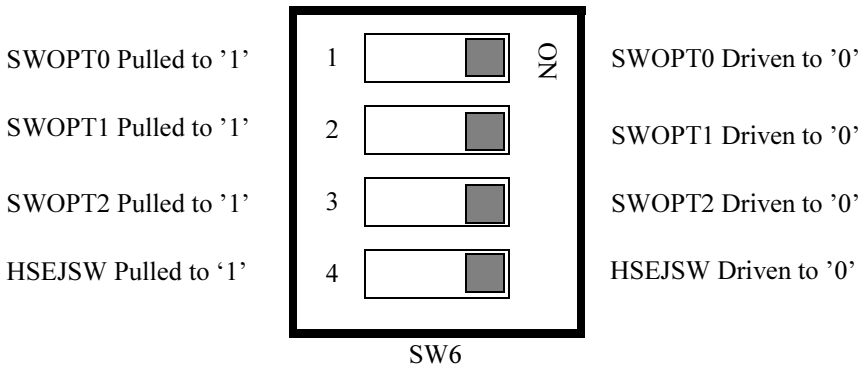
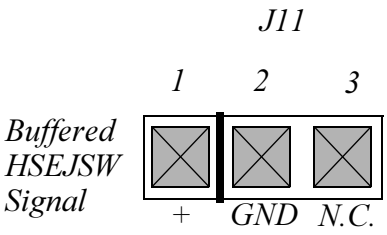


Figure 3-2. J11 - HSEJSW Connector



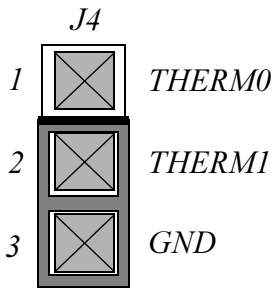
3.2.7 J1 - VDDL Voltage Level Selection

J1 selects between 2 different voltage levels available for VDDL. For further information over its function see 2.3.1 "Setting VDDL Level - J1" on page 17.

3.2.8 J4 - Thermal Sense Connector

There are 2 dedicated pins THERM(0:1) which provide a way to take internal temperature measurements of the MPC8266. These pins should be connected to GND for normal operation. J4 is factory set with a jumper on its 2 - 3 positions, so that THERM1 is connected to GND.

Figure 3-3. J4 - Therm Connector



3.2.9 J2 - Optional Fan Supply

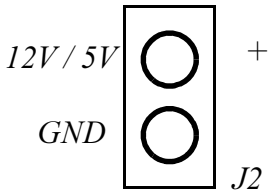
An optional cooling fan for the MPC8266 may be powered via J2, a 2 pin header connector. An option to connect the power supply source for the fan header to the 5V source is available, it is done by removing **R75** and soldering a 0 ohm resistor to **R4** instead. J2 is factory set to connect to the 12V supply voltage. In order to connect a fan to J2, a matching female connector is needed. J2 is shown in Figure 3-4 ". J2 - Fan Supply" below:

Warning

The job of soldering SMD resistors is very delicate and should be done by a skilled technician.

If this process is done by unskilled hands or repeated more than 3 times, permanent damage may occur to the PQ2PCIAI-ADS.

Figure 3-4. J2 - Fan Supply



3.2.10 J3 - 12V Source Enable

J3 enables the source for 12V programming voltage for an External tool. When a jumper is placed over J3, the PCI positive 12V source is connected to the 12V pins of the expansion connector, providing **12V VPP** to an external tool.

3.2.11 GND Bridges

There are 5 GND bridges on the PQ2PCIAI-ADS, 4, designated as GND reside on digital ground and 1, designated as AGND resides on analog ground plane. These bridges are meant to assist general measurements and logic-analyzer connection.

Warning

When connecting to a GND bridge, use only INSULATED GND clips. Otherwise, un-insulated clips may cause short- circuits, touching "HOT" points around them. Failure in doing so, might result in permanent damage to the PQ2PCIAI-ADS.

3.2.12 ATM TX Indicator - LD1

The green ATM Receive LED indicator blinks whenever the PM5350 ATM-UNI is transmitting cells via the ATM port. Illuminates only when the ATM transceiver is enabled via BCSR1.

3.2.13 ATM RX Indicator - LD2

The green ATM Receive LED indicator blinks whenever the PM5350 ATM-UNI is receiving cells via the ATM port. Illuminates only when the ATM transceiver is enabled via BCSR1.

3.2.14 Fast Ethernet CLSN Indicator - LD3

The red Ethernet Collision LED indicator CLSN, lights whenever a collision condition is detected on the 10/100-Base-T port, i.e., simultaneous receive and transmit. This led functions in this duty provided that bits 7:6) of LXT970's register 19, are cleared.

3.2.15 Ethernet LINK Indicator - LD4

The yellow Ethernet Twisted Pair Link Integrity LED indicator - LINK, lights to indicate good link integrity on the 10/100-Base-T port. LD4 is off when the link integrity fails.

3.2.16 Ethernet TX Indicator - LD5

The green Ethernet Receive LED indicator blinks whenever the LXT970 is transmitting data via the 10/100-Base-T port.

3.2.17 Ethernet RX Indicator - LD6

The green Ethernet Receive LED indicator blinks whenever the LXT970 is receiving data from the 10/100-Base-T port.

3.2.18 Fast Ethernet Indicator - LD7

When the LXT970 is enabled and is in 100 Mbps operation mode, the yellow led - LD7 lights.

3.2.19 General Purpose Indicator 1- LD8

This green indication led has no dedicated function over the ADS. It is meant to provide some visibility for program behavior. It is controlled by BCSR0.

3.2.20 General Purpose Indicator 2- LD9

This red indication led has no dedicated function over the ADS. It is meant to provide additional visibility for program behavior. Its different color from LD8 provides additional information. It is controlled by BCSR0.

3.2.21 ATM ON - LD10

When the yellow ATM ON led is lit, it indicates that the ATM-UNI transceiver - the PM5350, is enabled for communication. When it is dark, the ATM-UNI transceiver is disconnected from the MPC8266, enabling the use of its associated FCC1 pins off-board via the expansion connectors.

ATM ON led is controlled by BCSR1.

3.2.22 Fast Ethernet Port Initially Enabled - LD11

When the yellow ETH ON led is lit, it indicates that the fast ethernet port transceiver - the LXT970, is **initially** active. When it is dark, it indicates that the LXT970 is **initially** in power down mode, enabling the use of its associated FCC2 pins off-board via the expansion connectors. The state of LD11 is controlled by BCSR1.

This is a **soft**-indication, i.e., since the LXT970 may be controlled via the MII port, it is possible that the state of LD11 does not reflect correctly the status of the LXT970.

Note

Application S/W should always seek to match the state of LD11 to the status of the LXT970, so that, this indication is made reliable as to the correct status of the LXT970.

3.2.23 RS232 Port 1 ON - LD12

When the yellow RS232 Port 1 ON led is lit, it designates, that the RS232 transceiver connected to P1 (DB9 connector), is active and communication via that medium is allowed. When darkened, it designates that the transceiver is in shutdown mode and its associated SCC1 pins may be used off-board via the expansion connectors.

3.2.24 RS232 Port 2 ON - LD13

When the yellow RS232 Port 2 ON led is lit, it designates that the RS232 transceiver connected to P12 (10 pin Header connector) is active and communication via that medium is allowed. When darkened, it designates, that the transceiver is in shutdown mode and its associated SCC2 pins may be used off-board via the expansion connectors.

3.2.25 VDDL Indication - LD14

The green VDDL indicator led - LD14 is lit to indicate a VDDL power activity.

3.2.26 3.3V Indicator - LD15

The green 3.3V led - LD15, indicates the presence of the +3.3V supply on the ADS.

3.2.27 RUN Indicator - LD16

When the green RUN led - LD16 is lit, it indicates that the MPC8266 is performing cycles on the PPC Bus. When dark, the MPC8266 is either running internally or stuck.

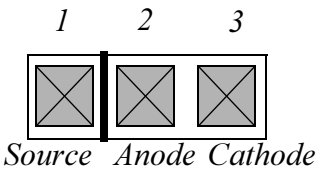
3.2.28 Hot Swap $\overline{\text{ENUM}}$ Indicator - LD17

When the yellow ENUM# led is lit, it indicates that the state of the MPC8266 ENUM# signal is in the logic low state. It is meant to provide visibility of the Hot-Swap state of the PCI bridge in the MPC8266.

3.2.29 Hot Swap “Blue Led” - LD18

This Blue led is available for conformance with the Hot-Swap standard. Its function is described in the PICMG Hot Swap Specification. A 3 pin header is provided, J10, as an option for connecting an external Led instead of the Blue Led of the ADS. This header connects to the Anode, Cathode and buffered HSLED source signal from the MPC8266 chip.

Figure 3-5. J10 - Blue Led Connector



3.3 Memory Map

All accesses to ADS's memory slaves are controlled by the MPC8266's memory controller. Therefore, the memory map is re programmable to the desire of the user. After Hard Reset is performed by the debug station, the debugger initializes the memory controller. The SDRAM and the Flash memory, respond to all types of memory access i.e., problem / supervisory, program / data and DMA. This memory map is a recommended memory map and since it is a "soft" map, devices' address may moved about the map, to the convenience of any user.

There are two possible memory maps available depending on **J5** setting. One map is in case the Flash is used as the boot memory and contain the reset configuration words. This map is shown in Table 3-1 ". ADS Memory Map (Flash as boot memory)" below. The second map shown in Table 3-2, ". ADS Memory Map (EEPROM as boot memory)," on page 31 is in case the user wishes to use the E^2PROM as the boot memory

and contain the reset configuration words.

Table 3-1. ADS Memory Map (**Flash as boot memory**)

ADDESS RANGE	*Memory Type*	*Device Name*	*Port Size*
00000000 - 01FFFFFF	SDRAM	Four MB81F641642D by Fujitsu (32 MByte)	64
02000000 - 03FFFFFF	Empty Space		-
04000000[1] - 04007FFF[2]	E^{2}PROM	28HC64 by Atmel (8 KByte)	8
04008000 - 044FFFFF	Empty Space		-
04500000 - 04507FFF	BCSR(0:3)[3]		32
04500000 - 04507FF3	BCSR0		
04500004 - 04507FF7	BCSR1		
04500008 - 04507FFB	BCSR2		
0450000C - 04507FFF	BCSR3 (Reserved)		
04508000 - 045FFFFF	Empty Space		-
04600000 - 04607FFF[4]	ATM UNI Proc. Control	PMC5350 M/P I/F	8
04608000 - 046FFFFF	Empty Space		-
04700000[5] - 04713FFF	MPC8266 Internal MAP[6]		32
04714000 - 7FFFFFFF	Empty Space	(Tool board is located at 60000000 and 70000000)	-
80000000 - EFFFFFFF	PCI Memory	PCI	32
F0000000 - FDFFFFFF	Empty Space		
FE000000[7] - FFBFFFFF	Reserved		
FFC00000 - FFFFFFFF	Flash	Two Am29F160DB (boot sector flash) by AMD (4 MByte)	32

[1]Memory capacity is 8 Kbytes but minimal CS~ region is 32Kbytes.

[2]The device appears repeatedly in multiples of its port-size.

[3]The device appears repeatedly in multiples of its port-size (in bytes) X depth. E.g., BCSR0 appears at memory locations 4700000, 4700010, 4700020..., while BCSR1 appears at 4700004, 4700014, 4700024... and so on.

[4]The internal space of the ATM UNI control port is 256 bytes, however, the minimal block size that may be controlled by a CS region is 32KBytes.

[5]Initially at h0F000000 - h0F013FFF, set by hard reset configuration.

[6]Refer to the MPC8266 User's Manual for complete description of the MPC8266's internal memory map.

[7]Set by Hard-Reset configuration.

Table 3-2. ADS Memory Map (**EEPROM as boot memory**)

ADDESS RANGE	*Memory Type*	*Device Name*	*Port Size*
00000000 - 01FFFFFF	SDRAM	Four MB81F641642D by Fujitsu (32 MByte)	64
02000000 - 03FFFFFF	Empty Space		-
04000000 - 043FFFFF	Flash	Two Am29F160DB (boot sector flash) by AMD (4 MByte)	32
04400000 - 044FFFFF	Empty Space		-
04500000 - 04507FFF	BCSR(0:3)[1]		32
04500000 - 04507FF3	BCSR0		
04500004 - 04507FF7	BCSR1		
04500008 - 04507FFB	BCSR2		
0450000C - 04507FFF	BCSR3 (Reserved)		
04508000 - 045FFFFF	Empty Space		-
04600000 - 04607FFF[2]	ATM UNI Proc. Control	PMC5350 M/P I/F	8
04608000 - 046FFFFF	Empty Space		-
04700000[3] - 04713FFF	MPC8266 Internal MAP[4]		32
04714000 - 7FFFFFFF	Empty Space	(Tool board is located at 60000000 and 70000000)	-
80000000 - EFFFFFFF	PCI Memory	PCI	32
F0000000 - FDFFFFFF	Empty Space		
FE000000[5] - FFFFBFFF	Empty Space		
FFF00000 - FFFFFFFF	EEPROM	28HC64 by Atmel (8 KByte)	8

[1]The device appears repeatedly in multiples of its port-size (in bytes) X depth. E.g., BCSR0 appears at memory locations 4700000, 4700010, 4700020..., while BCSR1 appears at 4700004, 4700014, 4700024... and so on.

[2]The internal space of the ATM UNI control port is 256 bytes, however, the minimal block size that may be controlled by a CS region is 32KBytes.

[3]Initially at h0F000000 - h0F013FFF, set by hard reset configuration.

[4]Refer to the MPC8266 User's Manual for complete description of the MPC8266's internal memory map.

[5]Set by Hard-Reset configuration.

3.4 MPC8266 Register Programming

The MPC8266 provides the following functions on the MPC8266ADS-PCI-AI:

1) System functions which include:
   - PPC Bus SDRAM Controller
   - Chip Select generator.
2) Communication functions which include:
   - ATM SAR
   - Fast Ethernet controller.
   - UART for terminal or host computer connection.

The internal registers of the MPC8266 must be programmed after Hard reset as described in the following paragraphs. The addresses and programming values are in **Hexadecimal** base.

For more information on the following initializations, see the MPC8266 User's Manual.

3.4.1 System Initialization

Table 3-3 Power-On Reset Configuration[1]

Flash Address [hex]	Init Value[hex]	Description
0	0C (04[2])	Internal arbitration, Internal memory controller, Core enabled, Single MPC8266, 32 Bit boot port size (8 Bit boot port size)[2], Exceptions vectored to 0xFFF00000, Internal space 64 bit slave for external master.
8	32	L2 cache signals configured for L2 cache, DP(1:7) configured as L2 cache I/F and IRQ(6:7)~, Initial Internal space @ 0x0F000000
10	36	Boot memory space @ 0xFE000000 - 0xFFFFFFFF, $\overline{\text{ABB/IRQ2}}$ pin is $\overline{\text{ABB}}$, $\overline{\text{DBB/IRQ3}}$ pin is $\overline{\text{DBB}}$, Mask masters requests, Boot master is PCI, Local Bus pins function as PCI bus, AP(1:3) configured as BNKSEL(0:2), APE~ configured as IRQ7~ and CS11~ as CS11~.
18	40	CS10~ configured as BCTL1~

[1]Programmed into the Flash memory in addresses 0x0, 0x8, 0x10 & 0x18.

[2]Programmed into the EEPROM memory in addresses 0x0, 0x8, 0x10 & 0x18.

Table 3-4. SIU Register Programming

Register	Init Value[hex]	Description
RMR	0001	Check-Stop Reset enabled.
IMMR	04700000	Internal space @ 0x0470_0000
SYPCR	FFFFFFC3	Software watchdog timer count - FFFF, Bus-monitor timing FF, PPC Bus-monitor - Enabled, Local Bus-monitor - Enabled, S/W watch-dog - disabled, S/W watch-dog (if enabled) causes reset, S/W watch-dog (if enabled) - prescaled.
BCR	004C_0000	Single MPC8266 , 0 wait-states on address tenure, No L2 cache , 0 clock hit delay , 1-level Pipeline depth, Extended transfer mode Enabled for PPC bus, Extended Transfer mode Enabled for Local Bus, Odd parity for PPC & Local Buses (not relevant for this application), Internal space responds as 64 bit slave for external master (not relevant for this application).

3.4.2 Memory Controller Register Programming

The memory controller on the MPC8266ADS-PCI-AI is initialized to 66 MHz operation. I.e., register programming is based on 66 MHZ timing calculation. Table 3-5, “. Memory Controller Initializations For 66Mhz (Flash as Boot memory),” on page 34 is for a case when the Flash memory is used as the source for the Configuration and Boot code, in case the EEPROM is used for initialization (controlled by **J5**) a different

memory controller initialization is used.

Table 3-5. Memory Controller Initializations For 66Mhz (**Flash as Boot memory**)

Reg.	Device Type	Bus	Init Value [hex]	Description
BR0	AM29F160DB90EC AMD Flash (AT28HC64B-70JC 8 Kbyte ATMEL EEPROM)[1]	PPC	FFC01801 (FFF00801)[1]	Base at FFC00000, 32 bit port size, no parity, GPCM
OR0			FFC00836 (FFF00846)[1]	4MByte block size, CS early negate, 6 w.s., Timing relax
BR1	BCSR	PPC	04501801	Base at 04500000, 32 bit port size, no parity, GPCM
OR1			FFFF8010	32 KByte block size, all types access, 1 w.s.
BR2	MB81F641642D-102FN SDRAM by Fujitsu	PPC	00000041	Base at 0, 64 bit port size, no parity, Sdram machine 1
OR2			FE002CC0	32MByte block size, 4 banks per device, row starts at A9, 12 row lines, internal bank interleaving allowed, normal AACK operation
BR3	AT28HC64B-70JC 8 Kbyte ATMEL EEPROM (AM29F160DB90EC AMD Flash)[1]	PPC	04008801 (04001801)[1]	Base at 04000000, 8 bit port size, no parity, GPCM
OR3			FFFF0846 (FFC00836)[1]	32 Kbyte block size, 3 w.s., Timing relax
BR4	Reserved	-	-	
OR4			-	
BR5	PM5350 - ATM UNI	PPC	04600801	Base at 04600000, 8 bit port size, no parity, GPCM on PPC bus.
OR5			FFFF8E36	32K Byte block size, delayed CS assertion, early CS and WE negation for write cycle, relaxed timing, 7 w.s. for read, 8 for write, extended hold time after read.
PSDMR	MB81F641642D-102FN SDRAM	PPC Single MPC8266 Bus Mode	4049A452	**Bank** Based Interleaving, Refresh enabled, normal operation code, address muxing mode 1, A(14 - 16) on BNKSEL(0:2), A10 on PSDA10, 5 clocks refresh recovery, 2 clocks precharge to activate delay, 2 clocks activate to read/write delay, 4 beat burst length, 1 clock last data out to precharge, 1 clock write recovery time, no extra cycle on address phase, normal timing for control lines, 2 clocks CAS latency.
PSRT	PPC Bus SDRAM	PPC	E	Divide MPTPR output by 15 (PSRT +1) Generates refresh every 13.4 msec, while 16 msec required. Therefore is refresh redundancy of 5.4 msec throughout full SDRAM refresh cycle which completes in 54.9 msec. I.e., Application s/w may withhold the bus upto app. 9.1 msec in a 64 msec period, without jeopardizing the contents of the ppc bus SDRAM.
MPTPR	SDRAM on board		3B	Divide Bus clock by 59 (MPTPR) (decimal)

[1]When EEPROM is set as Boot memory.

Chapter 4 Functional Description

In this chapter the various ADS's modules are described to their design details.

4.1 Reset & Reset - Configuration

There are several reset levels for the MPC8266, all of which are provided by ADS logic:

1) Power On Reset
2) Hard-Reset
3) Soft-Reset

4.1.1 Power - On Reset

The power on reset to the MPC8266 initializes the processor state after power up. There are 3 sources for power-on reset on the ADS:

1) A dedicated logic, using Seiko S-80828ANMP-EDR-T2, which is a voltage detector of 2.8V +/- 2.4%, asserts PORESET# input to the MPC8266 for a period of ~2.5 sec. This time period is long enough to allow for VDDL stabilization time, powered by a different voltage regulator. It is assumed that the stabilization time for both linear regulators (see Figure 4-7 ". ADS Power Scheme" on page 55) is about the same - NOT APPLICABLE ON THIS BOARD.
2) A dedicated logic, using Seiko S-80816ANNP-EDD-T2, which is a voltage detector of 1.6V +/- 2.4%, asserts PORESET# input to the MPC8266 in case the VDDL regulator voltage drops - NOT APPLICABLE ON THIS BOARD.
3) PCI Reset signal from a motherboard the ADS is put in will cause the MPC8266 to start its Power-On Reset sequence.

4.1.1.1 Power - On Reset Configuration

At the end of the Power - On reset sequence, MODCK(1:3) and MODCKH(0:3) are sampled by the MPC8266 to configure the various clock modes of the MPC8266 (core, CPM, bus, etc). Selection among the MODCK(1:3) combination options is done by means of 3 dip-switches, see 2.3.2 "Setting MODCK(1:3) for PLLs Multiplication Factor - SW2(#1 - #3)" on page 17, while MODCKH(0:3) are obtained from the Reset Configuration word programmed to the Flash memory (or EEPROM). Additional configuration for the PLL is set using SW3, see 2.3.5 "Setting PCIMODCKH(0:3) - for PCI PLLs Multiplication Factors - SW3" on page 19.

The configuration master is determined upon the rising edge of PORST#, according to the state of RSTCONF# signal, driven low on this board, to set the MPC8266 as a configuration master.

After power-on reset negates, the hard-reset sequence starts, during which, many other different options are configured (see 4.1.2.4 "Hard Rest Configuration" on page 36). Although these bits are sampled whenever the hard-reset sequence is entered, they are **influential only once - after power-on reset**. If a hard reset sequence is entered later, MODCKH(0:3), although sampled, are don't care.

4.1.2 Hard Reset

Hard-Reset may be generated on the ADS by the following sources:

1) COP/JTAG Port.
2) Manual Hard reset.

3) MPC8266's internal sources.

Hard-Reset, when generated, causes the MPC8266 to reset all its internal hardware except for PLL logic, re-acquires the Hard-reset configuration from its current source, and jumps to the Reset vector in the exception table. Since hard-reset resets also the refresh logic for dynamic RAMs, their content is lost as well.

HRESET# when asserted, is extended internally by the MPC8266 for additional 512 bus clock cycles at the end of which, the MPC8266 waits for 16 bus clock cycles and then, re-checks the state of the HRESET# line.

HRESET# is an open-drain signal and must be driven with an open-drain gate by which ever external source is driving it. Otherwise, contention will occur over that line, which might cause permanent damage to either ADS logic and/or to the MPC8266 itself.

4.1.2.1 COP/JTAG Port Hard - Reset

To provide convenient hard-reset capability for a COP/JTAG controller, HRESET# line appears at the COP/JTAG port connector - P7. The COP/JTAG controller may directly generate hard-reset by asserting (low) this line.

4.1.2.2 Manual Hard - Reset

Manual hard reset allows run-time Hard-reset, when the COP controller is disconnected from the ADS and to support resident debuggers. Depressing both Soft-Reset and ABORT buttons(SW5 & SW4), asserts the HRESET# pin of the MPC8266, generating a HARD RESET sequence.

Since the HRESET# line may be driven internally by the MPC8266, it is driven to the MPC8266 with an open-drain gate. If off-board H/W connected to the ADS is to drive HRESET# line, then, it should do so with an open-drain gate, this, to avoid contention over this line.

To save on board area, a dedicated button is not provided, but is shared with the Soft-Reset button and the ABORT button - when both depressed, Hard Reset is generated.

An option for connecting external switches is available through 3 pin headers J6 and J7.

4.1.2.3 Internal Sources Hard - Reset

The MPC8266 has internal sources which generate Hard Reset. Among these sources are:

1) Loss of Lock Reset. When one of the PLLs (Core, CPM), is out of lock, hard-reset is generated.
2) Check-Stop Reset. When the core enters a Check-Stop state from some reason, hard-reset may be generated, depended on CSRE bit in the RMR.
3) Bus Monitor Reset. When the bus monitor is enabled and a bus cycle is not terminated, hard-reset is generated.
4) S/W Watch Dog Reset. When the S/W watch-dog is enabled, and application s/w fails to perform its reset routine, it will generate hard - reset.
5) COP/JTAG Reset (Internal). Hard reset may be forced by driving the HRESET# line via the external pin's scan chain. Not useful for run time.

In general, the MPC8266 asserts a reset line HARD or SOFT for a period 512 clock cycles after a reset source has been identified. A hard reset sequence is followed by a soft reset sequence.

4.1.2.4 Hard Rest Configuration

When Hard-Reset is applied to the MPC8266 (externally as well as internally), it samples the Hard-Reset configuration. This configuration is taken from the current Hard-Reset configuration source (only over the MS 8 bits of the data bus, D0-D7) whenever HRESET# is asserted. The only exception to this are the MODCKH(0:3) bits, which are actually sampled only once - after power-on reset.

For additional information see 2.3.2 "Setting MODCK(1:3) for PLLs Multiplication Factor - SW2(#1 - #3)" on page 17, 2.3.4 "Setting Hard - Reset Configuration Source" on page 18 and 2.3.5 "Setting PCIMOD-

CKH(0:3) - for PCI PLLs Multiplication Factors - SW3" on page 19.

During hard reset sequence, the MPC8266 reads the Hard Reset configuration source at addresses 0, 0x8, 0x18, 0x20,... a byte each time, to assemble the 32 bit configuration word. A total of 32 bytes of data is read from D(0:7) to acquire 8 full configuration words for system that may have up to 8 MPC8266 chips.

The configuration word for a single[1] MPC8266 is stored in the Flash memory or EEPROM, while the other 7 words are not initialized, as there are no additional MPC8266 chips on this ADS.

Table 4-1. Hard Reset Configuration Word

Field	*Data Bus Bits*	*Prog Value [Bin]*	*Implication*	*Offset In Flash/ EEPROM [Hex]*	*Value [Hex]*
EARB	0	'0'	Internal Arbitration Selected.	0	0C (04)[1]
EXMC	1	'0'	Internal Memory Controller. CS0~ active at system boot.		
CDIS	2	'0'	Core Enabled.		
EBM	3	'0'	Single MPC8265 Mode		
BPS	4:5	'11' ('01')[1]	32 Bit Boot Port Size,(8 bit boot port size)[1].		
CIP	6	'0'	Core Initial Prefix 1.		
ISPS	7	'0' (X)	64 bit internal space for external master access. In fact don't care on this board, as external master not supported.		
L2CPC	8:9	'00'	CI~/BADDR(29)/IRQ2~ selected as CI~ WT~/BADDR(30)/IRQ3~ selected as WT~ L2_HIT~/IRQ4~ selected as L2_HIT~ CPU_BG~/BADDR(31)/IRQ5 selected as CPU_BG~	8	32
DPPC	10:11	'11'	Data Parity Pin Configuration: DP0 set as EXT_BR2~, DP1 as EXT_BG2~, DP2 as EXT_DBG2~, DP3 as EXT_BR3~, DP4 as EXT_BG3~, DP5 as EXT_DBG3~, DP6 is IRQ6~, DP7 as IRQ7~.		
Reserved	12	'0'	Reserved, should be cleared.		
ISB	13:15	'010'	IMMR initial value 0x0F000000, i.e., the internal space resides initially at this address.		

[1]Although the MPC8266 as configuration master reads 8 configuration words, only the first configuration word is influential.

Table 4-1. Hard Reset Configuration Word

BMS	16	'0'	Boot memory (Flash/EEPROM) at 0xFE000000.	10	36
BBD	17	'0'	ABB~/IRQ2~ pin is set to ABB~ DBB~/IRQ3~ pin is set to DBB~		
MMR	18:19	'11'	Mask masters requests. Boot master is PCI.		
LBPC	20:21	'01'	Local Bus pins function as PCI bus.		
APPC	22:23	'10'	MODCK1/AP(1)/TC(0) set as BKSEL0 MODCK2/AP(2)/TC(1) set as BKSEL1 MODCK3/AP(3)/TC(2) set as BKSEL2 IRQ7~/APE~ set as IRQ7~[2] CS11~/AP(0) set as CS11~		
CS10PC	24:25	'01'	CS10~/BCTL1~/DBG_DIS~ set as BCTL1~	18	65
ALD_EN	26	'1'	PCI EEPROM Auto Load Enable.		
Reserved	27	'00'	Reserved. Should be cleared.		
MODCK_HI[3]	28:31	'0101'	This field sets the MODCKH(0:3) field, which is the 4 MSB for the 7 bit MODCK field. When MODCKH(0:3) are set to this value (5) and MODCK(1:3) == '101', both CPM and Core MFs are set to 2. When MODCK(1:3) == '111', CPM's MF is set to 2 while Core's MF is set to 3.		

[1]For EEPROM Configuration

[2]DP7 is also set as IRQ7~. They are logic OR'ed into the interrupt controller.

[3]Applies only when not working in PCI mode and only ONCE after power-on reset.

4.1.3 Soft Reset

Soft - Reset may be generated on the ADS from the following sources:

1) COP/JTAG Port
2) Manual Soft Reset
3) Internal MPC8266 source.

Soft-Reset, when generated, causes the MPC8266 to reset its internal logic, while keeping its hard-reset configuration and memory controller setup and then jumping to the Reset vector in the exception table. Since soft-reset, does not reset the refresh logic for dynamic RAMs, their contents is preserved.

SRESET# when asserted, is extended internally by the MPC8266 for an additional 512 bus clock cycles at the end of which, the MPC8266 waits for 16 bus clock cycles and then, re-checks the state of the SRESET# line.

SRESET# is an open-drain signal and must be driven with an open-drain gate by every external source driving it. Otherwise, contention will occur over that line, which might cause permanent damage to either the ADS logic and / or to the MPC8266 itself.

4.1.3.1 COP/JTAG Port Soft - Reset

To provide convenient soft-reset capability for a COP/JTAG controller, SRESET# line appears at the COP/JTAG port connector - P7. The COP/JTAG controller may directly generate Soft-reset by asserting (low) this line.

4.1.3.2 Manual Soft - Reset

Manual soft reset allows run-time soft-reset when the COP controller is disconnected from the ADS and for resident debuggers' support. Depressing the Soft-Reset button (SW5), asserts the SRESET# pin of the MPC8266, generating a Soft Reset sequence.

Since the SRESET# line may be driven internally by the MPC8266, it is driven to the MPC8266 with an open-drain gate. If off-board hardware is connected to the ADS is to drive SRESET# line, then, it should do so with an open-drain gate to avoid contention over this line, which might inflict permanent damage to either the ADS logic and / or to the MPC8266 itself.

The option of connecting an off-board switch is available through a 3 pin header on J7.

4.1.3.3 Internal Sources Soft - Reset

The only internal Soft-reset source is the COP/JTAG soft-reset, which may be generated using Public JTAG instructions to shift active-value ('0') to the SRESET# pin via the boundary scan chain. This is not useful for run time.

4.2 Local Interrupter

There are 2 external interrupt which are applied by ADS logic to the MPC8266 via its interrupt controller:

1) ABORT (NMI)
2) ATM UNI interrupt
3) Fast Ethernet PHY Interrupt

4.2.1 ABORT Interrupt

The ABORT (NMI), is generated by a push-button. When this button is depressed, the IRQ0# input to the MPC8266 is asserted. The purpose of this type of interrupt, is to support the use of resident debuggers if any is made available to the ADS. This interrupt is enabled by setting the MSR[EE] bit.

To support external (off-board) generation of an NMI, the IRQ0# line is driven by an open-drain gate. This allows for external h/w to also drive this line. If external h/w indeed does drive IRQ0#, it is compulsory that IRQ0# is driven by an open-drain gate.

The option of connecting an off-board switch is available through a 3 pin header on J6.

4.2.2 ATM UNI Interrupt

To support ATM UNI (User Network I/F) event report by means of interrupt, the interrupt output of the UNI (INTB) is connected to IRQ6# line of the MPC8266.

Since INTB of the UNI is an open-drain output, it is possible to connect additional (off-board) interrupt requesters on the same IRQ6#, provided that they drive IRQ6# with an open-drain gate as well.

4.2.3 Fast Ethernet Transceiver Interrupt

To support Fast Ethernet Transceiver event report by means of interrupt, the (FDS/MDINT) interrupt output of the LXT970A is connected to IRQ7# line of the MPC8266.

Since FDS/MDINT of the LXT970A is an open-drain output, it is possible to connect additional (off-board) interrupt requesters on the same IRQ7#, provided that they drive IRQ7# with an open-drain gate as well.

The FDS/MDINT is a dual functionality signal - on its FDS (Full-Duplex Status) function, it indicates whether the LXT970 is configured to Full/Half Duplex mode, while in its alternate function it serves as the transceivers MDINT active-low output. In order to achieve this functionality, bit 1 in register 17 (17.1) must be SET after the ADS comes out of Hard Reset. Setting this bit is allowed through the MDIO port of the

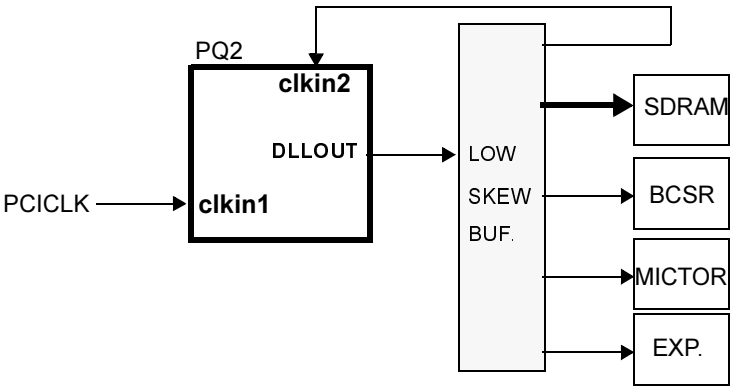
LXT970, Data of which is driven / sampled by PC9 of the MPC8266 while its Clock is driven by PC10. Failure in doing so, will result in IRQ7# pin of the MPC8266, constantly asserted (low).

4.3 Clock Distribution

The main clock input to the ADS is PCICLK. This is a 66MHz 3.3V clock signal from the PCI connector. The MPC8266 DLLOUT is connected to a low-skew buffer to split the load between all various clock consumers on board. A feedback path from the board to the MPC8266 CLKIN2 pin is used to control the bus clock skew in order to have same internal and external clock timing.

Special care is taken to isolate and terminate the clock routes between the clock-distributor and on-board consumers, this to provide "clean" clock inputs for proper operation.

Figure 4-1. Clocks Distribution Scheme



4.4 Buffering

In order to achieve best performance, it is necessary to reduce the capacitive load over the 60X bus as much as possible. Therefore, the slower devices on the bus, i.e., the Flash, the EEPROM, the BCSR and the ATM UNI M/P i/f are buffered, removing their capacitive load from the PPC bus, while the SDRAM is not buffered from the 60X bus.

Transceivers are provided for data. Use is done with 74ALVT buffers (by Phillips) which are 3.3V operated, 5V tolerant[1] and provide Bus-Hold to reduce pull up / down resistor count. This type of buffer reduces noise on board due to reduced transitions' amplitude.

To further reduce noise and reflections, damping resistors are placed over strobe lines and over all MPC8266's strobe lines.

The data transceivers open only if there is an access to a valid[2] buffered board address or during Hard - Reset configuration[3]. That way data conflicts are avoided between unbuffered memory reads and the data-buffers.

The MPC8266's PCI bus is not buffered.

4.5 Chip - Select Generator

The memory controller of the MPC8266 is used as a chip-select generator to access on-board[4] memories,

[1] Required for Flash and BCSR
[2] An address which covered in a Chip-Select region, that controls a buffered device.
[3] To allow a configuration word stored in Flash memory become active.
[4] And off-board. See further.

saving board's area reducing cost, power consumption and increasing flexibility.

The MPC8266's chip-selects assignment to the various memories / registers on the ADS are as shown in Table 4-2 ". ADS Chip Select Assignments" below:

Table 4-2. ADS Chip Select Assignments

Chip Select:	Assignment	Bus	Timing Machine
CS0#	Flash(EEPROM[1]) Memory.	60X (Buffered)	GPCM
CS1#	BCSR	60X (Buffered)	GPCM
CS2#	SDRAM	60X (Main)	SDRAM Machine 1
CS3#	EEPROM(Flash[1]) Memory.	60X (Buffered)	GPCM
CS4#	Unused.	-	-
CS5#	ATM UNI Microprocessor I/F	60X (Main)	UPMB
CS6#	Comm. Tool M/P I/F Cs 1	60X (Buffered)	GPCM / UPMx
CS7#	Comm. Tool M/P I/F Cs 2	60X (Buffered)	GPCM / UPMx
CS(8 -11)#	Unused	-	-

[1]EEPROM as boot memory.

For a situation when the Flash memorys' content is corrupt an option exists of booting from Flash memory or EEPROM memory, J6 jumper setting chooses between the two configurations. One configuration routes (by on board logic) CS0# line to the Flash and the EEPROM is mapped to CS3# line from MPC8266. In case the second option is enabled, CS0# line will be mapped (by on board logic) to the EEPROM memory and CS3# from MPC8266 will be mapped to the Flash memory (enabling the EEPROM as boot memory).

NOTE

Care should be taken when the EEPROM is used as boot memory. If writing to EEPROM wrong data (Hard Reset configuration words and boot code), an external programmer may be needed to reprogram the EEPROM with correct code for board initializations. Always make sure you can initialize the ADS correctly at least from either the Flash or EEPROM memory.

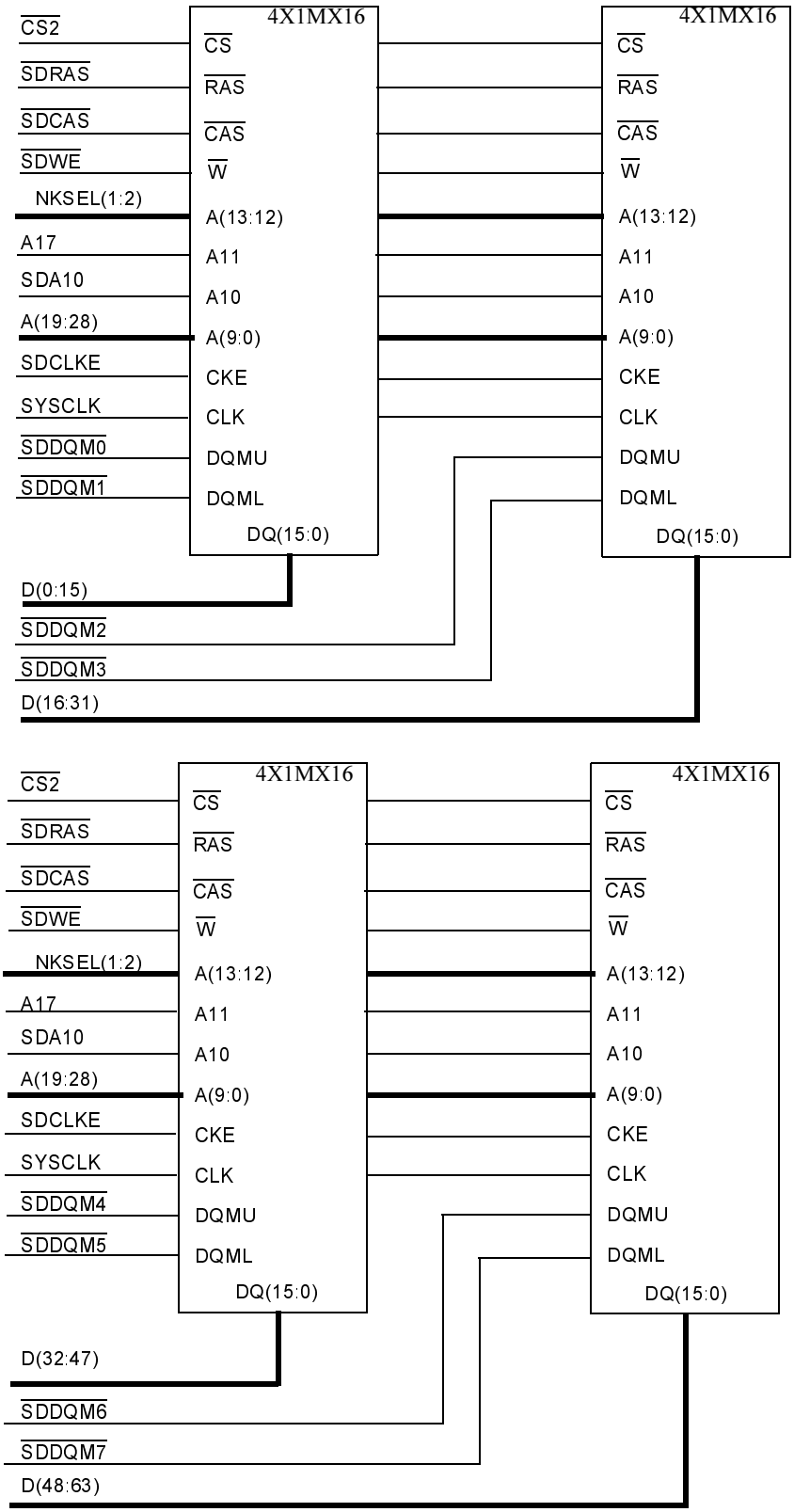
4.6 Synchronous DRAM (60X Bus)

To enhance performance, especially in higher operation frequencies - 32 MBytes of SDRAM are provided on board. The SDRAM's data bus is unbuffered from the MPC8266 60X bus and is configured as 4 X 1M X 64. The is composed of four 2 X 1M X 16 SDRAM chips (Fujitsu MB81F641642C-102FN).

The SDRAM's timing is controlled by SDRAM Machine #1, (associated with 60X bus,) via its assigned Chip Select line (See Table 4-2 ". ADS Chip Select Assignments" on page 41).

The SDRAM connection scheme is shown in Figure 4-2 ". SDRAM Connection Scheme" below.

Figure 4-2. SDRAM Connection Scheme



The SDRAM performance, is shown in Table 4-3 ". SDRAM (66MHz) Performance Figures" on page 43

Table 4-3. SDRAM (66MHz) Performance Figures

Cycle Type	System Clock Cycles @ 66MHz Bus Clock Freq.
Burst Read - Page Miss	6[1],1,1,1
Burst Read - Page Hit	4[1],1,1,1
Burst Write - Page Miss	4[1],1,1,1
Burst Write - Page Hit	2[1],1,1,1
Refresh	8[2]

[1]From TS# Asserted. First access may be longer due to internal pipeline delay

[2]Not including arbitration overhead.

4.6.1 SDRAM Programming

After power-up, the SDRAM needs to be initialized by means of programming, to establish its mode of operation. The SDRAM is programmed according to the following procedure:

1) Issue Precharge-All command
2) Issue 8 CBR refresh commands
3) Issue MODE-SET command.

When a Mode Register Set command is issued, data is passed to the Mode Register through the SDRAM's address lines. This command is fully supported by the SDRAM machine of the MPC8266.

Mode Register programming values are shown in Table 4-4 ". 66 MHz SDRAM Mode Register Program-

ming" below:

Table 4-4. 66 MHz SDRAM Mode Register Programming

SDRAM Address Line[1]	SDRAM Mode Reg Field	Value	Meaning:
A11 (MSB)	Reserved	'0'	
A10	Reserved	'0'	
A9	Opcode	'0' / '1'	0 - Burst Read & Burst Write (Copy-Back data cache) 1 - Burst Read & Single Write (Write-Through Data cache)
A8	Reserved	'0'	
A7	Reserved	'0'	
A6 - A4	CAS Latency	'010'	Data Valid 2 Clocks cycles after CAS Asserted
A3	Burst Type	'0'	Sequential Burst
A2 - A0	Burst Length	'011'	8 Operand Burst Length

[1]Actually SDRAM's A0 is connected to MPC8266's A28 and so on...

The SDRAM machine one of the MPC8266 needs to be initialized as well.

The programming of the SDRAM machine 1, is shown in Table 3-5 ". Memory Controller Initializations For 66Mhz (Flash as Boot memory)" on page 34.

4.6.2 SDRAM Refresh

The SDRAM is refreshed using its auto-refresh mode. I.e., using SDRAM machine one's periodic timer, an auto-refresh command is issued to the SDRAM every 13.4 µsec, so that all 1024[1] SDRAM rows are refreshed within specified 32.8 msec, while leaving an interval of ~5.4 msec of refresh redundancy within that window, as a safety measure, to cover for possible delays in bus availability for the refresh controller.

4.7 Flash Memory

The ADS is provided with 4 Mbytes of 90nsec Flash memory, 5V programmable, two AM29F160DB-90EC Bottom Boot Block type, by AMD, arranged as 1M X 32 in single bank.

To minimize use of MPC8266's chip-select lines, only one chip-select line is used to select the Flash as a whole. The control over the Flash is done using the GPCM and a dedicated region, controlling the whole bank. During hard - reset initializations[2], the debugger or any application S/W for that matter, can read the BCSR to detect which memory resides on CS0# (Flash or EEPROM) and decide how to program BR0 & OR0, BR3 & OR3 registers.

[1]In fact each SDRAM component is composed of 4 internal banks each having 1024 rows, but they are refreshed in parallel.
[2]I.e., initializations that follow the hard reset sequence at system boot.

The performance of the Flash memory is shown in Table 4-5 ". Flash Memory Performance Figures" below:

Table 4-5. Flash Memory Performance Figures

	Number of Bus Clock Cycles @ 66 MHz Bus Clock Freq.
Cycle Type \ Flash Delay [nsec]	90
Read Access	8[1]
Write[2] Access	6[1]

[1]From TS~ asserted. However, due to internal activity, these figures may be larger.

[2]The figures in the table refer to the actual write access. The write operation continues internally and the device has to be polled for completion.

4.8 E^{2}PROM Memory

The ADS is provided with 8 Kbytes of 70nsec Parallel Electrically Erasable and Programmable Read Only Memory (EEPROM), 5V programmable with software data protection, assembled in a 32 pin PLCC socket. The part number is AT28HC64B70JI, by Atmel, arranged as 8192words X 8 bits. The 60X bus address lines A17 thru A31 are routed to the socket (only A19 thru A31 are used by the 8 Kbyte EEPROM) to support a larger EEPROM memory, up to 32 Kbytes.

During hard - reset initializations[1], the debugger or any application S/W for that matter, can read the BCSR to detect which memory resides on CS0# (Flash or EEPROM) and decide how to program BR0 & OR0, BR3 & OR3 registers.

The EEPROM is accessed like a Static RAM for the read and write cycles.

NOTE

Due to the inherent characteristics of the EEPROM, data stored can be altered after power up/down sequences. Therefore, a software data protection should be activated before power is turned off. The EEPROM is factory locked. Consult the devices' data sheet for software data protection activation/de-activation.

The performance of the EEPROM memory is shown in Table 4-6 ". EEPROM Memory Performance

[1]I.e., initializations that follow the hard reset sequence at system boot.

Figures" below:

Table 4-6. EEPROM Memory Performance Figures

	Number of Bus Clock Cycles @ 66 MHz Bus Clock Freq.
Cycle Type\ EEPROM Delay [nsec]	70
Read Access	8[1]
Write[2] Access	10[1]

[1]From TS~ asserted.

[2]The figures in the table refer to the actual write access. The write operation continues internally.

4.9 Communication Ports

The ADS includes several communication ports, to allow convenient CPM evaluation. Obviously, it is not possible to provide all types of communication interfaces supported by the CPM, but it provides a convenient connection to communication interface devices to the MPC8266 via the CPM expansion connectors, residing on the edge of the board.

The communication ports' interfaces provided on the ADS are listed below:

1) 155 Mbps ATM UNI on FCC1 with Optical I/f, connected via UTOPIA I/F.
2) 10/100-Base-T Port on FCC2, MII controlled.
3) Dual RS232 port residing on SCC1 & SCC2.

4.9.1 ATM Port

To support the MPC8266's ATM controller, a 155.52Mbps User Network Interface (UNI) is provided on board, connected to FCC1 of the MPC8266 via the UTOPIA I/F. This is implemented with a PM5350 S/UNI-155-ULTRA by PMC-SIERA. Although these transceivers are capable of supporting 51.84Mbps rate, support is given only to the higher rate.

The control over the transceiver is done using the microprocessor i/f of the transceiver, controlled by the MPC8266 memory controller's GPCM. Since the UNI is 5V powered and the MPC8266 3.3V powered (5V intolerant), the UNI is buffered (LCX buffers) from the MPC8266 on both the receive part of UTOPIA I/F and the microprocessor control ports.

The ATM transceiver may be enabled / disabled at any time by writing '0' / '1' to the ATMEN# bit in BCSR1. When ATMEN# is negated, ('1') the microprocessor control port remains accessible on the MPC8266 memory map while its associated FCC is detached and may be used off-board via the expansion connectors.

The UNI interrupt output is connected to the MPC8266's DP6/CSE0/IRQ6# pin. This allows for interrupt-based handshake between the MPC8266 and the ATM UNI, in addition to a polling based handshake. This is an open-drain output and is pulled-up on the ADS. It is also appears at the CPM expansion connector, to be shared with an external tool interrupt request. See also 4.2 "Local Interrupter" on page 39.

The ATM transceiver reset input is driven by HRESET# signal of the MPC8266, so that the UNI is reset whenever a hard-reset sequence occurs. The UNI may also be reset by either asserting ATM_RST bit in BCSR1 (see Table 4-8 ". BCSR1 Description" on page 51) or by asserting ('1') the RESET bit in the Master Reset and Identify / Load Meters register via the UNI m/p i/f.

The UNI transmit and receive clocks is fed with a 19.44 MHz +/- 20 ppm, clock generator, 5 V powered,

while the receive and transmit fifos' clocks are provided by the MPC8266 using the same clock (CLK11).

The ATM transceiver has Transmit and Receive visual indications. These, however, are enabled by setting the following bits in the UNI POPC register (offset 0x68 from UNI base):

- TRAFIC to 1
- ALARM to 0
- TOGGLE[1:] to b11.

This will generate a 100 msec pulse over OUT1 and OUT0 pins of the UNI (attached to LD2 and LD1 respectively) indicating a successful ATM cell receive or transmit event, respectively.

The ATM SAR is connected to the physical medium by an optical I/F. This is implemented with HP's HFBR 5205 optical I/F, which operates at 1300 nm with upto 2 Km transmission range.

4.9.2 10/100 Base-T Port

A fast Ethernet port with T.P. (100-Base-TX) I/F is provided on the ADS. This port also supports 10 Mbps ethernet (10-Base-T) via the same transceiver - the LXT970AQ by Level One.

The LXT970 is connected to FCC2 of the MPC8266 via MII interface[1], which is used for both the device's control and data path. The initial configuration of the LXT970 is done by setting desired values at 8 configuration signals: FDE, CFG(0:1) and MF(0:4). The MF(0:4) pins however, are controlled by four voltage levels, this to allow each pin to configure two functions. On the ADS these pins are driven by factory set zero ohm resistors, connected to a voltage divider, allowing for a future option change during production.

The LXT970 is initially disabled, according to the state of FETHIEN in BCSR1. See Table 4-8 ". BCSR1 Description" on page 51.

The LXT970 reset input is driven by HRESET# signal of the MPC8266, resetting the transceiver whenever hard-reset sequence is taken. The LXT970 may also be reset by either asserting the FETH_RST bit in BCSR1 (see Table 4-8 ". BCSR1 Description" on page 51) or by asserting bit 0.15 (MSB of LXT970 control register) via the MII I/F.

To allow external use of FCC2, its pins appear at the CPM expansion connectors and the ethernet transceiver may be Disabled / Enabled at any time via the MII's MDIO port.

The LXT970 is able to interrupt the MPC8266 via the IRQ7# line. This line is shared also with the CPM expansion connectors. Therefore, any tool that is connected to IRQ7# or IRQ6# for that matter, should drive these lines with an Open Drain buffer. Both IRQ6# and IRQ7# are pulled-up on the ADS.

4.9.2.1 LXT970 Control

The LXT970 is controlled via the MII management[2] port which is a 2 wire interface: a clock (MDC) and a bidirectional data line (MDIO). This is in fact a bus, i.e., up to 32 devices may reside over it, while the protocol defines a 5-bit slave address field, which is compared against the slave address set to each device by hardware during device reset, according to the levels on MF(4:0) pins. On the ADS the slave address is hard-set to b00000. The MPC8266 on the ADS interfaces this port using two PI/O pins: PC9 for MDIO and PC10 for MDC. There is no special support within the MPC8266 for the MDIO port and the protocol is implemented in S/W.

The MDIO port may interrupt a host in 2 ways: (a[3]) driving low the MDIO line during IDLE time or (b) using a dedicated interrupt line FDS/MDINT# which may also serve as Full-Duplex indication. On the ADS, this line is connected to the MPC8266's DP7/CSE1/IRQ7# line, appearing also at the CPM expansion connectors. After the LX970 is reset, the FDS/MDINT# pin, wakes-up as FDS rather than MDINT# and therefore, **MUST be initially programmed to MDINT# function, by setting 17.1 bit**, otherwise, IRQ7# may

[1] Media Independent Interface.
[2] Also known as MII MDIO port.
[3] Not supported on the ADS.

be constantly driven low, possibly generating interrupts to the MPC8266, if not masked properly.

Since IRQ7# may also be driven by any tool, connected to the expansion connectors, it should be driven with an Open Drain buffer. IRQ7# is pulled-up on the ADS.

4.9.3 RS232 Ports

To assist user's applications and to provide convenient communication channels with both a terminal and a host computer, two identical RS232 ports are provided on the ADS, connected to SCC1 and SCC2 ports of the MPC8266. This is implemented by an MC145583 transceiver which generates RS232 levels internally using a single 3.3V supply and has a standby mode. When the $\overline{\text{RS232EN1}}$ or $\overline{\text{RS232EN2}}$ bits in BCSR1 are asserted (low), the corresponding transceiver is enabled. When negated, the corresponding transceiver enters standby mode, within which, the receiver outputs are tri-stated, enabling use of the corresponding port's pins, off-board via the expansion connectors.

The RS232 ports are implemented with one 9-pin, female D-Type connector P1 which is connected to SCC1 and one 10 pin, male, header connector P12 which is connected to SCC2. Both connectors, are configured to be directly (via a flat cable) connected to a standard IBM-PC like RS232 connector.

Figure 4-3. RS-232 Serial Port Connector P1

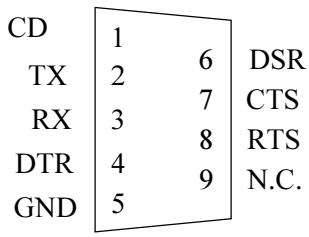
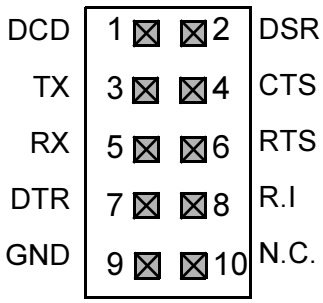


Figure 4-4. RS-232 Serial Port Connector P12



4.9.3.1 RS-232 Ports Signal Description

In the list below, the directions 'I', 'O', and 'I/O' are relative to the ADS board. (I.e. 'I' means input to the ADS)

- CD (O) - Data Carrier Detect. This line is always asserted by the ADS.
- TX (O) - Transmit Data. On Port 1 (Upper connector), connected to SCC1's TxD on PD30. On Port 2 (Lower connector) connected to SCC2's TxD on PD27.
- RX (I) - Receive Data. On Port 1 (Upper connector), connected to SCC1's RxD on PD31. On Port 2 (Lower connector) connected to SCC2's RxD on PD28.
- DTR (I) - Data Terminal Ready. This signal is used by the software on the ADS to detect if a terminal is connected to the ADS board. On Port 1 (Upper connector), connected to SCC1's CD#

on PC14. On Port 2 (Lower connector) connected to SCC2's CD# on PC12.

- DSR[1] (O) - Data Set Ready. This line is always asserted by the ADS.
- RTS (I) - Request To Send. This line is not connected on the ADS.
- CTS (O) - Clear To Send. On Port 1 (Upper connector), connected to SCC1's RTS# on PD29. On Port 2 (Lower connector) connected to SCC2's RTS# on P26.

4.10 Board Control & Status Register - BCSR

Most of the hardware options on the ADS are controlled or monitored by the BCSR, which is a 32 bit wide read / write register file. BCSR resides over the PPC Bus, accessed via the MPC8266's memory controller (see Table 4-2 ". ADS Chip Select Assignments" on page 41) and in fact includes 4 registers: BCSR0 to BCSR3. Since the minimum block size for a CS region is 32KBytes and only A(27:29) lines are decoded by the BCSR for register selection, BCSR0 - BCSR3 are duplicated many times inside that region. See also Table 1-1 ". MPC8266ADS-PCI-AI Specifications" on page 12.

The following functions are controlled / monitored by the BCSR:

1) ATM Port Control which includes:
   - Transceiver Enable / Disable
   - Transceiver Reset.
2) Fast Ethernet Port Control which includes:
   - Transceiver Initial Enable
   - Transceiver Reset
3) RS232 port 1 Enable / Disable.
4) RS232 port 2 Enable / Disable.
5) Flash Ready / Busy# Status.
6) Flash Reset / Power-down.
7) Hot-Swap ENUM# status.
8) Configuration source memory select status.
9) External (off-board) tools Support which include:
   - Tool Identification
   - Tool Revision
   - Tool Status Information
10) S/W Option Identification.
11) ADS Revision code.

Since part of the ADS's modules are controlled by the BCSR and since they may be disabled in favor of external hardware, the enable signals for these modules are presented at the CPM expansion connectors, so that off- board hardware may be mutually exclusively enabled with on-board modules.

4.10.1 BCSR0 - Board Control - Status Register 0

The BCSR0 serves as a control register on the ADS. Although it resides only over D(0:7) lines of the PPC data bus, it is accessed as a **word** at **offset 0** from BCSR base address. It may be read or written at any time. BCSR0 gets its defaults upon Power-On reset. BCSR0 fields are described in Table 4-7 ". BCSR0 Descrip-

[1]Since there are only 3 RS232 transmitters in the device, DSR is connected to CD.

tion" below:

Table 4-7. BCSR0 Description

BIT	MNEMONIC	Function	PON DEF	ATT.
0 - 5	Reserved	Un-Implemented.	-	-
6	SIGNAL_LAMP_1	***Signal Lamp 1***. When this signal is active (**low**), a dedicated Green LED (LD8) illuminates. When in-active, this led is darkened. This led may be used for S/W signalling to user.	1	R,W
7	SIGNAL_LAMP_2	***Signal Lamp 2***. When this signal is active (**low**), a dedicated Red LED (LD9) illuminates. When in-active, this led is darkened. This led may be used for S/W signalling to user.	1	R,W
8 - 31	Reserved	Un-Implemented.	-	-

4.10.2 BCSR1 - Board Control / Status Register 1

The BCSR1 serves as a control register on the ADS. Although it resides only over D(0:7) lines of the PPC data bus, it is accessed as a **word** at **offset 4** from BCSR base address. It may be read or written at any time. BCSR1 gets its defaults upon Power-On reset. BCSR1 fields are described in Table 4-8 ". BCSR1 Description" below

Table 4-8. BCSR1 Description

BIT	MNEMONIC	Function	PON DEF	ATT.
0	$\overline{\text{FLASH\_RST}}$	***Flash Reset Enable.*** When asserted (**low**), the Flash memory in the Reset / Power-Down state. This signal is **not** driven by HRESET# signal.	1	R,W
1	$\overline{\text{FLASH\_CFG}}$	***Flash Configuration Source***. When asserted (**low**) the status of the configuration source jumper (J6) is set to enable the Flash memory as the source for the Hard Reset configuration words. When negated, the status of the jumper indicates that the configuration words are read from the E^2PROM. i.e. when asserted CS0 selects the Flash memory and CS3 selects the E^2PROM.	J[1]	R
2	ATM_EN	***ATM Port Enable***. When asserted (**low**) the ATM UNI chip (PM5350) connected to FCC1 is enabled for transmission and reception. When negated, the ATM transceiver is in fact[2] in standby mode and its associated buffers[3] are in tri-state mode, freeing all its i/f signals for off-board use via the expansion connectors.	1	R,W
3	ATM_RST	***ATM Port Reset.*** When asserted (**low**), the ATM port transceiver is in reset state. This line is driven also by HRESET# signal of the MPC8266.	1	R,W
4	FETHIEN	***Fast Ethernet Port Initial Enable***. When asserted (**low**) the LXT970's MII port, residing on FCC2, is enabled after Power-Up or after FETH_RST is negated. When negated (**high**), the LXT970's MII port is isolated after Power-Up or after FETH_RST is negated and all i/f signals are tri-stated. After initial value has been set this signal has no influence over the LXT970 and MII isolation may be controlled via MDIO 0.10 bit.	1	R,W
5	FETH_RST	***Fast Ethernet port Reset.*** When active (**low**) the LXT970 is reset. This line is also driven by HRESET# signal of the MPC8266. Since MDDIS pin of the LXT970 is driven low with this application, the negation of this signal causes all the H/W configuration bits to be sampled for initial values and device control is moved to the MDIO channel, which is the control path of the MII port.	1	R,W
6	RS232EN_1	***RS232 port 1 Enable***. When asserted (**low**) the RS232 transceiver for port 1, is enabled. When negated, the RS232 transceiver for port 1, is in standby mode and SCC1 pins are available for off-board use via the expansion connectors.	1	R,W
7	RS232EN_2	***RS232 port 2 Enable***. When asserted (**low**) the RS232 transceiver for port 2, is enabled. When negated, the RS232 transceiver for port 2, is in standby mode and SCC2 pins are available for off-board use via the expansion connectors.	1	R,W
8 - 31	Reserved	Un-implemented	-	-

[1]Depends on J5 setting.

[2]ATM transceiver itself does not enter standby mode, the fact that it is disconnected from the MPC8266 emulates this state.

[3]Required for voltage levels adaptation.

4.10.3 BCSR2 - Board Control / Status Register - 2

BCSR2 is a status register which is accessed as **word** at **offset 8** from the BCSR base address. Its a **Read-Only** register which may be read at any time. BCSR2's various fields are described in Table 4-9 ". BCSR2 Description" on page 52.

Table 4-9. BCSR2 Description

BIT	MNEMONIC	Function	PON DEF	ATT.
0 - 7	TSTAT(0:7)	***Tool Status (0:7)***. This field is reserved for external tool status report. The exact meaning of each bit within this field is tool unique and therefore will be documented separately per each tool. These signals are available at the System expansion connector - P5.	-	R
8 - 11	TOOLREV(0:3)	***TOOL Revision (0:3)***. This field may contains the revision code of an external tool connected to the ADS. The various combinations of this field will be described per each tool user's manual. These signals are available at the System expansion connector - P5.		R
12 - 15	EXTTOLI(0:3)	***External Tools Identification***. These lines, which are available at the CPM expansion connectors, are intended to serve as tools' identifier. On-board S/W may check these lines to detect The presence of various tools (h/w expansions) at the CPM expansion connectors. For the external tools' codes and their associated combinations see Table 4-10 ". EXTOOLI(0:3) Assignment" on page 52.	-	R
16 - 17	SWOPT(0:1)[1]	***Software Option (0:1)***. This field shows the state of a dedicated dip-switches (SW6/1-2) providing an option to manually change a program flow.	0	R
18	$\overline{\text{HSENUM}}$	***Hot Swap $\overline{\text{ENUM}}$***. Hot Swap MPC8266 ENUM# pin value.	-	R
19	$\overline{\text{FRDY}}$	***Flash Ready/$\overline{\text{Busy}}$.*** Flash memory status bit.	-	R
20 - 23	BREVN(0:3)	***Board Revision Number (0:3)***. This field represents the revision code, hard-assigned to the ADS. See Table 4-12 ". ADS Revision Encoding" on page 53, for revisions' encoding.	-	R
24	SWOPT2	***Software Option 2.*** This is the LSB of the field. Shows the state of a dedicated dip-switch (SW6/3) providing an option to manually change a program flow. For the setting of SW6 see Figure 3-1. "SW6 - Description" on page 24.	0	R
25 - 31	GP(0:6)	***General Purpose(0:6).*** Board Configuration resistors for future announcments.	-	R

[1]There is additional bit to this field. See bit 24 in the same table.

Table 4-10. EXTOOLI(0:3) Assignment

EXTTOOLI(0:3) [hex]	External Tool
0	T/ECOM - MPC8266 Communication tool
1	Reserved
2	T1 Circuit Emulation Tool
3 - E	Reserved
F	Tool Non Existent

Table 4-11. External Tool Revision Encoding

TOOLREV(0:3) [hex]	External Tool Revision
0	ENGINEERING
1	PILOT
2	A[1]
3 - F	Reserved

[1]Future revision

Table 4-12. ADS Revision Encoding

Revision Number (0:3) [Hex]	ADS Revision
0	ENG (Engineering)
1	PILOT[1]
2	A[1]
3 - F	Reserved

[1]Future revisions

4.10.4 BCSR3 - Board Control / Status Register 3

BCSR3 is an additional control / status register which may be accessed as a **word** at **offset 0xC** from BCSR base address. This register is not implemented. It may be read or written but with no valid data nor any effect on the ADS. The description of BCSR3 is shown in Table 4-13 ". BCSR3 Description" below.

Table 4-13. BCSR3 Description

BIT	MNEMONIC	Function	PON DEF	ATT.
0 - 31	Reserved	Un Implemented	-	-

4.11 COP/JTAG Port

The COP - Common On-Chip Processor, is part of the MPC8266's JTAG machine, implemented as a set of additional instructions and logic within the JTAG permissions. This TAP (Test Access Port) port may be connected to a dedicated debug station[1], for extensive system debug.

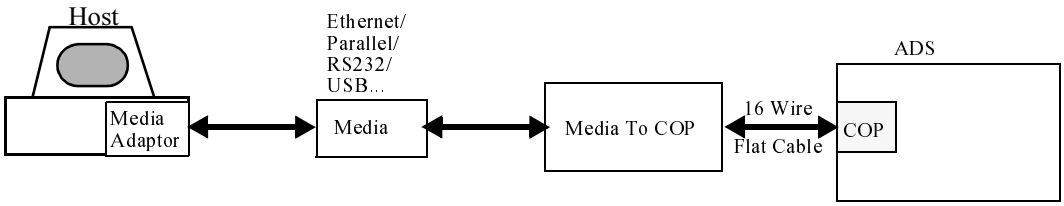
There are several third party debug solutions on the market. These debug-stations may be connected to the

[1]Not provided with the ADS.

host computer via either Ethernet, Parallel-Port, RS232 or any other media.

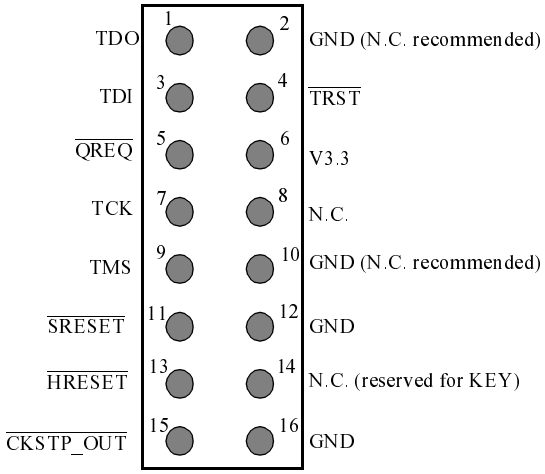
The debug station connection scheme is shown in Figure 4-5 ". Debug Station Connection Schemes" below:

Figure 4-5. Debug Station Connection Schemes



To support debug station connection to the COP/JTAG port, a 16 pin generic header connector (P7) is provided on the ADS, carrying the COP/JTAG signals as well as additional signals aiding in system debug. The pinout of this connector, is a general Motorola recommendation for including a COP/JTAG port in a design. The pinout of the COP/JTAG connector is shown in Figure 4-6 ". COP/JTAG Port Connector" on page 54:

Figure 4-6. COP/JTAG Port Connector[1]



For the detailed description of the COP / JTAG connector signals, see Table 5-5 ". P7 - COP / JTAG Connector - Interconnect Signals" on page 67.

4.12 Power

There are 4 power buses within the MPC8266:

1) VDDH (I/O)
2) VDDL (Internal Logic)
3) VCCSYN (CPM PLL)

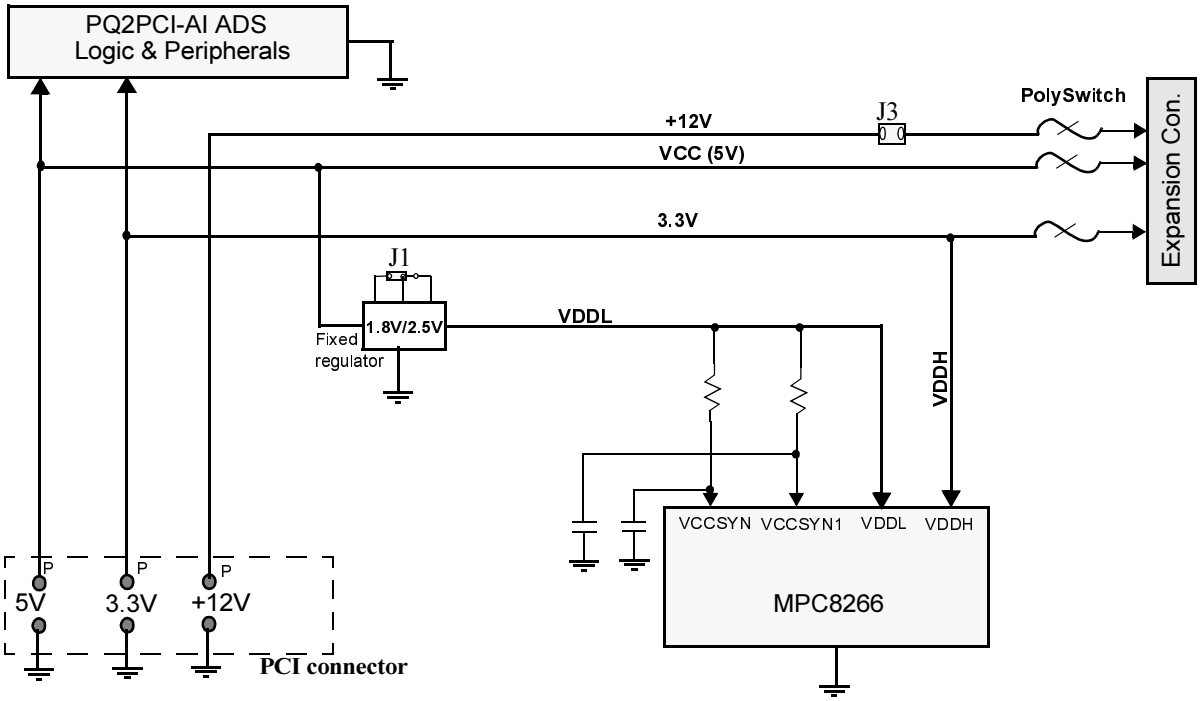
[1]To improve crosstalk immunity for COP/JTAG signals, pins 2 and 10 were connected to GND. According to the general recommendation they should be N.C.

4) VCCSYN1 (Core PLL)

and there are 4 power buses on the ADS whose source is the PCI connector:

1) VCC (5V) bus
2) V3.3 (3.3V) bus
3) VDDL (1.8V/2.5V) bus
4) VPP (+12V) bus

Figure 4-7. ADS Power Scheme



To support off-board application development, all the power buses are connected[1] to the expansion connectors, so that external logic may be powered directly from the board. The maximum current allowed to be drawn from the board on each bus is shown in Table 4-14 ". Off-board Application Maximum Current Consumption" below:

Table 4-14. Off-board Application Maximum Current Consumption

Power Bus	Max. Current
5V	2A
3.3V	2A
+12V	0.5A

As can be seen from Figure 4-7 ". ADS Power Scheme" above, +12V may also be provided to the expansion connector with the placement of a jumper on J3.

To protect on-board devices against supply spikes, decoupling capacitors are provided between the devices'

[1]Except for the +12V bus which connects through jumper J3.

power leads and GND, located as close as possible to the power leads, while bulk capacitors are spread around.

4.12.1 5V Bus

Some of the ADS peripherals reside on the 5V bus. Since the MPC8266 is not 5V tolerant, buffering is provided between 5V peripherals and the MPC8266, protecting the MPC8266 from the higher voltage level.

4.12.2 3.3V Bus

The MPC8266, the SDRAMs, the address and data buffers are powered by the 3.3V bus.

4.12.3 VDDL Bus

The MPC8266's internal logic and the PLL are powered with a lower-voltage power source, voltage of which may be in 2 levels:

- 2.5V
- 1.8V

Selection between the above levels is done via J1, which selects between different resistor values within the VDDL's variable regulator (U5) feedback network. For the different settings of J1 and their corresponding voltage levels see 2.3.1 "Setting VDDL Level - J1" on page 17 .

Changing the voltage to the Core logic of the MPC8266, obviously has an influence over the maximal speed of the core. There is the power-speed trade-off, i.e., lower operation speeds may be obtained with lower voltage supply.

4.12.4 +12V Bus

The sole purpose of the +12V bus is to supply programming voltage for Flash[1] memories or other peripherals connected to the expansion connectors.

[1] If necessary.

Chapter 5 Support Information

In this chapter all information needed for support, maintenance and connectivity to the PQ2PCIAI-ADS is provided.

5.1 Interconnect Signals

The PQ2PCIAI-ADS interconnects with external devices via the following set of connectors:

1) P1 - RS232 port 1 (DB9)
2) P2 - 100 / 10 - Base-T Ethernet port
3) P3 - PCI edge (“fingers”) Connector
4) P4, P6, P8, P9, P10 - Logic Analyzer MICTOR Connectors
5) P5 - System Expansion
6) P7 - COP / JTAG
7) P11 - CPM Expansion
8) P12 - RS232 port 2 (10 pin header)
9) P13 - Mach/Lattice In System Programming (ISP)

5.1.1 P1 - RS232 Port Connector

The RS232 port connector P1 is presented in Table 5-1 ". P1 Interconnect Signals" below

Table 5-1. P1 Interconnect Signals[1]

Pin No.	Signal Name	Description
1	CD	Carrier Detect **output** from the MPC8266ADS-PCI-AI.
2	TX	Transmit Data **output** from the MPC8266ADS-PCI-AI.
3	RX	Receive Data **input** to the MPC8266ADS-PCI-AI.
4	DTR	Data Terminal Ready **input** to the MPC8266ADS-PCI-AI.
5	GND	Ground signal of the MPC8266ADS-PCI-AI.
6	DSR	Data Set Ready **output** from the MPC8266ADS-PCI-AI.
7	CTS.	Clear To Send **output** from the MPC8266ADS-PCI-AI.
8	RTS	Ready To Send **input** from the MPC8266ADS-PCI-AI.
9	N.C.	No connect

[1]Refer to 4.9.3 "RS232 Ports" on page 47.

5.1.2 P2 - Ethernet Port Connector

The Ethernet connector on the PQ2PCIAI-ADS - P2, is a Twisted-Pair (10-Base-T) compatible connector. It is implemented with a 90^{o}, 8-pin, RJ45 connector, signals of which are described in Table 5-2 ". P2 -

Ethernet Port Interconnect Signals" below.

This connector is a part of an assembly that includes an integrated transformer and an RJ45 connector in one package. The part is an XFATM2-COMBO1-4 made by XFMRS.

Table 5-2. P2 - Ethernet Port Interconnect Signals

Pin No.	Signal Name	Description
1	TPTX	Twisted-Pair Transmit Data positive output from the PQ2PCIAI-ADS.
2	TPTX~	Twisted-Pair Transmit Data negative output from the PQ2PCIAI-ADS.
3	TPRX	Twisted-Pair Receive Data positive input to the PQ2PCIAI-ADS.
4	N.C.	Not connected, Bob Smith terminated on the PQ2PCIAI-ADS.
5		
6	TPRX~	Twisted-Pair Receive Data negative input to the PQ2PCIAI-ADS.
7	N.C.	Not connected, Bob Smith terminated on the PQ2PCIAI-ADS.
8		

5.1.3 P3 - PCI Edge Connector

P3 is a 2 X 62 “fingers”, 3.3V keyed, 32 bit PCI Edge connector. The ADS receives its power, clock, PCI bus controls, address & data, arbitration, jtag and system signals through this connector. The pinout of P3 is

available in Table 5-3 ". P3 - PCI Edge Connector" below.

For signal descriptions for this connector, see the PCI v2.2 Standard.

Table 5-3. P3 - PCI Edge Connector

Pin Number	Side B	Comments	Side A	Comments
1	-12V	Not Connected	TRST#	
2	TCK		+12V	
3	Ground		TMS	
4	TDO		TDI	
5	+5V		+5V	
6	+5V		INTA#	
7	INTB#	Not Connected	INTC#	Not Connected
8	INTD#	Not Connected	+5V	
9	PRSNT1#	Connected to GND	Reserved	Not Connected
10	Reserved	Not Connected	+3.3V(I/O)	
11	PRSNT2#	Connected to GND	Reserved	Not Connected
12	CONNECTOR KEY	3.3 volt key	CONNECTOR KEY	3.3 volt key
13	CONNECTOR KEY	3.3 volt key	CONNECTOR KEY	3.3 volt key
14	Reserved	Not Connected	3.3Vaux	Not Connected
15	Ground		RST#	
16	CLK		+3.3V (I/O)	
17	Ground		GNT#	
18	REQ#		Ground	
19	+3.3V (I/O)		PME#	Not Connected
20	AD[31]		AD[30]	
21	AD[29]		+3.3V	
22	Ground		AD[28]	
23	AD[27]		AD[26]	
24	AD[25]		Ground	
25	+3.3V		AD[24]	
26	C/BE[3]#		IDSEL	
27	AD[23]		+3.3V	
28	Ground		AD[22]	
29	AD[21]		AD[20]	
30	AD[19]		Ground	
31	+3.3V		AD[18]	
32	AD[17]		AD[16]	
33	C/BE[2]#		+3.3V	
34	Ground		FRAME#	
35	IRDY#		Ground	
36	+3.3V		TRDY#	
37	DEVSEL#		Ground	
38	Ground		STOP#	
39	LOCK#	Not Connected	+3.3V	
40	PERR#		SDONE	Not Connected
41	+3.3V		SBO#	Not Connected
42	SERR#		Ground	
43	+3.3V		PAR	
44	C/BE[1]#		AD[15]	
45	AD[14]		+3.3V	

Table 5-3. P3 - PCI Edge Connector

Pin Number	Side B	Comments	Side A	Comments
46	Ground		AD[13]	
47	AD[12]		AD[11]	
48	AD[10]		Ground	
49	M66EN	Coupled to GND, using a 0.01uF capacitor	AD[09]	
50	Ground		Ground	
51	Ground		Ground	
52	AD[08]		C/BE[0]#	
53	AD[07]		+3.3V	
54	+3.3V		AD[06]	
55	AD[05]		AD[04]	
56	AD[03]		Ground	
57	Ground		AD[02]	
58	AD[01]		AD[00]	
59	+3.3V (I/O)		+3.3V (I/O)	
60	ACK64#	Not Connected	REQ64#	Not Connected
61	+5V		+5V	
62	+5V		+5V	

5.1.4 P4, P6, P8, P9, P10 - Logic Analyzer Connectors

These are 38 pin, SMT, high density, matched impedance connector made by AMP. They contain the MPC8266 60X bus, 60X system and memory controller signals, unbuffered. The pinout of these connectors is shown in Chapter 6, “Schematics.”

For signal description of these connectors, see the MPC8266 User’s Manual.

5.1.5 MPC8266ADS-PCI-AI’s P5 - System Expansion Connector

P5 is a 128 pin, 90^0, DIN 41612 connector, which provide a minimal system I/F required to interface various types of communication transceivers, data path of which passes through MPC8266’s serial ports via P11. This connector contains 16 bit (lower PPC bus) address lines, 16 bit (higher PPC bus) Data lines plus useful GPCM and UPM control lines. The pinout of P5 is shown in Table 5-4 ". P5 - System Expansion - Intercon-

nect Signals" below:

Table 5-4. P5 - System Expansion - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
A1	EXPA16	O	Expansion Address (16[1]:31). This is a Latched-Buffered version of the MPC8266's PPC Address lines (16:31), provided for external tool connection. To avoid reflection these lines are series terminated with 43 Ω resistors.
A2	EXPA17		
A3	EXPA18		
A4	EXPA19		
A5	EXPA20		
A6	EXPA21		
A7	EXPA22		
A8	EXPA23		
A9	EXPA24		
A10	EXPA25		
A11	EXPA26		
A12	EXPA27		
A13	EXPA28		
A14	EXPA29		
A15	EXPA30		
A16	EXPA31		
A17	EXP12V	O	These can be connected to the positive 12V source from the PCI edge connector thru J3. This line is fused by a 0.5A ressetable poly-switch.
A18			
A19	N.C.	-	Not Connected.
A20	EXP3.3V	O	3.3V Power Out. These lines are connected to the main 3.3V plane of the PQ2PCIAI-ADS, this, to provide 3.3V power where necessary for external tool connected. The amount of current allowed to be drawn from this power bus is found in Table 4-14 ". Off-board Application Maximum Current Consumption" on page 55. This line is fused by a 1.9A ressetable poly-switch.
A21			
A22			
A23			
A24			
A25	N.C.	-	Not Connected.

Table 5-4. P5 - System Expansion - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
A26	EXPVCC	O	5V Supply. Connected to ADS's 5V VCC plane. Provided as power supply for external tool. For allowed current draw, see Table 4-14 ". Off-board Application Maximum Current Consumption" on page 55. This line is fused by a 1.9A ressetable poly-switch.
A27			
A28			
A29			
A30			
A31			
A32			
B1	GND	O	Digital Ground. Connected to main GND plane of the ADS.
B2			
B3			
B4	TSTAT0	I	Tool Status (0^1:7). These lines may be driven by an external tool to be read via BCSR2 of the ADS. These lines are pulled-up on the ADS, by 10 KΩ resistors. See also Table 4-9 ". BCSR2 Description" on page 52.
B5	TSTAT1		
B6	TSTAT2		
B7	TSTAT3		
B8	TSTAT4		
B9	TSTAT5		
B10	TSTAT6		
B11	TSTAT7		
B12	TOOLREV0	I	Tool Revision (0^1:3). These lines should be driven by an external tool with the Tool Revision Code, to be read via BCSR2 of the ADS. These lines are pulled-up on the ADS, by 10 KΩ resistors. See also Table 4-9 ". BCSR2 Description" on page 52.
B13	TOOLREV1		
B14	TOOLREV2		
B15	TOOLREV3		
B16	EXTOLI0	I	External Tool Identification (0^1:3). These lines should be driven by an external tool with the Tool Identification Code, to be read via BCSR2 of the ADS. These lines are pulled-up on the ADS, by 10 KΩ resistors. See also Table 4-9 ". BCSR2 Description" on page 52
B17	EXTOLI1		
B18	EXTOLI2		
B19	EXTOLI3		
B20	N.C.	-	Not Connected
B21	EXP3.3V	O	3.3V Power Out. These lines are connected to the main 3.3V plane of the PQ2PCIAI-ADS, this, to provide 3.3V power where necessary for external tool connected. The amount of current allowed to be drawn from this power bus is found in Table 4-14 ". Off-board Application Maximum Current Consumption" on page 55. This line is fused by a 1.9A ressetable poly-switch.
B22			
B23			
B24			
B25	N.C.	-	Not Connected

Table 5-4. P5 - System Expansion - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
B26	EXPVCC	O	5V Supply. Connected to ADS's 5V VCC plane. Provided as power supply for external tool. For allowed current draw, see Table 4-14 ". Off-board Application Maximum Current Consumption" on page 55. This line is fused by a 1.9A ressetable poly-switch.
B27			
B28			
B29			
B30			
B31			
B32			
C1	GND	O	Digital Ground. Connected to main GND plane of the ADS.
C2	CLK8	O	Buffered System Clock. This is a low skew buffered version of the MPC8266's DLLOUT signal, to be used by an external tool.
C3	GND	O	Digital Ground. Connected to main GND plane of the ADS.
C4	BTOOLCS1#	O	Buffered Tool Chip Select 1 (L). This is a buffered MPC8266's CS6# line, reserved for an external tool.
C5	BTOOLCS2#	O	Buffered Tool Chip Select 2 (L). This is a buffered MPC8266's CS7# line, reserved for an external tool.
C6	GND	O	Digital Ground. Connected to main GND plane of the ADS.
C7	ATMEN#	O	ATM Port Enable (L). This line enables the ATM port UNI's output lines towards the MPC8266. An external tool, using the same pins as does the ATM port should consult this signal before driving the same lines. **Failure to do so might result in permanent damage to the PM5350 ATM UNI.**
C8	ATMRST#	O	ATM Port Reset (L). This signal resets the ATM UNI (PM5350). An external tool may use this signal to its benefit.
C9	FETHRST#	O	Ethernet Port Reset (L). This signal resets the LXT970 Ethernet transceiver. An external tool may use this signal to its benefit.
C10	HRESET#	I/O, O.D.	MPC8266's Hard Reset (L). When asserted by an external H/W, generates Hard-Reset sequence for the MPC8266. During that sequence, asserted by the MPC8266 for 512 system clocks. Pulled Up on the ADS using a 1KΩ resistor. When driven by an external tool, **MUST be driven with an Open Drain gate. Failure to do so might result in permanent damage to the MPC8266 and / or to ADS logic.**
C11	IRQ6#	I	Interrupt Request 6 (L). Connected to MPC8266's DP6/CSE0/IRQ6# signal. Pulled up on the ADS with a 10 KΩ resistor. This line is shared with the ATM UNI's interrupt line and therefore, when driven by an external tool, **MUST be driven with an Open Drain gate. Failure to do so may result in permanent damage to the MPC8266 or to ADS logic.**

Table 5-4. P5 - System Expansion - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
C12	IRQ7#	I	Interrupt Request 7 (L). Connected to MPC8266's DP7/CSE1/IRQ7# signal. Pulled up on the ADS with a 10 KΩ resistor. This line is shared with the Fast Ethernet transceiver's interrupt line and therefore, when driven by an external tool, **MUST be driven with an Open Drain gate. Failure to do so might result in permanent damage to the MPC8266 and / or to ADS logic.**
C13	GND	O	Digital Ground. Connected to main GND plane of the ADS.
C14	EXPD0	I/O, T.S.	Expansion Data (0^1:15). This is a double buffered version of the PPC bus D(0:15) lines, controlled by on-board logic. These lines will be driven only if BTOOLCS1# or BTOOLCS2# are asserted. Otherwise they are tristated. The direction of these lines is determined by buffered BCTL0, in function of W/R#.
C15	EXPD1		
C16	EXPD2		
C17	EXPD3		
C18	EXPD4		
C19	EXPD5		
C20	EXPD6		
C21	EXPD7		
C22	EXPD8		
C23	EXPD9		
C24	EXPD10		
C25	EXPD11		
C26	EXPD12		
C27	EXPD13		
C28	EXPD14		
C29	EXPD15		
C30	N.C.	-	Not Connected
C31			
C32			
D1	GND	O	Digital Ground. Connected to main GND plane of the ADS.
D2			
D3			
D4	EXPWE0#	O	Expansion Write Enable (0:1) (L). These are buffered GPCM Write Enable lines (0:1). They are meant to qualify writes to GPCM controlled 8/16 data bus width memory devices. This to provide eased access to various communication transceivers. EXPWE0# controls EXPD(0:7) while EXPWE1# controls EXPD(8:15). These lines may also function as UPM controlled Byte Select Lines, which allow control over almost any type of memory device.
D5	EXPWE1#		
D6	GND	O	Digital Ground. Connected to main GND plane of the ADS.

Table 5-4. P5 - System Expansion - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
D7	EXPGL0#	O	Expansion General Purpose Lines (0:5) (L). These are buffered GPL(0:5)# lines which assist UPM control over memory device if necessary. These are output only signals and therefore, do not support H/W controlled UPM waits.
D8	EXPGL1#		
D9	EXPGL2#		
D10	EXPGL3#		
D11	EXPGL4#		
D12	EXPGL5#		
D13	GND	O	Digital Ground. Connected to main GND plane of the ADS.
D14	EXPALE	O	Expansion Address Latch Enable (H). This is the buffered MPC8266's ALE, provided for expansion board's use.
D15	EXPCTL0	O	Expansion Control Line 0. This line is a buffered version of MPC8266's BCTL0 (Bus Control Line 0) which serves as W/R#, provided for expansion board's use.
D16	GND	O	Digital Ground. Connected to main GND plane of the ADS.
D17			
D18			
D19			
D20			
D21			
D22			
D23			
D24			
D25			
D26			
D27			
D28			
D29			
D30			
D31			
D32			

[1]MS Bit.

5.1.6 P7 - COP / JTAG Port Connector

P7 is a Motorola standard COP / JTAG connector for the 60X processors family. It is a 16 pin protected header connector. The pinout of P7 is shown in Table 5-5 ". P7 - COP / JTAG Connector - Interconnect

Signals" below:

Table 5-5. P7 - COP / JTAG Connector - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
1	TDO	O	Transmit Data Output. This the MPC8266's JTAG serial data output driven by Falling edge of TCK.
2	GND	O	Digital GND. Main GND plane.
3	TDI	I	Transmit Data In. This is the JTAG serial data input of the ADS, sampled on the rising edge of TCK.
4	TRST#	I	Test port Reset~ (L). When this signal is active (Low), it resets the JTAG logic of the MPC8266. This line is pull-down on the ADS with a 1KΩ resistor, to provide constant reset of the JTAG logic.
5	QREQ#	O	Quiescent Request (L). When asserted (low), this line indicates that the MPC8266 desires to enter low-power mode. This signal may be required by a debug station.
6	3v3	O	3.3V power supply bus.
7	TCK	I	Test port Clock. This clock shifts in / out data to / from the JTAG logic. Data is driven on the falling edge of TCK and is sampled both internally and externally on it's rising edge. TCK is pulled up internally by the MPC8266.
8	N.C.	-	Not Connected.
9	TMS	I	Test Mode Select. This signal qualified with TCK in a same manner as TDI, changes the state of the JTAG machine. This line is pulled up internally by the MPC8266.
10	GND	O	Digital GND. Main GND plane.
11	SRESET#	I/O, O.D.	Soft Reset (L). This is the MPC8266's soft reset which is in fact a non-maskable interrupt, making the PPC take the reset exception from the reset vector. This line may be driven by the MPC8266 as well during soft-reset sequence, for 512 system clocks. This line is pulled up on the ADS with a 1KΩ resistor. When driven externally, it **MUST be driven with an Open Drain gate. Failure to do so may result in permanent damage to the MPC8266 and / or to ADS logic.**
12	GND	O	Digital GND. Main GND plane.
13	HRESET#	I/O, O.D.	MPC8266's Hard Reset (L). When asserted by an external H/W, generates Hard-Reset sequence for the MPC8266. During that sequence, asserted by the MPC8266 for 512 system clocks. Pulled Up on the ADS using a 1KΩ resistor. When driven by an external tool, **MUST be driven with an Open Drain gate. Failure to do so may result in permanent damage to the MPC8266 and / or to ADS logic.**
14	N.C.	-	Not Connected.
15	XBR3# (CKSTOP_OUT#)	I/O	Normally configured as XBR3# which has no function with this connector. May be configured as CKSTP_OUT# - Check Stop Out (L). When asserted (Low) indicates that the MPC8266 core has entered a Check-Stop state.

Table 5-5. P7 - COP / JTAG Connector - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
16	GND	O	Digital GND. Main GND plane.

5.1.7 MPC8266ADS-PCI-AI's P11 - CPM Expansion Connector

P11 is a 128 pin, 90^0, DIN 41612 connector, which allows for convenient expansion of the MPC8266's serial ports. This connector contains all CPM pins plus power supply pins, to provide for easy tool connection. The pinout of P11 is shown in Table 5-6 ". P11 - CPM Expansion - Interconnect Signals" below:

Table 5-6. P11 - CPM Expansion - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
A1	RS_RXD1 (PD31[1])	I/O, T.S.	When RS232 port #1 is enabled, this signal is the receive data line for that port. When this port is disabled, this signal is tristated and may be used to any available alternate function for PD31.
A2	RS_TXD1 (PD30)	I/O, T.S.	When RS232 port #1 is enabled, this signal is the transmit data line for that port. When this port is disabled, this signal may be used to any available alternate function for PD30.
A3	PD29	I/O, T.S	MPC8266's Port D 29 line. Parallel I/O or CPM dedicated line.May be used for any of it's available functions.
A4	RS_RXD2 (PD28)	I/O, T.S.	When RS232 port #2 is enabled, this signal is the receive data line for that port. When this port is disabled, this signal is tristated and may be used to any available alternate function for PD28.
A5	RS_TXD2 (PD27)	I/O, T.S.	When RS232 port #2 is enabled, this signal is the transmit data line for that port. When this port is disabled, this signal may be used to any available alternate function for PD27.
A6	PD26	I/O, T.S.	MPC8266's PD(26:18) Port D lines. Parallel I/O or CPM dedicated lines. May be used for any of their available functions.
A7	PD25		
A8	PD24		
A9	PD23		
A10	PD22		
A11	PD21		
A12	PD20		
A13	PD19		
A14	PD18		
A15	ATMRXPTY (PD17)	I/O, T.S.	ATM Receive Parity Line. When the ATM port is enabled, this line is connected to the receive parity of the PM5350 ATM UNI. When this port is disabled, this signal is tristated and may be used for any available function of PD17.
A16	ATMTXPTY (PD16)	I/O, T.S.	ATM Transmit Parity Line. When the ATM port is enabled, this line is connected to the transmit parity of the PM5350 ATM UNI. When this port is disabled, this signal may be used for any available function of PD16.

Table 5-6. P11 - CPM Expansion - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
A17	I2CSDA (PD15)	I/O, T.S.	This signal is connected to the serial I^2C data line. This line may be used off-board as an I^2C data line for external I^2C device.
A18	I2CSCL (PD14)	I/O, T.S.	This signal is connected to the serial I^2C clock line. This line may be used off-board as an I^2C clock line for external I^2C device.
A19	PD13	I/O, T.S.	MPC8266's PD(13:4) Port D lines. Parallel I/O or CPM dedicated lines. May be used for any of their available functions.
A20	PD12		
A21	PD11		
A22	PD10		
A23	PD9		
A24	PD8		
A25	PD7		
A26	PD6		
A27	PD5		
A28	PD4		
A29	ATMRCLKDIS	I	ATM Receive Clock Out Disable. When active (H), the ATMRCLK output, on pin C29 of this connector, is Tri-stated. When either not connected or driven low, ATMRCLK on pin C29, is enabled. This provides compatibility with ENG revision of T/ECOM communication tools.
A30	EXPVCC	O	5V Supply. Connected to ADS's 5V VCC plane. Provided as power supply for external tool. For allowed current draw, see Table 4-14 ". Off-board Application Maximum Current Consumption" on page 55. This line is fused by a 1.9A ressetable poly-switch.
A31			
A32			
B1	ATMTXEN# (PA31)	I/O, T.S.	ATM Transmit Enabled (L). When this signal is asserted (Low), while the ATM port is enabled and ATMTFCLK is rising, an octet of data, ATMTXD(7:0), is written into the transmit FIFO of the PM5350. When the ATM port is disabled, this line may be used for any available function of PA31.
B2	ATMTCA (PA30)	I/O, T.S.	ATM Transmit Cell Available (H). When this signal is asserted (High), while the ATM port is enabled, it indicates that the transmit FIFO of the PM5350 is empty and ready to except a new cell. When negated, it may show either that the transmit FIFO is Full or close to Full, depending on PM5350 internal programming. When the ATM port is disabled, this line may be used for any available function of PA30.
B3	ATMTSOC (PA29)	I/O, T.S.	ATM Transmit Start Of Cell (H). When this signal is asserted (High) by the MPC8266, while the ATM port is enabled, it indicates to the PM5350 the start of a new ATM cell over ATMTXD(7:0), i.e., the 1'st octet is present there. When the ATM port is disabled, this line may be used for any available function of PA29.

Table 5-6. P11 - CPM Expansion - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
B4	ATMRXEN# (PA28)	I/O, T.S.	ATM Receive Enable (L). When this signal is asserted (Low), while the ATM port is enabled and ATMRFCLK[2] goes high, on octet of data is available at the PM5350's ATMRXD(7:0) lines. When negated while ATMRFCLK goes high data on ATMRXD(7:0) is invalid, however driven. When the ATM port is disabled, this line may be used for any available function for PA28.
B5	ATMRSOC (PA27)	I/O, T.S.	ATM Receive Start Of Cell (H). When this signal is asserted (High), while the ATM port is enabled, it indicates, that the 1'st octet of data for the received cell is available at the PM5350's ATMRXD(7:0) lines. This line is updated over the rising edge of ATMRFCLK. When the ATM port is disabled, this line is tristated and may be used for any available function for PA27.
B6	ATMRCA (PA26)	I/O, T.S.	ATM Receive Cell Available (H). When this signal is asserted (High), while the ATM port is enabled and ATMRFCLK goes high, it indicates that the PM5350's receive FIFO is either full or that there are 4 empty bytes left in it - PM5350 internal programming dependent. When the ATM port is disabled, this line is tristated and may be used for any available function of PA26.
B7	ATMTXD0 (PA25)	I/O, T.S.	ATM Transmit Data (7^3:0). When the ATM port is enabled, this bus carries the ATM cell octets, written to the PM5350's transmit FIFO. This bus is considered valid only when ATMTXEN# is asserted and are sampled on the rising edge of ATMTFCLK. When the ATM port is disabled, these lines may be used for any available respective function.
B8	ATMTXD1 (PA24)		
B9	ATMTXD2 (PA23)		
B10	ATMTXD3 (PA22)		
B11	ATMTXD4 (PA21)		
B12	ATMTXD5 (PA20)		
B13	ATMTXD6 (PA19)		
B14	ATMTXD7 (PA18)		
B15	ATMRXD7 (PA17)	I/O, T.S.	ATM Receive Data (7^3:0). When the ATM port is enabled, this bus carries the cell octets, read from the PM5350 receive FIFO. This lines are updated on the rising edge of ATMRFCLK[2]. When the ATM port is disabled, these lines are tristated and may be used for any available respective function.
B16	ATMRXD6 (PA16)		
B17	ATMRXD5 (PA15)		
B18	ATMRXD4 (PA14)		
B19	ATMRXD3 (PA13)		
B20	ATMRXD2 (PA12)		
B21	ATMRXD1 (PA11)		
B22	ATMRXD0 (PA10)		

Table 5-6. P11 - CPM Expansion - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
B23	PA9	I/O, T.S.	MPC8266's Port A (9:0). Parallel I/O or dedicated CPM lines. May be used for any of their available functions.
B24	PA8		
B25	PA7		
B26	PA6		
B27	PA5		
B28	PA4		
B29	PA3		
B30	PA2		
B31	PA1		
B32	PA0		
C1	FETHTXER (PB31)	I/O, T.S.	Fast-Ethernet[4] Transmit Error (H). When the Ethernet port is enabled, this signal will be asserted (High) by the MPC8266 when an error is discovered in the transmit data stream. When the port is operation at 100 Mbps, the LXT970 responds by sending invalid code symbols on the line. When the Ethernet port is disabled, this line may be used for any available function of PB31.
C2	FETHRXDV (PB30)	I/O, T.S.	Fast-Ethernet Receive Data Valid (H). When this signal is asserted (High) while the Fast Ethernet port is enabled and FETHRXCK goes high, it indicates that data is valid on the MII Receive Data lines - FETHRXD(3:0). When the Fast Ethernet port is disabled, this line is tristated and may be used for any available function go PB30.
C3	FETHTXEN (PB29)	I/O, T.S.	Fast-Ethernet Transmit Enable (H). The MPC8266 will assert (High) this line, to indicate data valid on the FETHTXD(3:0) lines. When the Fast-Ethernet port is disabled, this line may be used for any available function of PB29.
C4	FETHRXER (PB28)	I/O, T.S.	Fast-Ethernet Receive Error (H). When this signal is asserted (High) by the LXT970, while the Ethernet port is enabled and FETHRXCK goes high, it indicates that the port is receiving invalid data symbols from the network. When the Ethernet port is disabled, this line is tristated and may be used for any available function of PB28.
C5	FETHCOL (PB27)	I/O, T.S.	Fast-Ethernet Port Collision Detected (H). When this signal is asserted (High) by the LXT970, while the ethernet port is enabled, it indicates a Collision state over the line. When the LXT970 is in Full-Duplex mode, this line is inactive. When the Ethernet port is disabled, this line is tristated and may be used for any available function of the PB27.

Table 5-6. P11 - CPM Expansion - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
C6	FETHCRS (PB26)	I/O, T.S.	Fast-Ethernet Carrier Sense (H). When this signal is asserted (High), while the Ethernet port is enabled and the LXT970 is in half-duplex mode, it indicates that either the transmit or receive media are non-idle. When the LXT970 is in either full-duplex or repeater operation, it indicates that the receive medium is non-idle. When the Ethernet port is disabled, this line may be used for any available function of PB26.
C7	FETHTXD3 (PB25)	I/O, T.S.	Fast Ethernet Transmit Data (3:0). This is the MII transmit data bus. The MPC8266 drives these lines according to rising edge of FETHTXCK. When the ethernet port is disabled, these lines may be used for any available respective function.
C8	FETHTXD2 (PB24)		
C9	FETHTXD1 (PB23)		
C10	FETHTXD0 (PB22)		
C11	FETHRXD0 (PB21)	I/O, T.S.	Fast Ethernet Receive Data (3:0). This is the MII receive data bus. The LXT970 drives these lines according to rising edge of FETHRXCK. When the ethernet port is disabled, these lines are tristated and may be used for any available respective parenthesized function.
C12	FETHRXD1 (PB20)		
C13	FETHRXD2 (PB19)		
C14	FETHRXD3 (PB18)		
C15	PB17	I/O, T.S.	MPC8266's Port B (17:4) Parallel I/O lines. May be used to any of their available functions.
C16	PB16		
C17	PB15		
C18	PB14		
C19	PB13		
C20	PB12		
C21	PB11		
C22	PB10		
C23	PB9		
C24	PB8		
C25	PB7		
C26	PB6		
C27	PB5		
C28	PB4		
C29	ATMRCLK	O, T.S.	ATM Receive Clock. A divide by 8 of the ATM line clock recovered by the ATM receive logic. Provided to assist Circuit Emulation Tool. Enabled only when pin A29 of this connector is either not connected or driven low. Otherwise, Tri-stated.
C30	GND	O	Digital Ground. Connected to main GND plane of the ADS.
C31			
C32			

Table 5-6. P11 - CPM Expansion - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
D1	PC31	I/O, T.S.	MPC8266's Port C (31:22) Parallel I/O lines. May be used to any of their available functions.
D2	PC30		
D3	PC29		
D4	PC28		
D5	PC27		
D6	PC26		
D7	PC25		
D8	PC24		
D9	PC23		
D10	PC22		
D11	ATMTFCLK (PC21)	I/O, T.S.	ATM Transmit FIFO Clock. Upon the rising edge of this clock (driven by the MPC8266), while the ATM port is enabled, the cell octets are written to the PM5350's transmit FIFO. This clock samples ATMTXD(7:0), ATMTXPTY, ATMTXEN# and ATMTSOC. When the ATM port is disabled, this line may be used for any available function of PC21.
D12	PC20	I/O, T.S.	MPC8266's Parallel I/O Port-C 20. Parallel I/O line. May be used for any of its available functions
D13	FETHRXCK (PC19)	I/O, T.S.	Fast-Ethernet Receive Clock. When the Ethernet port is enabled, this clock (25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps) is extracted from the received data and driven to the MPC8266 to qualify incoming receive data. When the Ethernet port is disabled, this line is tristated and may be used for any available function of PC19
D14	FETHTXCK (PC18)	I/O, T.S.	Fast-Ethernet Transmit Clock. When the Ethernet port is enabled, this clock (25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps) is normally extracted from the received data and driven to the MPC8266 to qualify out coming transmit data. In Slave mode (not used with this application) this clock should be input to the LXT970. When the Ethernet port is disabled, this line is tristated and may be used for any available function of PC18
D15	PC17	I/O, T.S.	MPC8266's Port C (17:15) Parallel I/O lines. May be used to any of their available functions.
D16	PC16		
D17	PC15		
D18	RS_CD1# (PC14)	I/O, T.S.	RS232 Port 1 Carrier Detect (L). Connected via RS232 transceiver to RS232 DTR1# input, allowing detection of a connected terminal to this port. This line is simply a PI/O input line to the MPC8266. When RS232 Port 1 is disabled, this line is tristated and may be used for any available function of PC14.
D19	PC13	I/O, T.S.	MPC8266's Port C 13 Parallel I/O line. May be used to any of its available functions.

Table 5-6. P11 - CPM Expansion - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
D20	RS_CD2# (PC12)	I/O, T.S.	RS232 Port 2 Carrier Detect (L). Connected via RS232 transceiver to RS232 DTR2# input, allowing detection of a connected terminal to this port. This line is simply a PI/O input line to the MPC8266. When RS232 Port 2 is disabled, this line is tristated and may be used for any available function of PC12.
D21	PC11	I/O, T.S.	MPC8266's Port C 11 Parallel I/O line. May be used to any of its available functions.
D22	FETHMDC (PC10)	I/O, T.S.	Fast-Ethernet Port Management Data Clock. This slow clock (S/W generated) qualifies the management data I/O to read / write the LXT970's internal registers. When the Ethernet port is disabled, this line may be used for any available function of PC10.
D23	FETHMDIO (PC9)	I/O, T.S.	Fast-Ethernet Port Management Data I/O. This signal serves as bidirectional serial data line, qualified by FETHMDC, to allow read / write the LXT970's internal registers. When the Ethernet port is disabled, this line may be used for any available function of PC9.
D24	PC8	I/O, T.S.	MPC8266's Port C (8:0) Parallel I/O lines. May be used to any of their available functions.
D25	PC7		
D26	PC6		
D27	PC5		
D28	PC4		
D29	PC3		
D30	PC2		
D31	PC1		
D32	PC0		

[1]The functions in parenthesis, are MPC8266's parallel I/Os.

[2]Normally connected to ATMTFCLK on the ADS.

[3]MS bit.

[4]For that matter, both 100-Base-T and 10-Base-T.

5.1.8 P12 - RS232 Port Connector

This is a 10 pin generic 0.100" pitch header connector. The RS232 port connector P12 is presented in Table 5-7 ". P12 Interconnect Signals" below

Table 5-7. P12 Interconnect Signals[1]

Pin No.	Signal Name	Description
1	CD	Carrier Detect **output** from the MPC8266ADS-PCI-AI.
2	DSR	Data Set Ready **output** from the MPC8266ADS-PCI-AI.
3	TX	Transmit Data **output** from the MPC8266ADS-PCI-AI.

Table 5-7. P12 Interconnect Signals[1]

Pin No.	Signal Name	Description
4	N.C.	No connect
5	RX	Receive Data **input** to the MPC8266ADS-PCI-AI.
6	RTS	Ready To Send **input** to the MPC8266ADS-PCI-AI.
7	DTR	Data Terminal Ready **input** to the MPC8266ADS-PCI-AI.
8	CTS	Clear To Send **output** from the MPC8266ADS-PCI-AI.
9	GND	Ground signal of the MPC8266ADS-PCI-AI.
10	N.C.	No connect

[1]Refer to 4.9.3 "RS232 Ports" on page 47.

5.1.9 P13 - Mach/Lattice In System Programming (ISP)

This is a 10 pin generic 0.100" pitch header connector, providing In System Programming capability for Lattice made programmable logic on board. The pinout of P13 is shown in Table 5-8 ". P13 - ISP Connector - Interconnect Signals" below:

Table 5-8. P13 - ISP Connector - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
1	ISPTCK	I	ISP Test port Clock. This clock shifts in / out data to / from the programmable logic JTAG chain.
2	N.C.	-	Not Connected.
3	ISPTMS	I	ISP Test Mode Select. This signal qualified with ISPTCK, changes the state of the prog. logic JTAG machine.
4	GND	O	Digital GND. Main GND plane.
5	ISPTDI	I	ISP Transmit Data In. This is the prog. logic's JTAG serial data input, sampled on the rising edge of TCK.
6	VCC	O	5V power supply bus.
7	ISPTDO	O	ISP Transmit Data Output. This the prog. logic's JTAG serial data output driven by Falling edge of TCK.
8	GND	O	Digital GND. Main GND plane.
9	N.C.	-	Not Connected.
10	N.C.	-	Not Connected.

5.2 PQ2PCIAI-ADS Part List

In this section the PQ2PCIAI-ADS's bill of material is listed according to their reference designation.

The BOM for the PQ2PCIAI-ADS is shown in Table 5-9 ". PQ2PCIAI-ADS Bill Of Material" below.

Table 5-9. PQ2PCIAI-ADS Bill Of Material

Reference Designation	Part Description	Manufacturer	Part #
C1,C2,C9,C13,C17,C19,C30, C40	Capacitor 68µF, 20V, 20%, SMD, Size D, Tantalum	AVX	TAJD686K020R
C3,C4,C5,C6,C7,C8,C10,C11,C12, C18,C20,C21,C24,C36,C38,C50, C51,C52,C53,C54,C55,C56	Capacitor 10µF, 25V, 10%, SMD Size C, Tantalum	AVX	TAJC106K025R
C14,C23,C25,C26,C27,C28, C29,C41,C42,C43,C44,C45, C46,C47,C48,C49,C60,C61, C63,C64,C65,C66,C67,C73, C75,C80,C84,C85,C88,C89, C100,C101,C102,C104,C105, C107,C108,C109,C111,C112, C113,C115,C116,C117,C118, C119,C121,C122,C123,C124, C125,C126,C127,C128,C129, C130,C131,C132,C133,C134, C135,C136,C137,C138,C139, C140,C141,C142,C143,C144, C145,C146,C174,C175,C176, C177,C178,C179,C180,C181, C182,C183,C184,C185,C186, C187,C188,C189,C190,C191, C192,C193,C194,C195,C196, C197,C198,C199	Capacitor 0.1µF, 16V, 10%, SMD 0603, Ceramic	AVX	0603YC104KAT2A
C15,C16,C32,C33,C34,C35, C37,C62,C68,C69,C70,C72, C76,C77,C78,C79,C81,C82, C83,C86,C87,C90,C91,C92, C94,C95,C96,C97,C98,C99, C103,C114,C120,C147,C148, C149,C150,C151,C152,C153, C154,C155,C156,C157,C158, C159,C160,C161,C162,C163, C164,C165,C166,C168,C169, C170,C171	Capacitor 10nF, 50V, 10%, X7R, SMD 0603, Ceramic	AVX	06035C103KAT2A
C22,C31,C39,C57	Capacitor 47µF, 16V, 10%, SMD Size D, Tantalum	AVX	TAJD476K016
C58	Capacitor 0.1µF, X7R, 500V, 20%, SMD Size 1812, Ceramic	JOHANSON DIELECTRIC	501S43W104MV4E
C59	Capacitor 0.001µF, 2 KV, 10%, SMD Size 1210, Ceramic	AVX	1210B102K202NT
C71,C74	Capacitor 10pF, 50V, 5%, SMD 1206, Ceramic	AVX	AV12065A100JATJ

Table 5-9. PQ2PCIAI-ADS Bill Of Material

Reference Designation	Part Description	Manufacturer	Part #
C93	Capacitor 1µF, 25V, 10%, SMD Size A, Tantalum	SIEMENS	B45196H5105K109
C106	Capacitor 1500pF, 50V, 10%, COG, SMD 1206 Ceramic	AVX	12065A152JAT00J
C167,C172,C173	Capacitor 22pF, 50V, 5%, COG, SMD 1206 Ceramic	AVX	12065A220JAT00J
D1	Diode SMD	TSC	LL4004G
F1,F2	PolySwitch, 1.9A miniSMD Fuse, Size 453x210	RAYCHEM	miniSMDE190
F3	PolySwitch, 0.5A miniSMD Fuse, Size 186x134	RAYCHEM	miniSMDC050
JP1,JP2,JP3,JP4,JP5	Gnd Bridge, Gold Plated	PRECIDIP	PD999-11-11210
J1,J4,J5,J6,J7,J8,J9	Jumper Header, 3 Pole with Fabricated Jumper	MOLEX	87156-0303
J2,J3	Jumper, 2 Pole, Soldered, Gold Plated	MOLEX	87156-4003
L1,L2,L3,L4,L5	Ferrite Bead SMD, Size 4532	TDK	HF70ACC453215
LD1,LD2,LD5,LD6,LD8,LD14, LD15,LD16	Led Green SMD, Size 1206	KINGBRIGHT	KPT-3216SGD
LD3,LD9	Led Red SMD, Size 1206	KINGBRIGHT	KPT-3216ID
LD4,LD7,LD10,LD11,LD12, LD13,LD17	Led Yellow SMD, Size 1206	KINGBRIGHT	KPT-3216YD
LD18	Led Blue SMD, Size 1206	KINGBRIGHT	KPT-3216MBC
P1	Connector 9 pin, Female, DType, 90°	KCC	DNR09SCB-SG
P2	Connector 8 pin, Combo Magnetics & Single RJ45 Receptacle, Shielded, 90°	XFMRS Inc. USA	XFATM2-COMBO1-4
P4,P6,P8,P9,P10	Connector MICTOR[1] 38 pin, SMD	AMP	2-767004-2
P5,P11	Connector 128 pin, Female, DIN 41612, 90°	ERNI	ERNI 043326
P7	Connector header, 16 pin, Male, T.H, 90°	KCC	LPH-16SA-SG
P12,P13	Connector header, 10 pin, dual in-line, SMD	SAMTEC	TSM-10501-SDV
Q1	Field Effect Transistor, TMOS Dual N-Channel, SO-8 Package	ON Semiconductor	MMDF4N01HD
R1,R23,R24,R32,R33	Resistor 51.1 Ω, 1%, SMD 0603, 0.1W	RODERSTEIN	D11 51R1FCS

Table 5-9. PQ2PCIAI-ADS Bill Of Material

Reference Designation	Part Description	Manufacturer	Part #
R2,R30,R46,R47,R49,R55, R58,R75,R93,R98,R99,R112, R120,R121,R124,R125,R127, R132,R137,R141,R151,R152, R153,R154,R156,R157,R159, R162,R163,R164,R165,R166, R167,R182	Resistor 0 Ω, SMD 0603, 0.1W	RODERSTEIN	D11 000RFCS
R5,R6,R44,R45,R48,R50,R78, R79,R80,R82,R83,R85,R91, R95,R113,R128,R130,R168, R169,R170,R171,R172,R173, R174,R175	Resistor 1 KΩ, 1%, SMD 0603, 0.1W	DRALORIK	D11 001KFCS
R7,R101	Resistor 10 Ω, 1%, SMD 1206, 1/4W	RODERSTEIN	D25 10R FCS
		AVX	CR32-10ROF-T
R9,R81,R86,R87,R88,R89, R90,R92,R96,R97,R100, R102,R103,R104,R105,R106, R107,R108,R109,R115,R116, R117,R118,R135,R138	Resistor 10 KΩ, 1%, SMD 0603, 0.1W	RODERSTEIN	D11 010KFCS
R10,R11,R12,R13,R14,R15, R16,R17,R18,R84	Resistor 43.2 Ω, 1%, SMD 0603, 0.1W	RODERSTEIN	D11 43R2FCS
R19,R20	Resistor 270 Ω, 1%, SMD 1206, 1/ 4W	DRALORIK	D25 270RFCS
R21,R22,R26,R28,R43	Resistor 2.7 Ω, 1%, SMD 1206, 1/ 4W	RODERSTEIN	D25 02R7FCS
R25	Resistor 100 Ω, 1%, SMD 1206, 1/ 4W	RODERSTEIN	D25 100RFCS
R27,R74	Resistor 0 Ω, SMD 1206, 1/4W	RODERSTEIN	D25 000RFCS
R29	Resistor 22.1 KΩ, 1%, SMD 1206, 1/ 4W	DRALORIK	D25-22K1FCS
R31	Resistor 63.4 Ω, 1%, SMD 1206, 1/ 4W	DRALORIK	D25 63R4FCS
R35,R36,R56,R59	Resistor 82.5 Ω, 5%, SMD 1206, 1/ 4W	DRALORIK	D25 82R5FCS
R37,R38,R60	Resistor 133 Ω, 1%, SMD 1206, 1/ 4W	DRALORIK	D25 133RFCS
R39	Resistor 2.2 MΩ, 1%, SMD 1206, 1/ 4W	RODERSTEIN	D2502M2FCS
R42,R53	Resistor 1.5 Ω, 1%, SMD 1206, 1/ 4W	RODERSTEIN	D25 01R5FCS
R51,R57,R63,R66,R67,R142, R143,R144,R146	Resistor 4.7 KΩ, 1%, SMD 0603, 0.1W	RODERSTEIN	D11 04K7FCS

Table 5-9. PQ2PCIAI-ADS Bill Of Material

Reference Designation	Part Description	Manufacturer	Part #
R61,R62,R139,R145,R147, R148,R149,R150,R176,R177, R178,R179	Resistor 150 Ω, 5% SMD 1206, 1/ 4W	RODERSTEIN	D25-150RFCS
R64	Resistor 24.9 Ω, 1%, SMD 1206, 1/ 4W	DRALORIK	D25 24R9FCS
R65,R71,R73,R76,R77	Resistor 330 Ω, 5%, SMD 1206, 1/ 4W	RODERSTEIN	D25 330RJCS
R70,R72	Resistor 243 Ω, 1%, SMD 1206, 1/ 4W	RODERSTEIN	D25 243RFCS
R155	Resistor 2 KΩ, 1%, SMD 1206, 1/ 4W	RODERSTEIN	D250 02KFCS
R158	Resistor 47 KΩ, 1%, SMD 1206, 1/ 4W	RODERSTEIN	D25 047KFCS
R161	Resistor 0.5 Ω, 1%, SMD 1206, 1/ 4W	RODERSTEIN	D25 0R50FCS
R180	Resistor 51.1 Ω, 1%, SMD 1206, 1/ 4W	RODERSTEIN	D25 51R1FCS
RN1,RN2,RN12,RN13,RN14, RN15,RN16,RN19,RN20,RN24, RN25,RN26,RN27,RN30,RN32, RN34,RN36,RN37,RN39,RN40, RN42,RN44,RN47,RN63	Resistor Network 22 Ω, 5%, 4 resistors, 8 pin.	DALE	CRA06S 08 03 220JR
RN3,RN10,RN21,RN22,RN23, RN28,RN29,RN31,RN41,RN46, RN49,RN50,RN51,RN52,RN53, RN54,RN55,RN56,RN59,RN60, RN61,RN62	Resistor Network 10 KΩ, 5%, 8 resistors, 10 pin, Common Bus	ROHM	RS8A 1002 J
RN4,RN5,RN6,RN7,RN8,RN9, RN11,RN17,RN18,RN33,RN35, RN38,RN43,RN45,RN48,RN57, RN58	Resistor Network 43 Ω, 5%, 4 resistors, 8 pin.	DALE	CRA06S 08 03 430JRT
SW2,SW3,SW6	Dip-Switch, 4 X SPST, SMD	GRAYHILL	90HBW04SR
SW4	SPDT, push button, WHITE, Sealed	C & K	KS12R21-CQE
SW5	SPDT, push button, BLACK, Sealed	C & K	KS12R22-CQE
U1	Fiber Optic I/F Module, 1300 nm wavelength, 2 Km Range	HP	HFBR 5205
U2	Clock Generator, 19.44 MHz, 20 ppm, 5V Supply, 4 pins, (8 pin DIP form factor)	COMCLOK	CM42AH-19.440
U3	Fast Ethernet Transceiver. 64 pin PQFP pkg.	Level One	LXT970QC/AQC
U4	Saturn User Network I/F (S/UNI) for 155.52 & 51.84 Mbps, 128 pin PQFP	PMC-Sierra Inc.	PM5350-RC

Table 5-9. PQ2PCIAI-ADS Bill Of Material

Reference Designation	Part Description	Manufacturer	Part #
U5	Voltage Regulator, Variable, 1.5 A output, D^2PAK package	ON Semiconductor	LM317D2T
U6,U11,U12	Octal CMOS Buffer. TSSOP pkg.	ON Semiconductor	MC74LCX541DT
U7	MPC8266, 2'nd generation Power QUICC.	Motorola	MPC8266
	Socket for the above, 480 pin, 1.27mm, PGA to PGA, 29 X 29 array, gold plated contacts.	ANDON	0-29-05-480-286-G04-N10
	Adaptor, PGA to BGA, 480 pin, 1.27mm, 29 X 29 array, gold plated contacts.		0-29-05-480-27KP30-N10
	Socket for the above, 480 pin, 1.27mm, PGA to BGA, 29 X 29 array, gold plated contacts, screw-lock, with HeatSink	E-Tec	BPW480-1265-29BA01H
U8,U26,U34	Low Voltage, CMOS, 5V Tolerant 16 bit buffer, with OEs. 48 pin Plastic TSSOP, Case 1201-01	ON Semiconductor	MC74LCX16244DT
U9,U10	Low Voltage, CMOS, 5V Tolerant 16 bit buffer, with Bus-Hold. 48 pin Plastic TSSOP.	Phillips	74ALVT16244DL
U13	9 Output, Low inter-skew, Clock Buffer.	Motorola Semiconductor	MPC947FA
U14,U15,U16,U17	SDRAM, 4 Banks X 1MByte X 16 Bit, 100MHz. 54p TSOPII pkg.	Fujitsu	MB81F641642C-102FN
U18	M4A-96/48 - 48 I/O, 96 Macrocell, 7.5 nsec propagation delay, In System Programmable Logic Device, 100 pin TQPF	Lattice/Vantis	M4A3-96/48-7VC
U19,U20	Low Voltage, CMOS, 5V Tolerant 16 bit Transceiver, with Bus-Hold. 48 pin Plastic TSSOP.	Phillips	74ALVT16245DL
U21	Octal Tri-State Buffer. 20 pin SOIC pkg.	ON Semiconductor	74ACT541DW
U22,U29	3.3V Powered, Single Supply, RS232 Transceiver (3 Tx, 5 Rx).	Motorola	MC145583VFEL
U23,U24	16 Mbit Flash, 90 nsec delay, Single bank, Bottom Boot block. 48 pin TSOP pkg.	AMD	AM29F160DB-90EI
U25	64 Kbit parallel EEPROM, 70 nsec, 32 pin PLCC pkg.	ATMEL	AT28HC64B-70JC
	32 pin PLCC SMD Socket	AMP	AMP 822273-1

Table 5-9. PQ2PCIAI-ADS Bill Of Material

Reference Designation	Part Description	Manufacturer	Part #
U27	Voltage level detector. Range 1.6V ±2%. O.D. output. SC-82AB package.	Seiko	S-80816ANNP-EDD-T2
U28	Voltage level detector. Range 2.8V ±2%. O.D. output. SOT-23-5 package.	Seiko	S-80828ANMP-EDR-T2
U30,U31,U33,U35	Quad CMOS buffer with individual Output Enable. TSSOP pkg.	ON Semiconductor	MC74LCX125DT
U32	Low Voltage, CMOS, 5V Tolerant 16 bit Transceiver. 48 pin Plastic TSSOP, Case 1201-01	ON Semiconductor	MC74LCX16245DT
Y1	Crystal resonator, 25 MHz, Fundamental Oscillation mode, Frequency tolerance ±30 ppm, Drive-level - 2mW max 10µW - 100 µW recommended, Shunt capacitance - 5pF Max., Load capacitance - 10pF min, Equivalent Series Resistance - 40Ω Max. Insulation Resistance - 500 MΩ min.	EPSON	MA-505

[1]Matched Impedance Connector.

5.3 Programmable Logic Equations

The PQ2PCIAI-ADS has one programmable logic device on it - U18, serving the role of Board Control and Status Register and providing miscellaneous system control functions on the ADS. Implemented using an M4-96/48-7VC by Lattice.

5.3.1 U18 - BCSR & System Control

```
MODULE Bcsr

TITLE 'pq2pci-ai ads control status register'

"
"*******************************************************************************
"* Device declaration.                                          *
"*******************************************************************************

"*******************************************************************************
"* Pins declaration.                                            *
"*******************************************************************************
"* System i/f pins
"*******************************************************************************
SYSCLK              PIN  11 ; " Clk signal from MPC947

BcsrCs_B            PIN  41 ; " Cs1 from Pq2
DVal_B              PIN  7  ;
R_B_W               PIN  36 ; " BCTL0 signal
BCTL1               PIN  66 ; " Alternate Buffers Enable source

A27                 PIN  6  ;
A28                 PIN  91 ;
A29                 PIN  86 ;

D0                  PIN  17  istype 'com' ;
D1                  PIN  83  istype 'com' ;
D2                  PIN  80  istype 'com' ;
D3                  PIN  92  istype 'com' ;
D4                  PIN  10  istype 'com' ;
D5                  PIN  94  istype 'com' ;
D6                  PIN  70  istype 'com' ;
D7                  PIN  84  istype 'com' ;

"*******************************************************************************
"* Board Control Pins. Read/Write.
"*******************************************************************************
SignaLamp0_B        PIN  67  istype 'reg,buffer' ; " status lamp 0 for misc
SignaLamp1_B        PIN  8   istype 'reg,buffer' ; " status lamp 1 for misc
                             " signaling
```

```
AtmEn_B              PIN  57  istype 'reg,buffer' ; " atm uni enable
AtmRst_B NODE     istype 'reg,buffer' ; " atm uni reset bit
AtmRstOut_B          PIN  96  istype 'com' ; " atm uni reset driven by
                                " register or by HRESET_B
FEthEn_B             PIN  18  istype 'reg,buffer' ; " ethernet trans enable
FEthRst_B       NODE     istype 'reg,buffer' ; " trans. reset bit
FEthRstOut_B         PIN  5   istype 'com' ; " fast eth trans reset driven
                                " by register or by HRESET_B
RS232En1_B           PIN  59  istype 'reg,buffer' ; " RS232 port 1 enable
RS232En2_B           PIN  16  istype 'reg,buffer' ; " RS232 port 2 enable


"*****************************************************************************
"* Board Status Registers Chip-Selects
"*****************************************************************************
Bcsr2Cs_B            PIN  68  istype 'com' ;

"*****************************************************************************
"* Flash and EEPROM Associated Pins.
"*****************************************************************************

Cs0_B            PIN  19 ; " from PQ2
Cs3_B            PIN  15 ; " from PQ2 (as second CS for Flash or EEprrom)
FlashCs_B        PIN  82 ; " flash chip-select
EEpromCs_B       PIN  32 ; " EEprom Chip-select

FlashRst_B    NODE    istype 'reg,buffer' ;
FlashRstOut_B    PIN  30  istype 'com' ; " Flash reset/power-down pin
                                " driven by reg NOT by HRESET_B

"*****************************************************************************
"* PMI5346 ATM UNI Associated Pins.
"*****************************************************************************

AtmCsIn_B        PIN  60 ;
AtmCsOut_B       PIN  42  istype 'com' ; " remove if short of pins
"*****************************************************************************
"* Reset & Interrupt Logic Pins.
"*****************************************************************************

PORIn_B              PIN  56 ;
```

```
RstConf_B           PIN  55  istype 'com'; " Hard Reset master select.

Rst0                PIN  47 ; " connected to N.C. of Reset P.B.
Rst1                PIN  46 ; " connected to N.O. of Reset P.B.


HardReset_B          PIN  44  istype 'com' ; " Actual hard reset output (O.D.)
SoftReset_B          PIN  58  istype 'com' ; " Actual soft reset output (O.D.)

Abr0                PIN  45 ; " connected to N.C. of Abort P.B.
Abr1                PIN  43 ; " connected to N.O. of Abort P.B.

NMIEn          NODE     istype 'com' ; " enables T.S. NMI pin
NMI_B               PIN  65  istype 'com' ; " Actual NMI pin (O,O.D.)

PCIRST_B PIN  79 ;
PCIRST_B_B PIN  81 ; " PCIRST_B inverted

"*****************************************************************************
"* Data Buffers Enables and Reset configuration support
"*****************************************************************************
TEA_B               PIN  33 ; " Transfer Error Acknowledge.

DataBufEn_B          PIN  20  istype 'com,invert' ; " data buffer enable

ToolCs1_B           PIN  31 ; " comm tool cs line 1.
ToolCs2_B           PIN  29 ; " comm tool cs line 2.

ToolDataBufEn_B        PIN  34  istype 'com,invert' ; " tool data buffer enable

"*****************************************************************************
"* Hard Reset Configuration Logic
"*****************************************************************************
FlashCfgSrc_B          PIN  9  ; " enable signal from external jumper

"*****************************************************************************
"* Auxiliary Pins.
"*****************************************************************************

"*****************************************************************************
"* System Hard Reset Configuration.
"*****************************************************************************
```

```
DataOeNODE istype ‘com’ ;“ data bus output enable on read.

“*****************************************************************************
“* Control Register Enable Protection.
“*****************************************************************************

“*****************************************************************************
“* Reset & Interrupt Logic Pins.
“*****************************************************************************
RstDeb1  NODE istype ‘keep,com’ ;   “ reset push button debouncer
AbrDeb1 NODE istype ‘keep,com’ ;   “ abort push button debouncer

HardResetEnNODE istype ‘com’ ;   “ enables T.S. hard reset pin
SoftResetEnNODE istype ‘com’ ;   “ enables T.S. soft reset pin

“*****************************************************************************
“* data buffers enable.
“*****************************************************************************
SyncHardReset_B  NODE istype ‘reg,buffer’ ;“ synchronized hard reset
DSyncHardReset_B  NODE istype ‘reg,buffer’ ;“ double synchronized hard reset

HoldOffCnt1,
HoldOffCnt0   NODE istype ‘reg,buffer’ ;      “ data buf en hold-off counter
HoldOffTc     NODE istype ‘com’ ;             “ terminal count for that counter

“*****************************************************************************
“* Power On Reset
“*****************************************************************************

S_PORIn_B     NODE  istype ‘reg,buffer’ ;   “ synced pon reset.

“*****************************************************************************
“* Misceleneous.
“*****************************************************************************

Alt_DataBufEn_B NODE istype ‘com’ ;



“*****************************************************************************
H, L, X, Z = 1, 0, .X., .Z. ;
```

```
C, D, U    = .C., .D., .U. ;
"*****************************************************************************
"* Signal groups
"*****************************************************************************

Add = [A27..A29] ;

Data = [D0..D7] ;

ContReg = [SignaLamp0_B,
        SignaLamp1_B,
        AtmEn_B,
        AtmRst_B,
        FEthEn_B,
        FEthRst_B,
        RS232En1_B,
        RS232En2_B] ;

ReadBcsr0 = [0,
          0,
          0,
          0,
          0,
          SignaLamp0_B,
          SignaLamp1_B] ;

ReadBcsr1 = [FlashRst_B.fb,
          FlashCfgSrc_B,
          AtmEn_B,
          AtmRst_B.fb,
          FEthEn_B,
          FEthRst_B.fb,
          RS232En1_B,
          RS232En2_B] ;

DrivenContReg = [SignaLamp0_B,
             SignaLamp1_B,
             AtmEn_B,
             FEthEn_B,
             RS232En1_B,
             RS232En2_B] ;
```

```
ClockedContReg = [SignaLamp0_B,
                  SignaLamp1_B,
                  FlashRst_B,
                  AtmEn_B,
                  AtmRst_B,
                  FEthEn_B,
                  FEthRst_B,
                  RS232En1_B,
                  RS232En2_B] ;

Bcsr0 = [SignaLamp0_B,  " for simulation
         SignaLamp1_B] ;

Bcsr1 = [FlashRst_B,    " for simulation
     FlashCfgSrc_B,
     AtmEn_B,
         AtmRst_B,
         FEthEn_B,
         FEthRst_B,
         RS232En1_B,
         RS232En2_B] ;

ToolCs =        [ToolCs1_B,ToolCs2_B] ;
FlashCsOut = [FlashCs_B] ;
EECsOut =       [EEpromCs_B];
Reset = [HardReset_B,SoftReset_B] ;
ResetEn = [HardResetEn,SoftResetEn] ;
TransRst = [AtmRstOut_B,FEthRstOut_B] ;
Rst =       [Rst1,Rst0] ;
Abr =       [Abr1,Abr0] ;
Debounce = [RstDeb1,AbrDeb1] ;
SyncReset = [SyncHardReset_B,DSyncHardReset_B] ;
RstCause = [PORIn_B,Rst1,Rst0,Abr1,Abr0] ;
HoldOffCnt =[HoldOffCnt1, HoldOffCnt0] ;
Cs =        [Cs0_B,Cs3_B,BcsrCs_B,AtmCsIn_B,ToolCs1_B,ToolCs2_B] ;
BufEn =         [DataBufEn_B,ToolDataBufEn_B] ;
CfgSrc = [FlashCfgSrc_B];
ConfAdd =       [A27,A28];
Cs2 =       [EEpromCs_B,FlashCs_B,BcsrCs_B,AtmCsIn_B,ToolCs1_B,ToolCs2_B] ;
"*****************************************************************************
```

```
“* Power On Reset definitions
“*****************************************************************************
PON_RESET_ACTIVE = 0 ;

PON_RESET = (S_PORIn_B.fb == PON_RESET_ACTIVE) ;

“*****************************************************************************
“* Register Access definitions
“*****************************************************************************
BCSR0_ADD = 0 ;
BCSR1_ADD = 1 ;
BCSR2_ADD = 2 ;
BCSR3_ADD = 3 ;

VGR_WRITE_BCSR_0 = (!BcsrCs_B & !DVal_B & R_B_W & !A27 & !A28 & !A29) ;
VGR_WRITE_BCSR_1 = (!BcsrCs_B & !DVal_B & R_B_W & !A27 & !A28 & A29) ;
“ VGR_WRITE_BCSR_3 = (!BcsrCs_B & !DVal_B & R_B_W & !A27 & A28 & A29) ;

BCSR_WRITE_ACTIVE = 0 ;

VGR_READ = (!BcsrCs_B & !R_B_W) ;

VGR_READ_BCSR_0 = (!BcsrCs_B & !R_B_W & !A27 & !A28 & !A29) ;
VGR_READ_BCSR_1 = (!BcsrCs_B & !R_B_W & !A27 & !A28 & A29) ;
VGR_READ_BCSR_2 = (!BcsrCs_B & !R_B_W & !A27 & A28 & !A29) ;
VGR_READ_BCSR_3 = (!BcsrCs_B & !R_B_W & !A27 & A28 & A29) ;
VGR_READ_BCSR_4 = (!BcsrCs_B & !R_B_W & A27 & !A28 & !A29) ;
VGR_READ_BCSR_5 = (!BcsrCs_B & !R_B_W & A27 & !A28 & A29) ;
VGR_READ_BCSR_6 = (!BcsrCs_B & !R_B_W & A27 & A28 & !A29) ;
VGR_READ_BCSR_7 = (!BcsrCs_B & !R_B_W & A27 & A28 & A29) ;



“*****************************************************************************
“*****************************************************************************
“* BCSR 0 definitions.
“*****************************************************************************
“*****************************************************************************
SIGNAL_LAMP_ON = 0 ;

“*********************************************
“******* Power On Defaults Assignments *********
“*********************************************
```

```
SIGNAL_LAMP0_PON_DEFAULT = !SIGNAL_LAMP_ON ;
SIGNAL_LAMP1_PON_DEFAULT = !SIGNAL_LAMP_ON ;

"****************************************
"******* Data Bits Assignments *************
"****************************************
SIGNAL_LAMP0_DATA_BIT = [D6] ;
SIGNAL_LAMP1_DATA_BIT = [D7] ;

"*****************************************************************************
"*****************************************************************************
"* BCSR 1 definitions.
"*****************************************************************************
"*****************************************************************************
FLASH_RESET_ACTIVE = 0 ;
ATM_ENABLED = 0 ;
ATM_RESET_ACTIVE = 0 ;
FETH_ENABLED = 0 ;
FETH_RESET_ACTIVE = 0 ;
RS232_1_ENABLE = 0 ;
RS232_2_ENABLE = 0 ;

"*********************************************
"******* Power On Defaults Assignments *********
"*********************************************
FLASH_RESET_PON_DEFAULT = !FLASH_RESET_ACTIVE ;
ATM_ENABLE_PON_DEFAULT = !ATM_ENABLED ;
ATM_RESET_PON_DEFAULT = !ATM_RESET_ACTIVE ;
FETH_ENABLE_PON_DEFAULT = !FETH_ENABLED ;
FETH_RESET_PON_DEFAULT = !FETH_RESET_ACTIVE ;
RS232_1_ENABLE_PON_DEFAULT = !RS232_1_ENABLE ;
RS232_2_ENABLE_PON_DEFAULT = !RS232_2_ENABLE ;

"****************************************
"******* Data Bits Assignments *************
"****************************************
FLASH_RESET_DATA_BIT = [D0] ;
FLASH_CFG_DATA_BIT = [D1] ;
ATM_ENABLE_DATA_BIT = [D2] ;
ATM_RESET_DATA_BIT = [D3] ;
FETH_ENABLE_DATA_BIT = [D4] ;
FETH_RESET_DATA_BIT = [D5] ;
```

```
RS232_1_ENABLE_DATA_BIT = [D6] ;
RS232_2_ENABLE_DATA_BIT = [D7] ;

“*****************************************************************************
“*****************************************************************************
“* BCSR 3 definitions.
“*****************************************************************************
“*****************************************************************************


“*********************************************
“******* Power On Defaults Assignments *********
“*********************************************


“*****************************************
“******* Data Bits Assignments *************
“*****************************************


“*****************************************************************************
“* Flash Declarations.
“*****************************************************************************
FLASH_ENABLE_ACTIVE = 0 ;

“*****************************************************************************
“* ATM UNI Declarations.
“*****************************************************************************

“*****************************************************************************
“* Reset Declarations.
“*****************************************************************************

“*****************************************************************************
“* data buffers enable.
“*****************************************************************************

BUFFER_DISABLED = 1 ;
BUFFER_ENABLED = !BUFFER_DISABLED ;


BUFFER_HOLD_OFF = (HoldOffCnt.fb != 0) ; “ the delay is required for read as
```

```
                " well since a fast device (eg bcsr) may content with
                " the flash

END_OF_FLASH_READ = !DVal_B & (!FlashCs_B # !EEpromCs_B) & !R_B_W & DSyncHardReset_B.fb ;
   " end of flash/eeprom read cycle. not during hard reset config

END_OF_ATM_READ = !DVal_B & !AtmCsIn_B & !R_B_W ;
      " end of atm uni m/p i/f read cycle

END_OF_OTHER_CYCLE = (!DVal_B & FlashCs_B & AtmCsIn_B # " another access or
                !DVal_B & !AtmCsIn_B & R_B_W #   " atm uni write
                !DVal_B & !ToolCs1_B & R_B_W #" tool 1 write
                !DVal_B & !ToolCs2_B & R_B_W #" tool 2 write
                !DVal_B & !FlashCs_B & R_B_W) ; " flash write

"*****************************************************************************
"* Hard Reset Configuration Logic
"*****************************************************************************
HRESET_CFG_IN_FLASH = (FlashCfgSrc_B == 0) ;
HRESET_CFG_IN_EEPROM = (FlashCfgSrc_B == 1) ;

HARD_RESET_ASSERTION = ( (HardReset_B == 0) & (SyncHardReset_B.fb == 0) &
                (DSyncHardReset_B.fb == 1) );

CS0_ASSERTED = (Cs0_B == 0);
CS3_ASSERTED = (Cs3_B == 0);

"*****************************************************************************
"* Equations, state diagrams.                                    *
"*****************************************************************************
"*                                                               *
"*****************************************************************************
"*****************************************************************************
"* BCSR 0
"*****************************************************************************
"*****************************************************************************
equations

ClockedContReg.clk = SYSCLK ;
ClockedContReg.ar = 0;
ClockedContReg.ap = 0;
DrivenContReg.oe = ^hfff ;
```

```
“*****************************************************************************
state_diagram SignaLamp0_B
   state SIGNAL_LAMP_ON:
         if (VGR_WRITE_BCSR_0 &
               (SIGNAL_LAMP0_DATA_BIT.pin == !SIGNAL_LAMP_ON) &
               (!PON_RESET # (SIGNAL_LAMP0_PON_DEFAULT != SIGNAL_LAMP_ON)) #
               (PON_RESET & (SIGNAL_LAMP0_PON_DEFAULT == !SIGNAL_LAMP_ON)) ) then
               !SIGNAL_LAMP_ON
         else
               SIGNAL_LAMP_ON ;
   state !SIGNAL_LAMP_ON:
         if (VGR_WRITE_BCSR_0 &
               (SIGNAL_LAMP0_DATA_BIT.pin == SIGNAL_LAMP_ON) &
               (!PON_RESET # (SIGNAL_LAMP0_PON_DEFAULT != !SIGNAL_LAMP_ON)) #
               (PON_RESET & (SIGNAL_LAMP0_PON_DEFAULT == SIGNAL_LAMP_ON)) ) then
               SIGNAL_LAMP_ON
         else
               !SIGNAL_LAMP_ON ;
“*****************************************************************************
state_diagram SignaLamp1_B
   state SIGNAL_LAMP_ON:
         if (VGR_WRITE_BCSR_0 &
               (SIGNAL_LAMP1_DATA_BIT.pin == !SIGNAL_LAMP_ON) &
               (!PON_RESET # (SIGNAL_LAMP1_PON_DEFAULT != SIGNAL_LAMP_ON)) #
               (PON_RESET & (SIGNAL_LAMP1_PON_DEFAULT == !SIGNAL_LAMP_ON)) ) then
               !SIGNAL_LAMP_ON
         else
               SIGNAL_LAMP_ON ;
   state !SIGNAL_LAMP_ON:
         if (VGR_WRITE_BCSR_0 &
               (SIGNAL_LAMP1_DATA_BIT.pin == SIGNAL_LAMP_ON) &
               (!PON_RESET # (SIGNAL_LAMP1_PON_DEFAULT != !SIGNAL_LAMP_ON)) #
               (PON_RESET & (SIGNAL_LAMP1_PON_DEFAULT == SIGNAL_LAMP_ON)) ) then
               SIGNAL_LAMP_ON
         else
               !SIGNAL_LAMP_ON ;

“*****************************************************************************
“*****************************************************************************
“* BCSR1 State Machines
“*****************************************************************************
```

```
“*****************************************************************************
state_diagram FlashRst_B
   state FLASH_RESET_ACTIVE:
          if (VGR_WRITE_BCSR_1 &
                 (FLASH_RESET_DATA_BIT.pin == !FLASH_RESET_ACTIVE) &
                  (!PON_RESET # (FLASH_RESET_PON_DEFAULT != FLASH_RESET_ACTIVE)) #
                  (PON_RESET & (FLASH_RESET_PON_DEFAULT == !FLASH_RESET_ACTIVE)) ) then
                 !FLASH_RESET_ACTIVE
          else
                 FLASH_RESET_ACTIVE ;
   state !FLASH_RESET_ACTIVE:
          if (VGR_WRITE_BCSR_1 &
                 (FLASH_RESET_DATA_BIT.pin == FLASH_RESET_ACTIVE) &
                  (!PON_RESET # (FLASH_RESET_PON_DEFAULT != !FLASH_RESET_ACTIVE)) #
                  (PON_RESET & (FLASH_RESET_PON_DEFAULT == FLASH_RESET_ACTIVE)) ) then
                 FLASH_RESET_ACTIVE
          else
                 !FLASH_RESET_ACTIVE ;
“*****************************************************************************
state_diagram AtmEn_B
   state ATM_ENABLED:
          if (VGR_WRITE_BCSR_1 &
                 (ATM_ENABLE_DATA_BIT.pin == !ATM_ENABLED) &
                  (!PON_RESET # (ATM_ENABLE_PON_DEFAULT != ATM_ENABLED)) #
                  (PON_RESET & (ATM_ENABLE_PON_DEFAULT == !ATM_ENABLED)) ) then
                 !ATM_ENABLED
          else
                 ATM_ENABLED ;
   state !ATM_ENABLED:
          if (VGR_WRITE_BCSR_1 &
                 (ATM_ENABLE_DATA_BIT.pin == ATM_ENABLED) &
                  (!PON_RESET # (ATM_ENABLE_PON_DEFAULT != !ATM_ENABLED)) #
                  (PON_RESET & (ATM_ENABLE_PON_DEFAULT == ATM_ENABLED)) ) then
                 ATM_ENABLED
          else
                 !ATM_ENABLED ;
“*****************************************************************************
state_diagram AtmRst_B
   state ATM_RESET_ACTIVE:
          if (VGR_WRITE_BCSR_1 &
                 (ATM_RESET_DATA_BIT.pin == !ATM_RESET_ACTIVE) &
                  (!PON_RESET # (ATM_RESET_PON_DEFAULT != ATM_RESET_ACTIVE)) #
```

```
                (PON_RESET & (ATM_RESET_PON_DEFAULT == !ATM_RESET_ACTIVE)) ) then
                !ATM_RESET_ACTIVE
        else
                ATM_RESET_ACTIVE ;
  state !ATM_RESET_ACTIVE:
        if (VGR_WRITE_BCSR_1 &
                (ATM_RESET_DATA_BIT.pin == ATM_RESET_ACTIVE) &
                (!PON_RESET # (ATM_RESET_PON_DEFAULT != !ATM_RESET_ACTIVE)) #
                (PON_RESET & (ATM_RESET_PON_DEFAULT == ATM_RESET_ACTIVE)) ) then
                ATM_RESET_ACTIVE
        else
                !ATM_RESET_ACTIVE ;
"*****************************************************************************
state_diagram FEthEn_B
  state FETH_ENABLED:
        if (VGR_WRITE_BCSR_1 &
                (FETH_ENABLE_DATA_BIT.pin == !FETH_ENABLED) &
                (!PON_RESET # (FETH_ENABLE_PON_DEFAULT != FETH_ENABLED)) #
                (PON_RESET & (FETH_ENABLE_PON_DEFAULT == !FETH_ENABLED)) ) then
                !FETH_ENABLED
        else
                FETH_ENABLED ;
  state !FETH_ENABLED:
        if (VGR_WRITE_BCSR_1 &
                (FETH_ENABLE_DATA_BIT.pin == FETH_ENABLED) &
                (!PON_RESET # (FETH_ENABLE_PON_DEFAULT != !FETH_ENABLED)) #
                (PON_RESET & (FETH_ENABLE_PON_DEFAULT == FETH_ENABLED)) ) then
                FETH_ENABLED
        else
                !FETH_ENABLED ;
"*****************************************************************************
state_diagram FEthRst_B
  state FETH_RESET_ACTIVE:
        if (VGR_WRITE_BCSR_1 &
                (FETH_RESET_DATA_BIT.pin == !FETH_RESET_ACTIVE) &
                (!PON_RESET # (FETH_RESET_PON_DEFAULT != FETH_RESET_ACTIVE)) #
                (PON_RESET & (FETH_RESET_PON_DEFAULT == !FETH_RESET_ACTIVE)) ) then
                !FETH_RESET_ACTIVE
        else
                FETH_RESET_ACTIVE ;
  state !FETH_RESET_ACTIVE:
        if (VGR_WRITE_BCSR_1 &
```

```
                (FETH_RESET_DATA_BIT.pin == FETH_RESET_ACTIVE) &
                (!PON_RESET # (FETH_RESET_PON_DEFAULT != !FETH_RESET_ACTIVE)) #
                (PON_RESET & (FETH_RESET_PON_DEFAULT == FETH_RESET_ACTIVE)) ) then
                FETH_RESET_ACTIVE
        else
                !FETH_RESET_ACTIVE ;
"*****************************************************************************
state_diagram RS232En1_B
  state RS232_1_ENABLE:
        if (VGR_WRITE_BCSR_1 &
                (RS232_1_ENABLE_DATA_BIT.pin == !RS232_1_ENABLE) &
                (!PON_RESET # (RS232_1_ENABLE_PON_DEFAULT != RS232_1_ENABLE)) #
                (PON_RESET & (RS232_1_ENABLE_PON_DEFAULT == !RS232_1_ENABLE)) ) then
                !RS232_1_ENABLE
        else
                RS232_1_ENABLE ;
  state !RS232_1_ENABLE:
        if (VGR_WRITE_BCSR_1 &
                (RS232_1_ENABLE_DATA_BIT.pin == RS232_1_ENABLE) &
                (!PON_RESET # (RS232_1_ENABLE_PON_DEFAULT != !RS232_1_ENABLE)) #
                (PON_RESET & (RS232_1_ENABLE_PON_DEFAULT == RS232_1_ENABLE)) ) then
                RS232_1_ENABLE
        else
                !RS232_1_ENABLE ;
"*****************************************************************************
state_diagram RS232En2_B
  state RS232_2_ENABLE:
        if (VGR_WRITE_BCSR_1 &
                (RS232_2_ENABLE_DATA_BIT.pin == !RS232_2_ENABLE) &
                (!PON_RESET # (RS232_2_ENABLE_PON_DEFAULT != RS232_2_ENABLE)) #
                (PON_RESET & (RS232_2_ENABLE_PON_DEFAULT == !RS232_2_ENABLE)) ) then
                !RS232_2_ENABLE
        else
                RS232_2_ENABLE ;
  state !RS232_2_ENABLE:
        if (VGR_WRITE_BCSR_1 &
                (RS232_2_ENABLE_DATA_BIT.pin == RS232_2_ENABLE) &
                (!PON_RESET # (RS232_2_ENABLE_PON_DEFAULT != !RS232_2_ENABLE)) #
                (PON_RESET & (RS232_2_ENABLE_PON_DEFAULT == RS232_2_ENABLE)) ) then
                RS232_2_ENABLE
        else
                !RS232_2_ENABLE ;
```

```
"*******************************************************************************
"*******************************************************************************
" External Read Registers' Chip-Selects
"*******************************************************************************
"*******************************************************************************
equations

Bcsr2Cs_B.oe = H ;

!Bcsr2Cs_B = VGR_READ_BCSR_2 ;

"*******************************************************************************
"*******************************************************************************
"* Read Registers.
"* All registers have read capabilty. (BCSR2 is read externally)
"*******************************************************************************
"*******************************************************************************
equations
   DataOe = VGR_READ_BCSR_0 #
            VGR_READ_BCSR_1 ;
   Data.oe = DataOe ;

   when (VGR_READ_BCSR_0) then
            Data = ReadBcsr0 ;
   else when (VGR_READ_BCSR_1) then
            Data = ReadBcsr1 ;



"*********************  brd_ctl  ****************************************
"*******************************************************************************
"*******************************************************************************
"* Reset Logic
"*******************************************************************************
"*******************************************************************************
"*******************************************************************************
equations

Reset.oe = ResetEn ;

Reset = 0 ;" open drain

RstDeb1 = !( Rst1 & (!( RstDeb1.com & Rst0) ) ) ;
```

```
" Reset push-button debouncer

AbrDeb1 = !( Abr1 & (!( AbrDeb1.com & Abr0) ) ) ;
" Abort push-button debouncer


HardResetEn = RstDeb1.com & AbrDeb1.com  ;" both buttons are depressed

SoftResetEn = RstDeb1.com & !AbrDeb1.com ;" only reset button depressed


TransRst.oe = 3 ;" transceivers' reset, always enabled.

!AtmRstOut_B = !AtmRst_B.fb # !HardReset_B ;

!FEthRstOut_B = !FEthRst_B.fb # !HardReset_B ;

PCIRST_B_B = !PCIRST_B ;

"*****************************************************************************
"* Hard reset configuration
"*****************************************************************************
equations

RstConf_B.oe = H;

RstConf_B = L;

"*****************************************************************************
"* NMI generation
"*****************************************************************************
equations

NMI_B.oe = NMIEn ;

NMI_B = 0 ;" O.D.

NMIEn = !RstDeb1.com & AbrDeb1.com ;" only abort button depressed

"*****************************************************************************
"* local data buffers enable
"*****************************************************************************
```

```
equations

SyncHardReset_B.clk = SYSCLK ;
SyncHardReset_B.ar = 0;
SyncHardReset_B.ap = 0;

DSyncHardReset_B.clk = SYSCLK ;
DSyncHardReset_B.ar = 0;
DSyncHardReset_B.ap = 0;

SyncHardReset_B := HardReset_B ;
DSyncHardReset_B := SyncHardReset_B.fb ;

DataBufEn_B.oe = H ;

!DataBufEn_B = ( !Cs0_B  #     " covers also hard reset config
            !Cs3_B #
            !BcsrCs_B #
            !AtmCsOut_B #   " provides data-hold for write
            !ToolCs1_B #
            !ToolCs2_B)  &
                  (!BUFFER_HOLD_OFF) #
                  !Alt_DataBufEn_B ;

ToolDataBufEn_B.oe = H ;

!ToolDataBufEn_B = (!ToolCs1_B #
              !ToolCs2_B)  &  (!BUFFER_HOLD_OFF)  ;

"*****************************************************************************
"* local data buffers disable (data contention protection)
"*****************************************************************************
"* Since with Voyager, hard-reset conf is read from flash during HRESET
"* asserted and since these are all consequitive read cycles and since
"* the cycles following hard reset are also reads (boot) the hold-off
"* state machine may be left in NO_HOLD_OFF for HRESET_B asserted duration
"* without warrying about contention between flash and data buffers.


equations

HoldOffCnt.clk = SYSCLK ;
```

```
HoldOffCnt.ar = 0;
HoldOffCnt.ap = 0;

HoldOffTc = (HoldOffCnt.fb == 3) ;

when ( (((END_OF_FLASH_READ # END_OF_ATM_READ ) & (HoldOffCnt.fb == 0)) #
       (HoldOffCnt.fb != 0)) & !HoldOffTc.com & DSyncHardReset_B.fb  ) then
    HoldOffCnt := HoldOffCnt.fb + 1 ;
else
    HoldOffCnt := 0 ;


"*******************************************************************************
"* Flash Chip Select
"*******************************************************************************
equations

FlashCs_B.oe = H ;

!FlashCs_B = HRESET_CFG_IN_FLASH & CS0_ASSERTED #
           HRESET_CFG_IN_EEPROM & CS3_ASSERTED ;

"*******************************************************************************
"* EEPROM Chip Select
"*******************************************************************************
equations

EEpromCs_B.oe = H ;

!EEpromCs_B = HRESET_CFG_IN_FLASH & CS3_ASSERTED #
           HRESET_CFG_IN_EEPROM & CS0_ASSERTED ;

"*******************************************************************************
"* ATM UNI Chip Select
"*******************************************************************************
equations

AtmCsOut_B.oe = H ;

!AtmCsOut_B = !AtmCsIn_B;

"*******************************************************************************
```

```
"* Power On Reset
"*****************************************************************************
equations

S_PORIn_B.clk = SYSCLK ;
S_PORIn_B.ar = 0;
S_PORIn_B.ap = 0;

S_PORIn_B := PORIn_B ;

"*****************************************************************************
"* Flash Reset/power-down
"*****************************************************************************
equations

FlashRstOut_B.oe = H ;   " flash reset always enabled

!FlashRstOut_B = !FlashRst_B.fb # HardResetEn; " minimum RESET pulse of 500nS !

"*****************************************************************************
"* Auxiliary functions
"*****************************************************************************
equations

!Alt_DataBufEn_B = TEA_B & !BCTL1 &
                   (!BUFFER_HOLD_OFF)  ;
END
```