

# MSC8113


## Reference Manual Addendum

This document provides updates to revision 0 of the *MSC8113 Reference Manual (MSC8113RM)*. The changes are organized by the chapters that are affected.

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## 1 UART

 In **Section 21.1.1** on page 21-8, replace the second note on the page with the following:

**Note:** When the shift register is empty (the TC and TDRE flags are set), transmission starts no more than one bit time after the data register is written. If only the TC interrupt source is enabled ( $SCICR[TCIE] = 1$ ,  $SCICR[TIE] = 0$ ), then you must ensure at least one bit time interval between successive writes to the SCIDR to enable the transmitter software to write twice to the SCIDR per interrupt.

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