Freescale Semiconductor
Addendum

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Errata to MSC8157E Reference Manual, Rev. 2

This errata describes corrections to the *MSC8157E Reference Manual*, Revision 2. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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Section, Page No.	Changes
5.3.1, 5-16	In Table 5-9, update RCWLR[29] description to “Reserved. Write to zero for future compatibility.”
5.3.1, 5-16	In Table 5-11, remove Exception ‘2’ from Modes 3, 8, 10, 13, 15, 17, 20, 24, 26, 27, and 32; add Exception ‘3’ to Modes 3 and 30.
15.10.52, 15-95	Update SRDS Bank 1 Reset Control Register (SRDSB2RSTCTL) figure and table by changing bit 30 to RST_DONE and bit 29 to RST_ERR. Register figure and Table 15-60 appear as:

SRDB1RSTCTL SRDS Bank 1 Reset Control Register Offset 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RST REQ	RST_ DONE	RST_ ERR	—												
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	—															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15-60. SRDSB1RSTCTL Field Descriptions

Bits	Description	Settings
RSTREQ 31	**SerDes Reset Request** Resets the SerDes PLL1 lock detection and test circuitry and also resets all logic in all lanes associated with SerDes PLL1. To initiate a SerDes reset, software writes a 1. The reset state machine clears the bit before reset is completed. **Note:** Software can only set this bit but not clear it. If the bit cleared before reset is complete, the reset state machine ignores the change.	0 No reset requested. 1 SerDes reset requested.
RST_DONE 30	**SerDes Reset Done from SerDes State Machine**	0 In the middle of the reset sequence (also during software SerDes reset sequence). 1 SerDes reset sequence done.
RST_ERR 29	**SerDes Reset Error** No PLL lock before counter time_out	0 Normal function. 1 PLL lock did not happen in the expected time period.
— 28–0	Reserved. Write to zero for future compatibility.	

15.10.56, 15-98	Update Lane A–J General Control Register 0 (L[A–J]GCR0) figure and table by changing bit 22 to RRST and bit 21 to TRST. Register figure and Table 15-64 appear as:

LAGCR0	Lane A General Control Register 0	Offset 0200h
LBGCR0	Lane B General Control Register 0	Offset 0240h
LCGCR0	Lane C General Control Register 0	Offset 0280h
LDGCR0	Lane D General Control Register 0	Offset 02C0h
LEGCR0	Lane E General Control Register 0	Offset 0300h
LFGCR0	Lane F General Control Register 0	Offset 0340h
LGGCR0	Lane G General Control Register 0	Offset 0380h
LHGCR0	Lane H General Control Register 0	Offset 03C0h
LIGCR0	Lane I General Control Register 0	Offset 0400h
LJGCR0	Lane J General Control Register 0	Offset 0440h

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—		RRAT_SEL		—		TRAT_SEL		—	RRST	TRST	—				
Type	R		R/W		R		R/W		R							
Reset	0	0	x	x	0	0	x	x	0	1	0	0	1	x	1	x
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	—															
Type	R															
Reset	0	0	x	x	x	x	x	x	0	0	0	0	0	0	0	0

Table 15-64. L[A–J]GCR0 Field Descriptions

Bits	Reset	Description	Settings	
— 31–30	0	Reserved. Write to zero for future compatibility.		
RRAT_SEL 29–28	Configured by Reset	**Receiver Speed Selection** Selects the lane receiver speed	00 01 10 11	Full speed Half speed Quarter speed reserved
— 27–26	0	Reserved. Write to zero for future compatibility.		
TRAT_SEL 25–24	Configured by Reset	**Transmitter Speed Selection** Selects the lane transmitter speed	00 01 10 11	Full speed Half speed Quarter speed reserved
— 23	0	Reserved. Write to zero for future compatibility.		
RRST 22	Configured by Reset	**Resets Receiver**	0 1	Reset Application mode
TRST 21	Configured by Reset	**Resets Transmitter** Coming out of POR, it is asserted (1'b0) and deasserts at PLL lock.	0 1	Reset Application mode
— 20–0	0	Reserved. Write to zero for future compatibility.		

16.1.7.2, 16-10 Throughout section, replace references to "LmGCR0BnGCRm0" with "L[A–J]GCR0."

Section, Page No.	Changes
16.4.2.6, 16-253	In Table 16-124, change bitfield IB*m*T8C*n*DBPR[SIZE] setting 0000h definition to Reserved

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