

# Errata to MSC8157 Reference Manual, Rev. 2

This errata describes corrections to the *MSC8157 Reference Manual*, Revision 2. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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- 5.3.1, 5-16 In Table 5-9, update RCWLR[29] description to “Reserved. Write to zero for future compatibility.”
- 5.3.1, 5-16 In Table 5-11, remove Exception ‘2’ from Modes 12, 14, 20, 29, 31, 35, 36, 37, 40, 46, 48, 61, 66, 69, 81, 83, and 102; add Exception ‘3’ to Modes 35, 36, 40, 48, 83, and 84.
- 15.10.52, 15-95 Update SRDS Bank 1 Reset Control Register (SRDSB2RSTCTL) figure and table by changing bit 30 to RST\_DONE and bit 29 to RST\_ERR. Register figure and Table 15-60 appear as:

SRDB1RSTCTL			SRDS Bank 1 Reset Control Register													Offset 0000h
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RST REQ	RST_ DONE	RST_ ERR	—												
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Type	R/W															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**Table 15-60. SRDSB1RSTCTL Field Descriptions**

Bits	Description	Settings
<b>RSTREQ</b> 31	<b>SerDes Reset Request</b> Resets the SerDes PLL1 lock detection and test circuitry and also resets all logic in all lanes associated with SerDes PLL1. To initiate a SerDes reset, software writes a 1. The reset state machine clears the bit before reset is completed. <b>Note:</b> Software can only set this bit but not clear it. If the bit cleared before reset is complete, the reset state machine ignores the change.	0 No reset requested. 1 SerDes reset requested.
<b>RST_DONE</b> 30	<b>SerDes Reset Done from SerDes State Machine</b>	0 In the middle of the reset sequence (also during software SerDes reset sequence). 1 SerDes reset sequence done.
<b>RST_ERR</b> 29	<b>SerDes Reset Error</b> No PLL lock before counter time_out	0 Normal function. 1 PLL lock did not happen in the expected time period.
— 28–0	Reserved. Write to zero for future compatibility.	

- 15.10.56, 15-98 Update Lane A–J General Control Register 0 (L[A–J]GCR0) figure and table by changing bit 22 to RRST and bit 21 to TRST. Register figure and Table 15-64 appear as:

<b>LAGCR0</b>	Lane A General Control Register 0	Offset 0200h
<b>LBGCR0</b>	Lane B General Control Register 0	Offset 0240h
<b>LCGCR0</b>	Lane C General Control Register 0	Offset 0280h
<b>LDGCR0</b>	Lane D General Control Register 0	Offset 02C0h
<b>LEGCR0</b>	Lane E General Control Register 0	Offset 0300h
<b>LFGCR0</b>	Lane F General Control Register 0	Offset 0340h
<b>LGGCR0</b>	Lane G General Control Register 0	Offset 0380h
<b>LHGCR0</b>	Lane H General Control Register 0	Offset 03C0h
<b>LIGCR0</b>	Lane I General Control Register 0	Offset 0400h
<b>LJGCR0</b>	Lane J General Control Register 0	Offset 0440h

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Type	—		RRAT_SEL		—		TRAT_SEL		—		RRST	TRST	—			
Reset	R		R/W		R		R/W		R							
Bit	0	0	x	x	0	0	x	x	0	1	0	0	1	x	1	x
	<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
Type	—															
Reset	R															
Reset	0	0	x	x	x	x	x	x	0	0	0	0	0	0	0	0

**Table 15-64.** L[A–J]GCR0 Field Descriptions

Bits	Reset	Description	Settings
— 31–30	0	Reserved. Write to zero for future compatibility.	
<b>RRAT_SEL</b> 29–28	Configured by Reset	<b>Receiver Speed Selection</b> Selects the lane receiver speed	00 Full speed 01 Half speed 10 Quarter speed 11 reserved
— 27–26	0	Reserved. Write to zero for future compatibility.	
<b>TRAT_SEL</b> 25–24	Configured by Reset	<b>Transmitter Speed Selection</b> Selects the lane transmitter speed	00 Full speed 01 Half speed 10 Quarter speed 11 reserved
— 23	0	Reserved. Write to zero for future compatibility.	
<b>RRST</b> 22	Configured by Reset	<b>Resets Receiver</b>	0 Reset 1 Application mode
<b>TRST</b> 21	Configured by Reset	<b>Resets Transmitter</b> Coming out of POR, it is asserted (1'b0) and deasserts at PLL lock.	0 Reset 1 Application mode
— 20–0	0	Reserved. Write to zero for future compatibility.	

16.1.7.2, 16-10 Throughout section, replace references to “LmGCR0BnGCRm0” with “L[A–J]GCR0.”

**Section, Page No.****Changes**

16.4.2.6, 16-253

In Table 16-124, change bitfield  $IBmT8CnDBPR[SIZE]$  setting 0000h definition to Reserved

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