MPF5200AMBA1ES – NXP Standard

Configuration report for PF5200-ASILB OTP program ID: A1 rev A

Rev. 1.0 - 17/09/2021 **Report**

1 General description

The PF5200 integrates multiple high performance buck regulators. It can operate as a stand-alone point-of-load regulator IC, or as a companion chip to a larger PMIC.

Built-in one-time programmable (OTP) memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states.

2 Features and benefits

- Two high efficiency buck converters
- Watchdog timer/monitor
- Monitoring circuit to fit ASIL B safety level
- One-time programmable device configuration
- 3.4 MHz I2C communication interface
- 32-pin FC-QFN package with wettable flank

3 Applications

- Automotive Infotainment
- High-end consumer and industrial

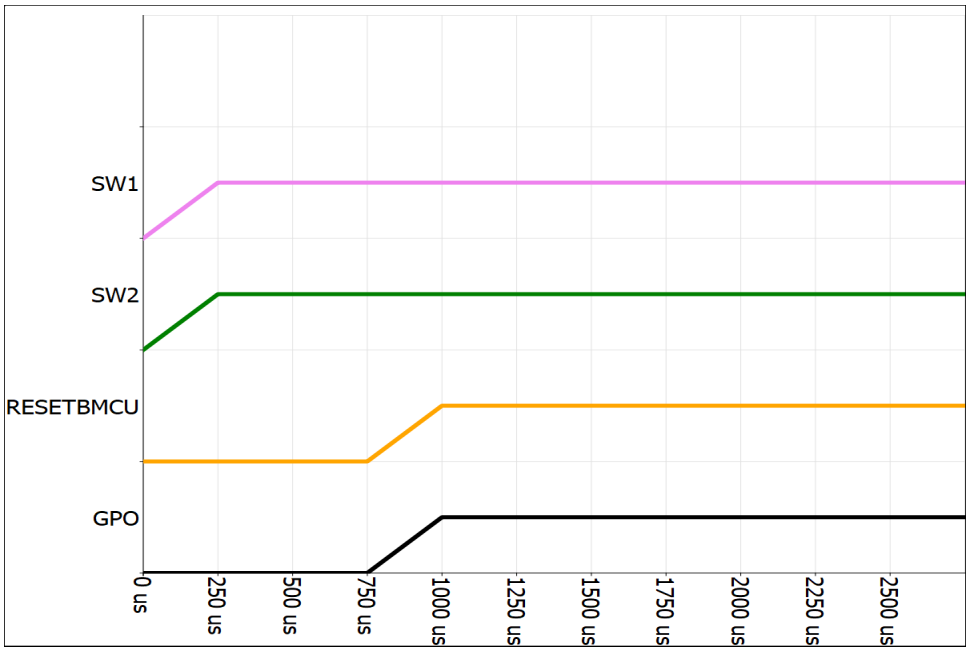
4 Ordering information

Table 1. Ordering information

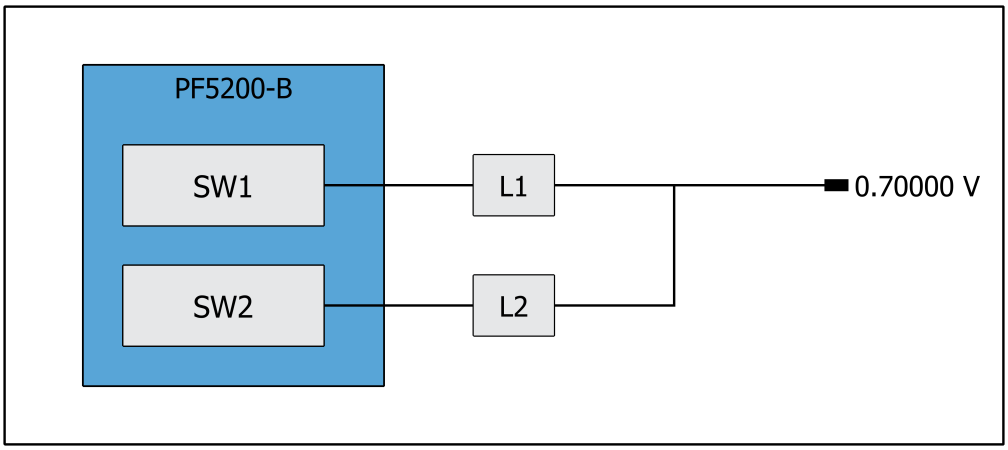
Type number[1]	Package		
	Name	Description	Version
MPF5200AMBA1ES	PQFN32	Plastic thermal enhanced very thin quad flat pack; no leads, wettable flank, 32 terminals, 0.5 mm pitch, 5 mm x 5 mm x 0.68 mm body	SOT2039 - 1(SC)

[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Power-up sequence summary



6 Hardware configuration diagram



7 OTP configuration

See PF5200 datasheet for parametric details. The OTP configuration summary for A1 sequence ID is provided in Tables below.

Table 2. Device OTP configuration

Functional block	Feature	OTP selection
System Configuration	I2C address	0x09
	I2C CRC	Enabled
	I2C secure write	Enabled
	VIN_OVLO Mode	Enabled
	VIN_OVLO shutdown	Device shuts down upon a VIN_OVLO
	Maximum fault counter	3 Faults
	Fault timer	1 ms
	Fail safe state	Disabled(Follow FS State condition)
	Max FS counter	2 Events
	FS self-clear timer	1 Minute
	Bandgap comparator	Disabled (Device Shutdown)
I/O CONFIGURATION	Power on event detection	Level sensitive
	PWRON debounce	Falling Edge - 32 ms and Rising Edge - 32 ms
	TRESET behavior	Shutdown
	TRESET time	2 s
	PGOOD pin operation	PGOOD mode
	PG check on power up	PG gates RESETBMCU
	EWARN delay	100 µs
	XFAIL operation	Disabled

Watchdog Monitoring	WD timer	Disabled
	WD window duration	1 ms
	WD clear window	Cleared within 100% timer
	WD expire number	Event on step 1
	Maximum WD event counter	1 Event
Clock Management	Nominal switching frequency	2.000 MHz
	SYNC mode	Disabled
	SYNCIN range	2000KHz to 2500KHz
	SYNCOUT enable	Disabled
	Frequency spread spectrum	Enabled
	FSS range	+/-5%

Table 3. Power Sequencer configuration

Functional block	Feature	OTP selection
Power Up Sequence	Sequence time base	250 µs
	SW1 sequence slot	Slot 0
	SW2 sequence slot	Slot 0
	RESETBMCU sequence slot	Slot 3
	PGOOD sequence slot	Slot 3
Power Down Sequence	Power down mode	Sequential
	SW1 Power down group	Group 4
	SW2 Power down group	Group 4
	RESETBMCU Power down	Group 4
	PGOOD Power down group	Group 4
	Power down delay	No delay

Power down delay	Group 1 power down delay	120 µs
	Group 2 power down delay	120 µs
	Group 3 power down delay	120 µs
	Group 4 power down delay	120 µs
	RESETBMCU group delay	No delay

Table 4. SW Regulator configuration

Functional block	Feature	OTP selection
SW1	Output voltage	0.70000 V
	UV detection threshold	96 %
	OV detection threshold	104 %
	Current limit	11.0 A
	Output inductor	0.47 µH
	Switching phase	0°
	PGOOD mode	Enabled
	SW1 OV Bypass	Protective behavior enabled
	SW1 UV Bypass	Protective behavior enabled
	SW1 ILIM Bypass	Protective behavior enabled
	DVS ramp	3.13/2.08 mV/µs
	SW1 gain margin	48.75 GM
SW2	Output voltage	0.70000 V
	UV detection threshold	96 %
	OV detection threshold	104 %
	Current limit	11.0 A
	Output inductor	0.47 µH

	Switching phase	180°
	PGOOD mode	Enabled
	SW2 OV Bypass	Protective behavior enabled
	SW2 UV Bypass	Protective behavior enabled
	SW2 ILIM Bypass	Protective behavior enabled
	DVS ramp	3.13/2.08 mV/µs
	SW2 gain margin	48.75 GM
SW Miscelleneaous	Switching Mode	PWM
	SW1 multi-phase selector	SW1/SW2 dual phase

Table 5. PROGRAM ID

Functional block	Feature	OTP selection
PROGRAM ID	Program ID High	A
	Program ID Low	1

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Date of release: 17/09/2021
Document identifier: R_MPF5200AMBA1ES