M68EM08SR12UM/D
REV. 2

M68EML08SR12

Emulator Module

User's Manual

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Section 1. General Information

1.1 Introduction

This section provides general information about the Motorola M68EML08SR12 emulator module (SR12EM)(Figure 1-1). This section also explains the two Motorola development systems that use the SR12EM.

The SR12EM lets you emulate and debug target systems based on MC68HC908SR12 microcontroller units (MCUs).

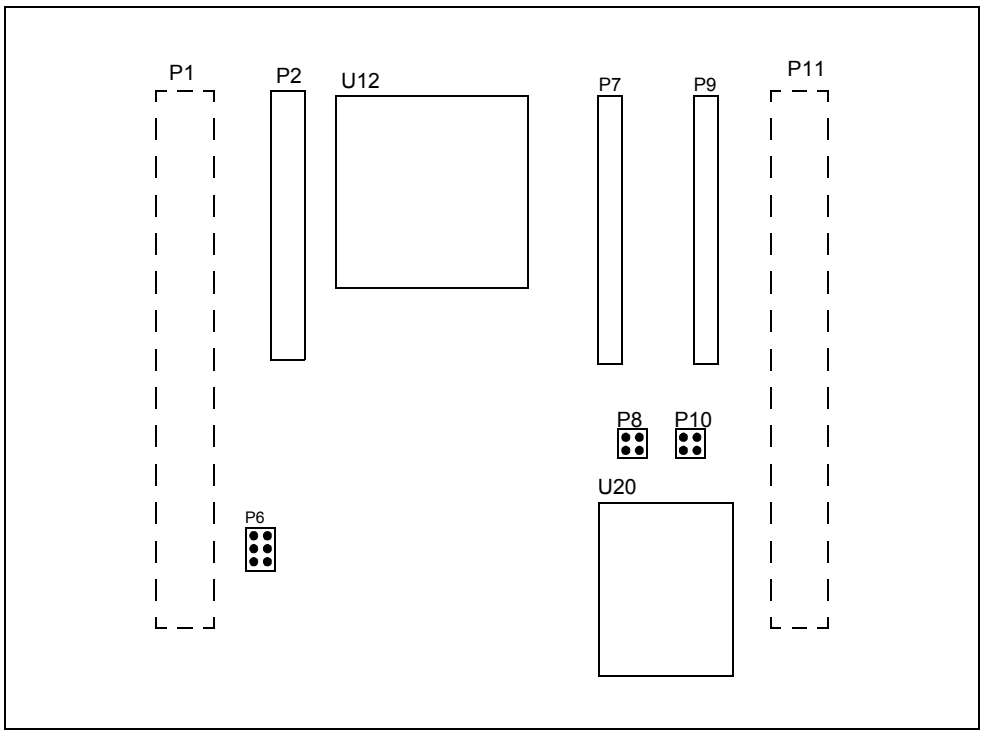


Figure 1-1. M68EML08SR12 Emulator Module

The main elements of the SR12EM are:

- DIN connectors P1 and P11 — Connect the EM to the MMDS control board or the MMEVS platform board

- Connector P2 — Permits connection to a logic analyzer
- Jumper header P8 and P10 — Select analog voltage supply and ground for the ADC module of the MC68HC908SR12
- Jumper header P6 — Selects the MCU clock source
- Connectors P7 and P9 — Customer-specific interfaces to the target system

The SR12EM requires a user-supplied 80-lead target cable and target head adapter to connect the target system to connectors P7 and P9.

1.2 Development Systems

The SR12EM can be part of two Motorola development systems:

- MMDS0508 Motorola Modular Development System (MMDS)
- MMEVS0508 Motorola Modular Evaluation System (MMEVS)

1.2.1 Motorola Modular Development System (MMDS)

The MMDS is an emulator system that provides a bus state analyzer and real-time memory windows. The unit's integrated design environment includes an editor, an assembler, user interface, and source-level debug.

A complete MMDS consists of:

- Station module — The metal MMDS enclosure containing the control board and the internal power supply
- Emulator module (EM) — A separately purchased printed circuit board that enables system functionality for a specific set of MCUs
- Two logic clip cable assemblies — Twisted-pair cables that connect the station module to the target system, a test fixture, a clock, an oscillator, or any other circuitry useful for evaluation or analysis. One end of each cable assembly has a molded connector, which fits into station-module pod A or pod B. Leads at the other end of each cable terminate in female probe tips. Ball clips come with the cable assemblies.

- 9-lead RS-232 serial cable — Cable that connects the station module to the host computer RS-232 port
- 9- to 25-pin adapter — A molded assembly that connects the 9-pin cable to a 25-pin serial port
- System software — MCUez software on CD-ROM and P&E Microcomputer System, Inc. software on CD-ROM
- MMDS documentation — *MMDS Operations Manual*, Motorola document order number MMDS0508OM/D; the MCUez™ software manual, included with the MCUezsoftware package; a system software manual, included with the P&E Microcomputer System, Inc.'s MMDS0508 software package; and this EM user's manual (this manual)

MMDS baud rates are user-selectable: 2400, 4800, 9600, 19,200, 38400, or 57600.

As mentioned, the SR12EM gives the MMDS the ability to emulate target systems based on MC68HC908SR12 MCUs. By substituting a different EM, you can enable your MMDS to emulate target systems based on a different MCU. (A local Motorola representative can explain all the EMs available.)

1.2.2 Motorola Modular Evaluation System (MMEVS)

An MMEVS is an economical, two-board tool for designing, debugging, and evaluating target systems based on MC68HC05 or MC68HC08 MCUs.

A complete MMEVS consists of:

- Platform board (PFB) — The bottom board, which supports the emulator module, and has connectors for power and for a terminal or host computer
- Emulator module (EM) — A separately purchased printed circuit board that enables system functionality for a specific set of MCUs
- RS-232 serial cable — A separately purchased cable that connects the PFB to the host computer RS-232 port
- System software — MCUez software on CD-ROM and P&E Microcomputer System, Inc. software on CD-ROM

- MMEVS documentation — *MMEVS Operations Manual*, Motorola document order number MMEVSOM/D; the MCUez software manual, included with the MCUez software package; a system software manual, included with the P&E Microcomputer System, Inc.'s MMEVS0508 software package; and this emulator user's manual

An MMEVS features automatic selection of the communication baud rate: 2400, 4800, 9600, 19,200, 38,400, or 57,600.

With an SR12EM, the MMEVS emulates target systems based on MC68HC908SR12 MCUs. By substituting a different EM, you can enable your MMEVS to emulate target systems based on a different MCU. (A local Motorola representative can explain all the EMs available.)

Section 2 explains how to configure and use the SR12EM as part of an MMDS or MMEVS system.

1.3 Specifications

Table 1-1 lists SR12EM specifications.

Table 1-1. SR12EM Specifications

Characteristics	Specifications
MCU extension I/O ports	HCMOS compatible
Operating temperature	0° to 40°C
Storage temperature	–40° to +85°C
Relative humidity	0 to 90% (non-condensing)
Power requirements	+5 V dc and +12 V dc (charge pump), provided from the MMDS control board or MMEVS platform board
Dimensions	8.5 x 5.7 inches (190 x 145 mm)
Weight	7.34 ounces (208g)

Section 2. Preparation and Installation

2.1 Introduction

This section explains how to configure your SR12EM, and how to install it in an MMDS (Motorola modular development system) or MMEVS (Motorola modular evaluation system). For other parts of system installation or configuration, see the MMDS or MMEVS hardware manuals.

NOTE: *It is possible to reconfigure an SR12EM already installed in an MMDS station module. To do so, switch off station-module power, then follow the guidance in this section. Similarly, it is possible to reconfigure an SR12EM already installed on an MMEVS platform board, provided that platform-board power is disconnected.*

CAUTION: *Be sure to switch off or disconnect power when reconfiguring an installed EM. Reconfiguring EM jumper headers with the power on can damage system circuits.*

ESD CAUTION: *Motorola development systems include open-construction printed circuit boards that contain static-sensitive components. These boards are subject to damage from electrostatic discharge (ESD). To prevent such damage, you must use static-safe work surfaces and grounding straps, as defined in ANSI/EOS/ESD S6.1 and ANSI/EOS/ESD S4.1. All handling of these boards must be in accordance with ANSI/EAI 625.*

2.2 Hardware Preparation

This subsection explains SR12EM limitations and configuration.

2.2.1 SR12EM Limitations

The SR12EM emulates I/O pins PTA0-PTA5, but does not override the pin functions if these pins are configured as ADC channels. You must configure the appropriate I/O pins as input ports before you use the ADC function, or ADC conversions may not be correct.

The SR12EM does not support direct LED drive capability on lines PTA0-PTA5.

For the SR12EM, register LEDA is a write-only register.

2.2.2 Configuring Jumper Headers

The SR12EM has three jumper headers, which Table 2-1 explains.

Table 2-1 Jumper Headers

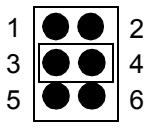
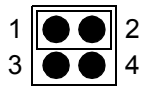
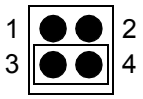
Jumper Header	Type (Factory default shown)	Description
P6 CLOCK SOURCE		Jumper between pins 1 and 2: Selects an external target system as the clock source. The OSC1 input signal must arrive at connector 9, pin 39. Jumper between pins 3 and 4 (factory default): Selects the on-board, 32.768-kHz crystal oscillator. Jumper between pins 5 and 6: Selects the clock signal from the MMDS control board or MMEVS platform board. *NOTE: Insert only one jumper in header P6. Inserting multiple jumpers could damage your SR12EM.*
P8 ADC VOLTAGE SOURCE		Jumper between pins 1 and 2 (factory default): Selects the on-board, isolated analog voltage source (LVDD), as input for the SR12EM analog-digital converter (ADC) module. Jumper between pins 3 and 4: Selects the target system analog voltage signal (VDDA), as input for the SR12EM ADC module.

Table 2-1 Jumper Headers (Continued)

Jumper Header	Type (Factory default shown)	Description
P10 ADC GROUND SOURCE		Jumper between pins 1 and 2: Selects the target system ground signal (VSSA), as input for the SR12EM ADC module. Jumper between pins 3 and 4 (factory default): Selects on-board ground (GND), as input for the SR12EM ADC module.

2.3 Remaining System Installation

When all jumper headers are configured, follow these steps to complete SR12EM installation:

- To install the SR12EM in an MMDS station module:
  - Remove the access panel of the station-module enclosure,
  - Insert the EM through the access-panel opening,
  - Fit together EM connectors P1 and P11 (on the bottom of the board) and control-board connectors P1 and P2,
  - Snap the corners of the EM onto the plastic standoffs,
  - Make cable connections to the EM, draping the cables through the side of the access-panel opening, and
  - Replace the access panel, so that cables exit the station-module enclosure through the slit at the side of the enclosure.
- To install the SR12EM on an MMEVS platform board, fit together EM connectors P1 and P11 (on the bottom of the board) and platform-board connectors P3 and P4. Snap the corners of the EM onto the plastic standoffs.

- Copy these personality files from the provided diskette to the directory that contains the debugging software:
  - 00459Vxx.MEM — P&E Personality file for the M68EML08SR12 MCU
  - 00C59Vxx.MEM — MCUez Personality file for the M68EML08SR12 MCU

At this point, make any remaining system cable connections and apply power power. For instructions, consult the MMDS or MMEVS operations manuals. installation, remaining system; remaining system installation

Section 3. Support Information

3.1 Introduction

This section consists of pin assignments and signal descriptions for SR12EM target and logic analyzer connectors.

3.2 Logic Analyzer Connector (P2)

Connector P2 is the SR12EM logic analyzer connector. Figure 3-1 shows the pin assignments for this connector; Table 3-1 gives the signal descriptions for this connector.

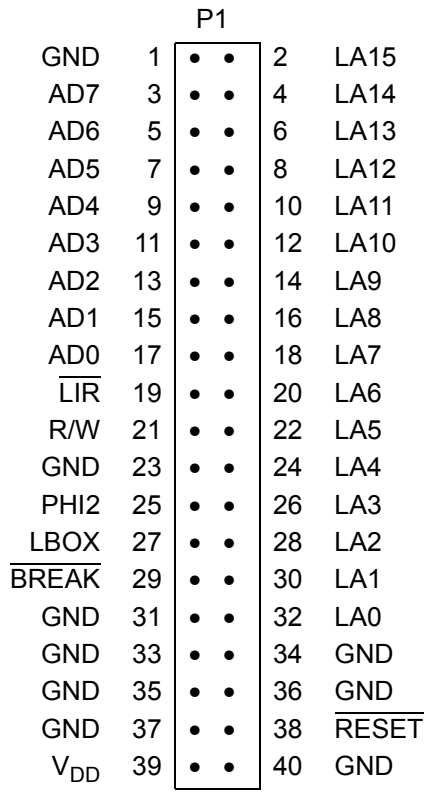


Figure 3-1. Logic Analyzer Connector P2 Pin Assignments

Table 3-1. Logic Analyzer Connector P2 Signal Descriptions

Pin	Mnemonic	Signal
1	GND	GROUND
2	LA15	Address bus bit 15 — MCU output address bus
3	AD7	Data bus bit 7 — MCU bidirectional data bus
4	LA14	Address bus bit 15 — MCU output address bus
5	AD6	Data bus bit 6 — MCU bidirectional data bus
6	LA13	Address bus bit 13 — MCU output address bus
7	AD5	Data bus bit 5 — MCU bidirectional data bus
8	LA12	Address bus bit 12 — MCU output address bus
9	AD4	Data bus bit 4 — MCU bidirectional data bus
10	LA11	Address bus bit 11 — MCU output address bus
11	AD3	Data bus bit 3 — MCU bidirectional data bus
12	LA10	Address bus bit 10 — MCU output address bus
13	AD2	Data bus bit 2 — MCU bidirectional data bus
14	LA9	Address bus bit 9 — MCU output address bus
15	AD1	Data bus bit 1 — MCU bidirectional data bus
16	LA8	Address bus bit 8 — MCU output address bus
17	AD0	Data bus bit 0 — MCU bidirectional data bus
18	LA7	Address bus bit 7 — MCU output address bus.
19	$\overline{\text{LIR}}$	Load instruction register — Active-low output signal, asserted when an instruction starts
20	LA6	Address bus bit 6 — MCU output address bus
21	R/W	Read/Write — Output signal that indicates the direction of data transfer
22	LA5	Address bus bit 5 — MCU output address bus
23	GND	GROUND
24	LA4	Address bus bit 4 — MCU output address bus
25	PHI2	PHI2 clock — Internally generated output clock signal used as a timing reference
26	LA3	Address bus bit 3 — MCU output address bus

Table 3-1. Logic Analyzer Connector P2 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
27	LBOX	Last bus cycle — Input signal that the emulator asserts to indicate that the target system MCU is in the last bus cycle of an instruction
28	LA2	Address bus bit 2 — MCU output address bus
29	$\overline{\text{BREAK}}$	$\overline{\text{BREAK}}$ — Active low signal that the EM asserts to stop the target system MCU from running user code
30	LA1	Address bus bit 1 — MCU output address bus
31	GND	GROUND
32	LA0	Address bus bit 0 — MCU output address bus
33	GND	GROUND
34	GND	GROUND
35	GND	GROUND
36	GND	GROUND
37	GND	GROUND
38	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ — Active-low bidirectional signal for starting an EVS reset
39	V_{DD}	+5 Vdc power — Input voltage (+5 Vdc @ 1A (max)) used by the EM logic circuits
40	GND	GROUND

3.3 Target Connectors (P7 and P9)

The SR12EM has two target connectors: P7 and P9, each a 2-row by 20-pin connector.

Figure 3-2 shows the pin assignments for both these connectors. Table 3-2 lists the signal descriptions for connector P7, and Table 3-3 lists the signal descriptions for connector P9.

P7					P9				
GND	1	•	2	V_{DD}	NC	1	•	2	PTC3
PTC5	3	•	4	GND	PTA5	3	•	4	PTD0
PTC6	5	•	6	LV_{DD}	PTC4	5	•	6	EVDD
VDDA	7	•	8	NC	VSSA	7	•	8	NC
NC	9	•	10	NC	GND	9	•	10	NC
PTA3	11	•	12	NC	PTA4	11	•	12	NC
PTA1	13	•	14	NC	PTA2	13	•	14	GND
VREFL	15	•	16	PTB6	VREFH	15	•	16	NC
OPIN2	17	•	18	PTB4	PTC7	17	•	18	PTB5
GND	19	•	20	OPIN1	PTA0	19	•	20	VSSAM
PTC2	21	•	22	PTD6	PTC1	21	•	22	PTC0
NC	23	•	24	GND	PTA7	23	•	24	PTD5
PTD7	25	•	26	PTB3	PTA6	25	•	26	PTD4
NC	27	•	28	PTB1	GND	27	•	28	PTB2
NC	29	•	30	PTD3	NC	29	•	30	PTB0
NC	31	•	32	RESET	NC	31	•	32	GND
NC	33	•	34	IRQ1	NC	33	•	34	PTD2
NC	35	•	36	GND	NC	35	•	36	PTD1
NC	37	•	38	GND	NC	37	•	38	GND
NC	39	•	40	GND	OSC1	39	•	40	GND

Figure 3-2. Target Connectors P7 and P9 Pin Assignments

Table 3-2. Target Connector P7 Signal Descriptions

Pin	Mnemonic	Signal
1	GND	EM GROUND — Ground signal of the EM board
2	V_{DD}	MMDS +5 V — Used for factory testing
3	PTC5	PORT C (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
4	GND	EM GROUND — Ground signal of the EM board
5	PTC6	PORT C (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
6	LV_{DD}	SR12EM Voltage high — Used for factory testing
7	VDDA	Analog supply pin for ADC convertor
8 -10	NC	No connect
11	PTA3	PORT A (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
12	NC	No connect
13	PTA1	PORT A (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
14	NC	No connect
15	VREFL	ADC voltage reference low
16	PTB6	PORT B (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
17	OPIN2	ADC input channel 2
18	PTB4	PORT B (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
19	GND	EM GROUND — Ground signal of the EM board
20	OPIN1	ADC input channel 1
21	PTC2	PORT C (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
22	PTD6	PORT D (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
23	NC	No connect
24	GND	EM GROUND — Ground signal of the EM board
25	PTD7	PORT D (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers

Table 3-2. Target Connector P7 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
26	PTB3	PORT B (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
27	NC	No connect
28	PTB1	PORT B (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
29	NC	No connect
30	PTD3	PORT D (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
31	NC	No connect
32	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ — Active-low bidirectional control line that initializes the MCU
33	NC	No connect
34	$\overline{\text{IRQ1}}$	INTERRUPT REQUEST — Active-low input line for requesting MCU asynchronous non-maskable interrupt
35	NC	No connect
36	GND	EM GROUND — Ground signal of the EM board
37	NC	No connect
38	GND	EM GROUND — Ground signal of the EM board
39	NC	No connect
40	GND	EM GROUND — Ground signal of the EM board

Table 3-3. Target Connector P9 Signal Descriptions

Pin	Mnemonic	Signal
1	NC	No connect
2	PTC3	PORT C (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
3	PTA5	PORT A (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
4	PTD0	PORT D (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
5	PTC4	PORT C (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
6	EVDD	Target system Voltage high
7	VSSA	Analog ground pin for ADC convertor
8	NC	No connect
9	GND	EM GROUND — Ground signal of the EM board
10	NC	No connect
11	PTA4	PORT A (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
12	NC	No connect
13	PTA2	PORT A (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
14	GND	EM GROUND — Ground signal of the EM board
15	VREFH	ADC voltage reference high
16	NC	No connect
17	PTC7	PORT C (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
18	PTB5	PORT B (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
19	PTA0	PORT A (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
20	V_{SSAM}	Analog module ground pin
21	PTC1	PORT C (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
22	PTC0	PORT C (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers

Table 3-3. Target Connector P9 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
23	PTA7	PORT A (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
24	PTD5	PORT D (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
25	PTA6	PORT A (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
26	PTD4	PORT D (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
27	GND	EM GROUND — Ground signal of the EM board
28	PTB2	PORT B (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
29	NC	No connect
30	PTB0	PORT B (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
31	NC	No connect
32	GND	EM GROUND — Ground signal of the EM board
33	NC	No connect
34	PTD2	PORT D (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
35	NC	No connect
36	PTD1	PORT D (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
37	NC	No connect
38	GND	EM GROUND — Ground signal of the EM board
39	OSC1	OSCILLATOR — Crystal oscillator amplifier input signal
40	GND	EM GROUND — Ground signal of the EM board

3.4 Target Cable Assembly

To connect the SR12EM to a target system, a separately purchased target cable assembly is needed, plus the appropriate target head and target-head/adapter package.

Figure 3-3 shows how one end of the flex cable plugs into the SR12EM module, and it also shows how the target head connects into the target system.

If the SR12EM is installed in the MMDS station module, run the flex cable through the slit in the station-module enclosure.

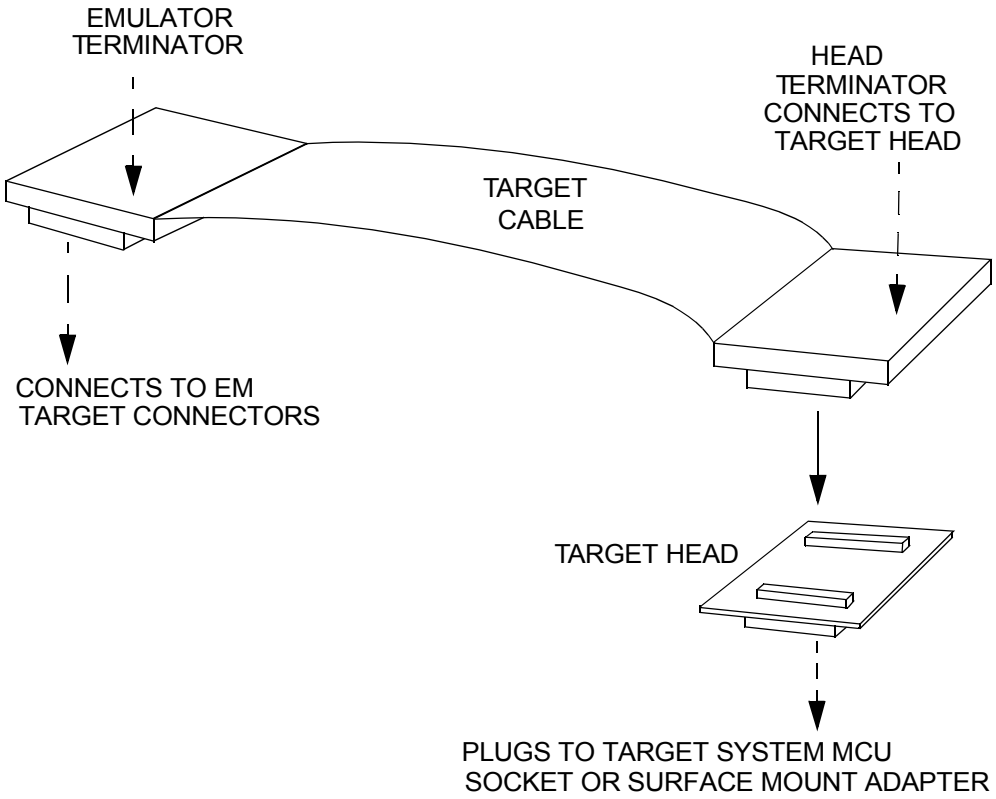


Figure 3-3. Target Cable Assembly

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