
THE POWER
MOSFET
APPLICATION
HANDBOOK
DESIGN ENGINEER'S GUIDE
NXP

The Power MOSFET Application Handbook

Design Engineer’s Guide

NXP Semiconductors

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Contributors:

Andrew Berry
Adam Brown
Brian Clifton
Jamie Dyer
Phil Ellis
Mark Fang
Keith Heppenstall
Chris Hill
Kelly Law
Wayne Lawson
Koji Nishihata
Jim Parkin
Christos Pateropoulos
Phil Rutter

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Introduction

Drawing on over 20 years' of experience, the Power MOSFET Application Handbook brings together a comprehensive set of learning and reference materials relating to the use of power MOSFETs in real world systems. MOSFETs are used in a range of fields, from automotive and industrial to computing, mobile and power supply, all of which have influenced the development of the material presented within this handbook.

This book is aimed at engineers from any industry who have need or interest in increasing their understanding of how to design with power MOSFETs. The knowledge shared within this reference guide has been collected and developed through years of working with many different engineers from many different companies to solve real problems. Although MOSFET technology has moved on significantly in the last decades, many of the challenges facing designers remain the same. The goal of this book is to give insight into the sometimes confusing and complex behaviour of power MOSFETs and provide engineers with the information necessary to solve common problems and avoid potential pitfalls.

Further product information and recently published application notes can be found at www.nxp.com/mosfets

Chapter 1: Understanding power MOSFET data sheet parameters

Chapter 1: Understanding power MOSFET data sheet parameters

1.1 Introduction

This chapter explains the parameters and diagrams given in an NXP Semiconductors Power MOSFET data sheet. The goal is to help an engineer decide what device is most suitable for a particular application.

It is important to pay attention to the conditions for which the parameters are listed, as they can vary between suppliers. These conditions can affect the values of the parameters making it difficult to choose between different suppliers. Throughout this chapter, the data sheet for the BUK7Y12-55B is used as an example. BUK7Y12-55B is an automotive-qualified part in an SOT669 (LFPAK56) package, with a voltage rating of 55 V.

The layout of this data sheet is representative of the general arrangement of NXP power MOSFET data sheets.

NXP Power MOSFETs are designed with particular applications in mind. For example, switching charge is minimized where switching losses dominate, whereas on-resistance is minimized where conductive losses dominate.

1.2 Data sheet technical sections

1.2.1 Product profile

This section provides the overview of the device; giving the designer the key information regarding device suitability. The general description describes the technology used; key features and example applications are listed.

The quick reference data table contains more detailed information and the key parameters for the intended application. An example of a quick reference data table is shown in **Table 1** “Quick reference data”.

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	55	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 25$ °C; **Figure 1**	-	-	61.8	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; **Table 3**	-	-	105	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 20$ A; $T_j = 25$ °C;	-	8.2	12	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 20$ A; $V_{DS} = 44$ V; $V_{GS} = 10$ V;	-	14.8	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain source avalanche energy	$I_D = 61.8$ A; $V_{sup} \leq 55$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C: unclamped	-	-	129	mJ

The general format for describing a parameter is to provide the official symbol and then the correct parameter name. Any relevant conditions and information are listed after the parameter names. The values and units of the values are entered in the last two columns. All entries conform to IEC60747-8.

The quick reference data parameters are described in more detail in the characteristics section of the data sheet. The following list is an introduction to some of the key issues together with their interpretation:

V_{DS} - the maximum voltage between drain and source that the device is guaranteed to block in the off state. This section of the data sheet deals with the most commonly used temperature range, as opposed to the full temperature range of the device.

I_D - the maximum continuous current the device can carry with the mounting base held continuously at 25 °C with the device fully on. In the example provided in **Table 1**, I_D requires a V_{GS} of 10 V.

P_{tot} - the maximum continuous power the device can dissipate with the mounting base held continuously at 25 °C.

$R_{DS(on)}$ (drain-source on state resistance) - the typical and maximum resistance of the device in the on-state under the conditions described. $R_{DS(on)}$ varies greatly with both T_j and the gate-source voltage (V_{GS}). Graphs are provided in the data sheet to assist in determining $R_{DS(on)}$ under various conditions.

Q_{GD} (gate-drain charge) - an important switching parameter that relates to switching loss, along with Q_{GS} and $Q_{G(tot)}$. Q_{GD} is inversely proportional to $R_{DS(on)}$, therefore choosing an appropriate balance between $R_{DS(on)}$ and Q_{GD} is critical for optimal circuit performance.

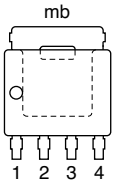
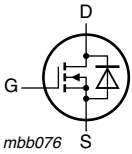
Q_{OSS} (output charge) - an increasingly important switching parameter in modern MOSFETs, as the other switching parameters have been optimized.

$E_{DS(AL)S}$ (non-repetitive drain-source avalanche energy) - describes the maximum energy allowed in any voltage spike or pulse that exceeds the V_{DS} rating of the device. Exceeding this rating, runs the risk of damaging the device. This parameter describes what is commonly referred to as “ruggedness” that is the ability of the device to withstand overvoltage events.

1.2.2 Pinning information

This section describes the internal connections and general layout of the device. Note that the symbol is for an enhancement n-channel MOSFET with the source and body tied together, and a parallel diode between the source and drain. The parallel diode is known as the body diode and is inherent in power MOSFETs. N-channel power MOSFETs have the body diode between drain and source, as shown in **Table 2**.

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mount base: connected to drain		

1.2.3 Ordering information

The ordering section provides information on how to order the device.

1.2.4 Limiting values

The limiting values table provides the range of operating conditions allowed for the MOSFET. The conditions are defined in accordance with the absolute maximum rating system (IEC60134). Operation outside of these conditions is not guaranteed, so it is recommended that these values are not exceeded. Doing so runs the risk of immediate device failure or reduced lifetime of the MOSFET. The avalanche ruggedness conditions, when given, describe the limited conditions for which the V_{DS} rating can be exceeded.

To calculate how the limiting values change with temperature, they are read together with the derating curves provided.

The limiting values table for the BUK7Y12-55B is given as an example of a standard limiting values table, in **Table 3**.

Table 3. Limiting values

In accordance with the absolute maximum rating system IEC 60134

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\ \Omega$	-	-	55	V
V_{GS}	gate-source voltage		-20	-	+20	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 25$ °C; Table 1; Figure 1	-	-	61.8	A
		$V_{GS} = 10$ V; $T_{mb} = 100$ °C; Table 1	-	-	43.7	A
I_{DM}	peak drain current	$V_{GS} = 10$ V; $T_{mb} = 25$ °C; pulsed; Figure 1	-	-	247	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C	-	-	105	W
T_{stg}	storage temperature		-55	-	+175	°C
T_j	junction temperature		-55	-	+175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25$ °C	-	-	61.8	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C	-	-	247	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 61.8$ A; $V_{sup} \leq 55$ V; $R_{GS} = 50\ \Omega$; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C: unclamped	-	-	129	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3 [1] [2] [3]	-	-	-	mJ

[1] Single pulse avalanche rating limited by a maximum junction temperature of 175 °C

[2] Repetitive avalanche rating limited by an average junction temperature of 170 °C

[3] Refer to application note AN10273 (Chapter 2 of this book) for further information

V_{DS} (drain-source voltage) - the maximum voltage the device is guaranteed to block between the drain and source terminals in the off-state for the specified temperature range. For the BUK7Y12-55B, the temperature range is from +25 °C to +175 °C. For operation below 25 °C, the V_{DS} rating reduces due to the positive temperature coefficient of avalanche breakdown. This is covered in **Section 1.2.4.1** of this chapter.

V_{GS} (gate-source voltage) - the maximum voltage the device is specified to block between the gate and source terminals. Some NXP data sheets specify different values for DC and pulsed V_{GS}. In these cases the DC value is a constant gate voltage over the lifetime of the device at the maximum T_j, whilst the higher-value pulsed-rating is for a shorter, specified accumulated pulse duration at the maximum specified T_j.

Gate-oxide lifetime reduces with increasing temperature and/or increasing gate voltage. This means that V_{GS} lifetimes or ratings quoted for lower junction temperatures are significantly greater than if specified at higher temperatures. This can be important when comparing data sheet values from different manufacturers.

V_{DGR} (drain-gate voltage) is typically the same value as the V_{DS} rating.

I_D (drain current) - the maximum continuous current the device is allowed to carry under the conditions described. This value can be related to either package construction, or the maximum current that would result in the maximum T_j. As such it depends on an assumed mounting base temperature (T_{mb}), the thermal resistance (R_{th}) of the device, and its $R_{DS(on)}$ at maximum T_j.

Note that some suppliers quote the “theoretical” silicon limit, while indicating the package limited limit in the characteristic curves.

I_{DM} (peak drain current) - the maximum drain current the device is allowed to carry for a pulse of 10 µs or less.

P_{tot} (total power dissipation) is the maximum allowed continuous power dissipation for a device with a mounting base at 25 °C. The power dissipation is calculated as that which would take the device to the maximum allowed junction temperature while keeping the mounting base at 25 °C. In reality, it is difficult to keep the mounting base at this temperature while dissipating the 105 W that is the calculated power dissipation for the BUK7Y12-55B. In other words, P_{tot} indicates how good the thermal conductivity of the device is, and its maximum allowed junction temperature.

Note that some other semiconductor vendors quote performance when mounted on a copper PCB usually 1 inch square. In practice, this information is rather meaningless as the semiconductor vendor has no control over how the device is cooled. See AN10874 - LFPAK MOSFET thermal design guide. AN10874 (Chapter 4 of this book) describes different techniques that can be used during the design phase to ensure that the PCB layout provides optimum thermal performance.

T_{stg} (storage temperature) is the temperature range in which the device can be stored without affecting its reliability. Long term storage should be in an inert atmosphere to prevent device degradation, for example, by tarnishing of the metal leads.

T_j (junction temperature) is the operational temperature range of the device. Typically, T_j is the same as the storage temperature. Outside of this range, device parameters are outside the range of the data sheet and device lifetime is reduced.

I_S (source current) - the maximum continuous current of the MOSFET body diode, which is briefly discussed in **Section 1.2.2**. The same considerations apply as for I_D.

I_{SM} (peak source current) - the maximum current pulse that the MOSFET body diode is guaranteed to carry. The same considerations apply as for I_{DM}.

$E_{DS(AL)S}$ (non-repetitive drain-source avalanche energy) - the maximum allowed single overvoltage energy pulse under the conditions specified. For this example, the conditions are the maximum continuous drain current allowed for a mounting base temperature of 25 °C. The avalanche energy allowed is the energy pulse that would raise the device temperature from 25 °C to its maximum allowed T_j, while the mounting base temperature is held at 25 °C.

The avalanche energy is specified for the maximum continuous drain current. Some vendors specify the avalanche energy for a different current and higher inductive load, which can increase the apparent avalanche energy for an inferior performance. An example is given with the derating curve as described in **Section 1.2.4.3** of this chapter.

$E_{DS(AL)R}$ (repetitive drain-source avalanche energy) - the maximum amount of energy allowed in any single avalanche event when there is more than one avalanche event. There are thermal constraints on a repeated avalanche operation that are in **Section 1.2.4.3** of this chapter. There are also the standard thermal requirements in addition to the energy requirements for repetitive avalanche events. These requirements are assessed with the thermal characteristic curves as described in **Section 1.2.5**. *Avalanche performance is covered in detail in application note AN10273 (Chapter 2 of this book).*

This parameter is only listed on NXP data sheets where the repetitive avalanche capability has been assessed. It is not shown in NXP data sheets where it has not been assessed, for example non-automotive MOSFETs.

1.2.4.1 Derating curves

The derating curves are provided immediately after the tabulated limiting value data, and help the designer calculate how the limits change with temperature.

1.2.4.1.1 Continuous drain current

The followings procedure serves as an example to calculate the maximum continuous drain current for the BUK7Y12-55B. Assume an application with a mounting base temperature T_{mb} of 75 °C.

Refer to the graph depicted in **Figure 1** which depicts the continuous drain current as a function of mounting base temperature.

Figure 1 shows that for a T_{mb} of 75 °C, the maximum continuous drain current has reduced from 61.8 A, listed at 25 °C, to 50 A.

The maximum current at any T_{mb}, is the current that increases T_j to the maximum allowed temperature (175 °C). $P = I^2 \times R_{DS(on)}$ represents the power dissipation at T_j, where the $R_{DS(on)}$ used is the maximum value for the maximum T_j. Therefore, the allowed current is proportional to the square root of the allowed power dissipation.

The power dissipation allowed for a given T_{mb} is proportional to the allowed temperature increase. This means that the derating curve shown, is based on the following equations:

$$(1)\quad I_D^{\,2}(T_{mb}) \propto \frac{T_j - T_{mb}}{T_j - 25\ ^{\circ}C}$$

$$(2)\quad I_D(T_{mb}) = I_D(25\ ^{\circ}C) \times \sqrt{\frac{T_j - T_{mb}}{T_j - 25\ ^{\circ}C}}$$

At the maximum allowed junction temperature of 175 °C, this current has decreased to zero.

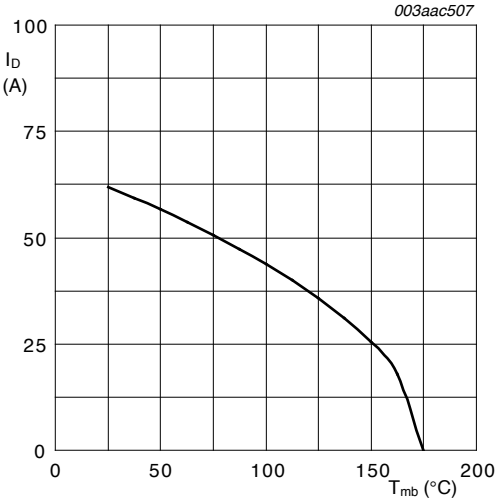


Fig 1. Continuous drain current as a function of mounting base temperature

1.2.4.2 Power dissipation

Power dissipation varies with different temperatures. However, in this case, the power dissipation curve is normalized. The allowed power is presented as a percentage of the allowed power dissipation at 25 °C, as opposed to an absolute value.

Example:

By observing the curve in **Figure 2**, the allowed power dissipation for a T_{mb} of 75 °C is approximately 66 % of that allowed at 25 °C.

The graphic data in **Figure 2**, shows the maximum continuous power dissipation (P_{tot}) at 25 °C is 105 W.

This means that the maximum power dissipation allowed at 75 °C, is 66 % of 105 W which is 70 W.

Equation 3 is the equation to calculate power dissipation:

$$(3)\quad P_{tot}(T_{mb}) = P_{tot}(25\ ^{\circ}C) \times \frac{T_j - T_{mb}}{T_j - 25\ ^{\circ}C}$$

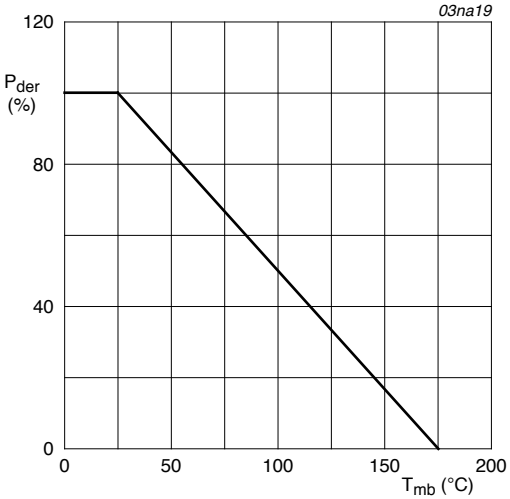
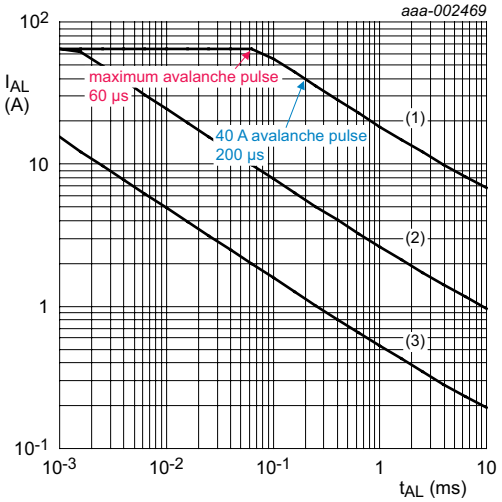


Fig 2. Normalized total power dissipation as a function of mounting base temperature

The curves provided in **Figure 1** and **Figure 2** are read in conjunction with the limiting values tables. The information extracted, assists in calculating the maximum current allowed and the power dissipation with respect to temperature.

1.2.4.3 Avalanche ruggedness

Avalanche ruggedness is covered in detail in AN10273 (Chapter 2 of this book).



Single-shot and repetitive avalanche rating

(1) Single pulse; T_j = 25 °C

(2) Single pulse; T_j = 150 °C

(3) Repetitive

Fig 3. Avalanche current as a function of avalanche period

A simple example for the BUK7Y12-55B, using the information in AN10273 (Chapter 2 of this book), is extracted from the limiting values **Table 3**:

With I_D = 61.8 A, $V_{sup} \leq$ 55 V, R_{GS} = 50 Ω, V_{GS} = 10 V and $T_{j(init)}$ = 25 °C unclamped, the maximum $E_{DS(AL)S}$ is 129 mJ.

An avalanche event has a triangular pulse shape, so the average power is calculated as ($0.5 \times V_{DS} \times I_{DS}$).

AN10273 (Chapter 2 of this book) states that the assumed breakdown voltage is 130 % of the rated voltage (55 V × 1.3).

Figure 3 shows a maximum current of just above 60 A at 25 °C (the limiting values **Table 3** shows that it is actually 61.8 A).

The time for the maximum avalanche energy can be read from **Figure 3** as 60 µs.

This means that the maximum avalanche energy allowed is: 0.5 × (55 V × 1.3) × 61.8 A × 60 µs = 133 mJ.

This value is approximately the 129 mJ quoted in the limiting value **Table 3**.

If a competitor quotes avalanche energy at 40 A, the graph shows that the avalanche time is now 200 µs. The avalanche energy is now 0.5 × (55 V × 1.3) × 40 A × 200 µs = 286 mJ.

Ruggedness events lie outside the Safe Operating Area (SOA).

1.2.4.4 Safe Operating Area (SOA)

The Safe Operating Area (SOA) curves are some of the most important on the data sheet.

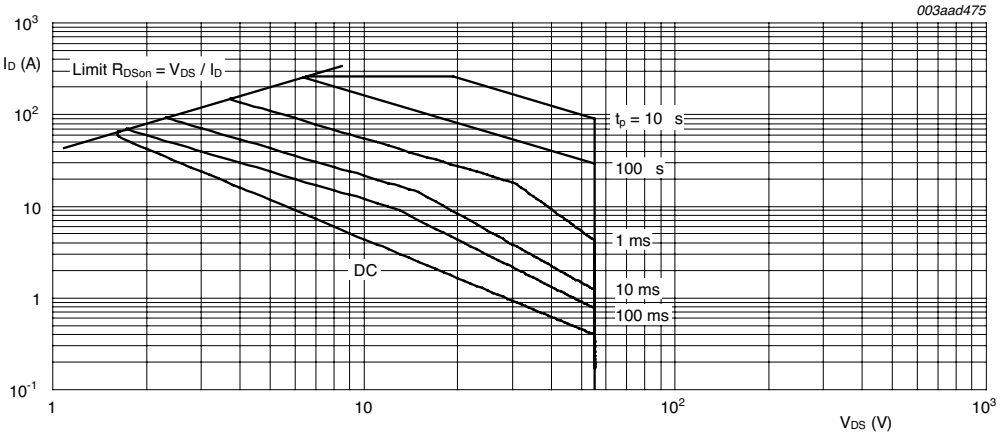


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

The SOA curves show the voltage allowed, the current and time envelope of operation for the MOSFET. These values are for an initial T_{mb} of 25 °C and a single current pulse. This is a complex subject which is further discussed in the appendix (**Section 1.3.1**).

1.2.5 Thermal characteristics

This section describes the thermal impedance as a function of pulse duration for different duty cycles. This information is required to determine the temperature that the silicon reaches under particular operating conditions, and whether it is within the guaranteed operation envelope.

The thermal characteristics are shown in **Figure 5**. The thermal impedance changes with pulse length because the MOSFET is made from different materials. For shorter durations, the thermal capacity is more important, while for longer pulses, the thermal resistance is more important.

The thermal characteristics are used to check whether particular power loading pulses above the DC limit would take T_j above its safe maximum limit. Repetitive avalanche pulses must be considered in addition to the constraints specific to avalanche and repetitive avalanche events.

Table 4. Characteristics table

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see **Figure 5**	-	-	1.42	K/W

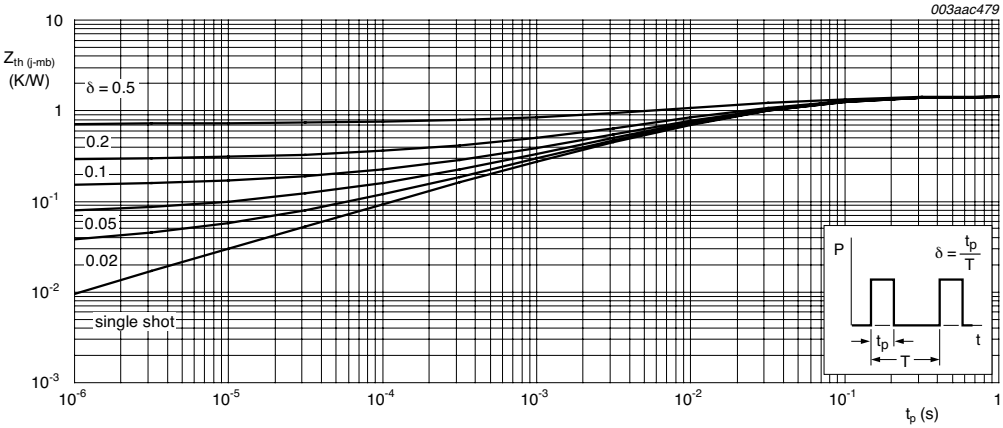


Fig 5. Thermal characteristics

Thermal resistance (R_{th}) and thermal impedance (Z_{th}) are related because the thermal resistance is the steady-state measure of how the device blocks heat flow. Thermal impedance is how the device responds to transient thermal events. It involves different thermal capacities of parts of the device and the thermal resistances between these parts.

Under DC conditions, Z_{th} is equal to R_{th}. **Equation 4** represents the temperature rise for a particular power dissipation:

(4) $$\Delta T_j = \left|Z_{th(j-mb))}\right| \times Power$$

A worked example is discussed in the appendix (**Section 1.3.1.2**).

1.2.6 Electrical characteristics

This section is used to determine whether the MOSFET would be suitable in a particular application. This section differs from the previous two sections that are used to determine whether the MOSFET would survive within the application. The examples in this section are taken from the data sheet for the BUK7Y12-55B unless otherwise stated.

1.2.6.1 Static characteristics

The static characteristics are the first set of parameters listed in this section and an example is shown in **Table 5**:

Table 5. Static characteristics

List of constants and limitations relating to the table i.e. voltages, currents and temperatures

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	55	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = −55 °C	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C	2	3	4	V
		I_D = 250 mA; V_{DS} = V_{GS}; Tj = −55 °C	-	-	4.4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C	1	-	-	V

Table 5. Static characteristics...continued

List of constants and limitations relating to the table i.e. voltages, currents and temperatures

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DSS}	drain leakage current	V_{DS} = 55 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	1	µA
		V_{DS} = 55 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 20 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = −20 V; T_j = 25 °C	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 175 °C;	-	-	27.6	m Ω
		V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C;	-	8.2	12	m Ω

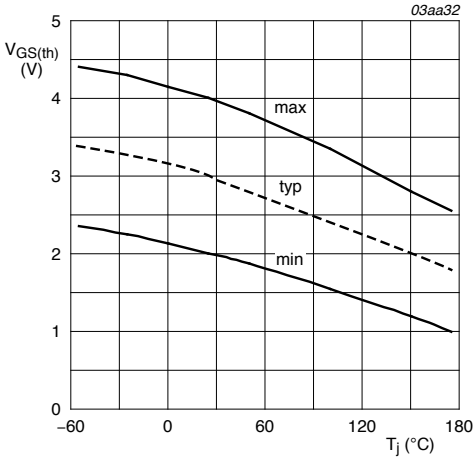
$V_{BR(DSS)}$ (drain-source breakdown voltage) - an expansion of the parameter listed and explained in **Section 1.2.4**. This section lists the maximum voltage the device is guaranteed to block between the drain and source terminals in the off-state over the entire MOSFET temperature range. The temperature range is from −55 °C to +175 °C. The current between the drain and the source terminals of the BUK7Y12-55B, is guaranteed to be below 250 µA for the voltage and temperature range. The range is 50 V or less if the device is cooler than +25 °C, and 55 V or below if the device is between +25 °C and +175 °C.

The effect of temperature on the off-state characteristics is twofold. The leakage current increases with temperature, turning the device on. Competing against the leakage current increase, the breakdown voltage also increases with temperature.

$V_{GS(th)}$ (gate-source threshold voltage) is important for determining the on-state and the off-state of the MOSFET. $V_{GS(th)}$ is defined where $V_{DS} = V_{GS}$, although it is sometimes quoted for a fixed V_{DS} (e.g. 10 V).

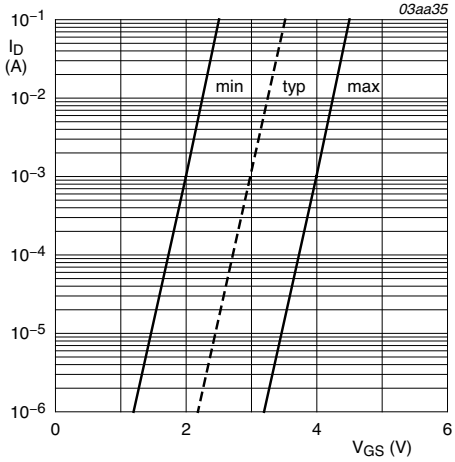
Note that the definition of the threshold voltage for a particular current where the gate and drain are shorted together, can differ from examples in textbooks. The parameter in textbooks describes a change in the physical state of the MOSFET and is independent of the MOSFET chip size. The parameter used in the data sheet is for a specified current and is dependent on the chip size, as the current flow is proportional to the chip area.

The threshold voltage in the data sheet is defined in a way that is best for routine measurement, but not how the actual device would typically be used. Consequently, the graphs provided in **Figure 6** support the parameter.



Gate-source threshold voltage as a function of junction temperature

I_D = 1 mA; V_{DS} = V_{GS}



Subthreshold drain current as a function of gate-source voltage

T_j = 25 °C; V_{DS} = 5 V

Fig 6. Supporting figures for threshold voltage parameter

The first graph shows the variation in the threshold voltage for the typical and limit devices over the rated temperature range. All the MOSFETs are guaranteed to have a threshold voltage between the lines.

Consequently, for the BUK7Y12-55B at 25 °C, if V_{DS} and V_{GS} are both less than 2 V, all devices carry less than 1 mA. Also, all devices carry more than 1 mA if V_{DS} and V_{GS} are both greater than 4 V. At 175 °C, the lower limit has fallen to 1 V, while the upper limit has fallen to 2.5 V. The lower limit is usually more important as it determines when the device is guaranteed to be turned off, and what noise headroom an application needs.

The second graph shows how the device turns on around this threshold voltage. For the BUK7Y12-55B, the current increases 100,000 times for an increase in gate voltage of less than 1 V. An example is given for the situation when the drain-source voltage is fixed at 5 V.

I_{DSS} (drain leakage current) guarantees the maximum leakage current that the device passes at its maximum rated drain-source voltage during the off-state. It is important to note how much higher I_{DSS} is at high temperature, which is the worst case.

I_{GSS} (gate leakage current) guarantees the maximum leakage current through the gate of the MOSFET. The I_{GSS} is important when calculating how much current is required to keep the device turned on. Because it is a leakage current through an insulator, this current is independent of temperature, unlike I_{DSS}.

$R_{DS(on)}$ (drain-source on-state resistance) is one of the most important parameters. The previous parameters guarantee how the device functions when it is off, how it turns off and what leakage currents could be expected. These factors are important when battery capacity is an issue in the application.

$R_{DS(on)}$ is a measure of how good a closed-switch the MOSFET is, when turned-on. It is a key factor in determining the power loss and efficiency of a circuit containing a MOSFET. The on-resistance $R_{DS(on)} \times I_D^2$ gives the power dissipated in the MOSFET when it is turned **fully** on. Power MOSFETs are capable of carrying tens or hundreds of amps in the on-state.

Power dissipated in the MOSFET makes the die temperature rise above that of its mounting base. Also when the MOSFET die temperature increases, its $R_{DS(on)}$ increases proportionally. Maximum recommended junction temperature is 175 °C (for all NXP **packaged** MOSFETs).

Using the BUK7Y12-55B data sheet as an example:

$R_{th(j\text{-}mb)}$ temperature rise per Watt between junction (die) and mounting base = 1.42 K/W (1.42 °C/W).

Maximum power dissipation for temperature rise of 150 K (T_{mb} = 25 °C, T_j = 175 °C) = $150/1.42$ = 105.63 W.

Maximum $R_{DS(on)}$ at a die temperature (T_j) of 175 °C = 27.6 mΩ.

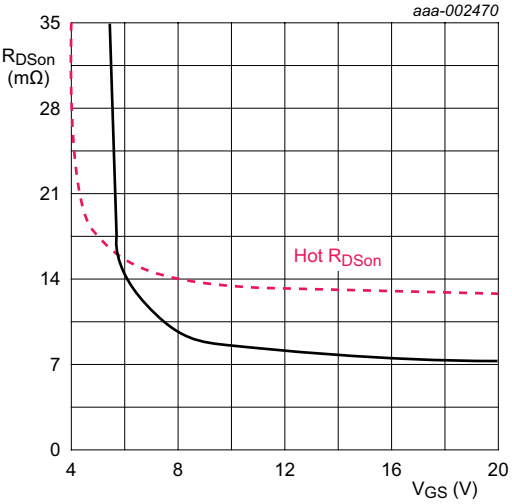
Therefore, at steady state with T_{mb} = 25 °C and T_j = 175 °C, P = 105.63 W $= I_{max}^2 \times R_{DS(on)(175\ ^oC)}$.

Therefore:

(5) $$I_{max} = \sqrt{\frac{P_{(max)175°C}}{R_{DS(on)175°C}}} = \sqrt{\frac{105.63W}{0.0276\Omega}}$$

= 61.86 A (rounded down to 61.8 A in the data sheet).

The $R_{DS(on)}$ of the MOSFET depends on gate-source voltage, and there is a lower value below which it rises very sharply. The ratio of the $R_{DS(on)}$ increase over temperature is different for different gate drives. The red dashed line in **Figure 7** shows the curve for a higher temperature and demonstrates the differences.

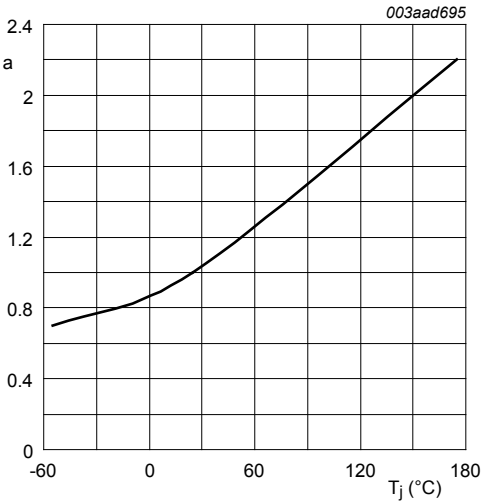


This diagram is for illustrative purposes only and not to be taken as an indication of hot R_{dson} performance for any device

Fig 7. Drain-source on-state resistance as a function of gate-source voltage at 25 °C and high temperature

If an application requires good $R_{DS(on)}$ performance for lower gate-source voltages, then MOSFETs are made with lower threshold voltages, e.g. the BUK9Y12-55B. However, the lower threshold voltage of such a device means that it has a lower headroom for its off-state at high temperature. This lower headroom often means that a device with a higher threshold voltage is needed.

A typical curve showing how resistance increases with temperature is shown in **Figure 8**.



$$a = \frac{R_{DS(on)}}{R_{DS(on)25\ °C}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature

1.2.6.2 Dynamic characteristics

The dynamic characteristics determine the switching performance of the device. Several of these parameters are highly dependent on the measurement conditions. Consequently, understand the dynamic characteristics before comparing data sheets from suppliers with different standard conditions. **Table 6** is a sample dynamic characteristics table.

Table 6. Dynamic characteristics

List of constants and limitations relating to the table i.e. voltages, currents and temperatures

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(tot)}$	total gate charge	I_D = 20 A; V_{DS} = 44 V; V_{GS} = 10 V	-	35.2	-	nC
Q_{GS}	gate source charge		-	9.24	-	nC
Q_{GD}	gate drain charge		-	14.8	-	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C	-	1550	2067	pF
C_{oss}	output capacitance		-	328	394	pF
C_{rss}	reverse transfer capacitance		-	153	210	pF
$T_{d(on)}$	turn-on delay time	V_{DS} = 30 V; V_{GS} = 10 V; R_L = 1.5 Ω; $R_{G(ext)}$ = 10 Ω	-	19.3	-	ns
T_r	rise time		-	29.4	-	ns
$T_{d(oFF)}$	turn-off delay time		-	43.2	-	ns
T_f	fall time		-	22	-	ns

1.2.6.2.1 Gate charge

$Q_{G(tot)}$, Q_{GS}, and Q_{GD} are all parameters from the same gate charge curve. They describe how much gate charge the MOSFET requires to switch, for certain conditions. This is particularly important in high frequency switching applications. Much of the power loss occurs during switching, when there are significant voltage and current changes simultaneously between the drain, gate and source. In the blocking state, there are significant voltages but negligible currents. In the full-on state, there are significant currents and small voltages.

The gate charge parameters are dependent on the threshold voltage and the switching dynamics as well as the load that is being switched. There is a difference between a resistive load and an inductive load.

An example of a gate charge curve is shown in **Figure 9**:

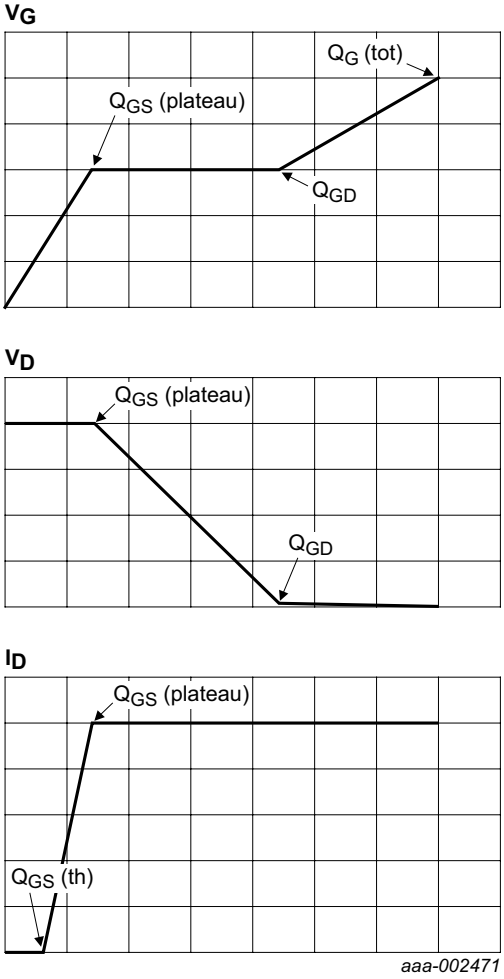


Fig 9. Gate charge curve also showing drain-source currents and voltages

Because the capacitance varies with voltage and current, it is better to look at the gate charge data than the capacitance data when determining switching performance. This is especially true if the gate-driver circuit for the MOSFET is limited to a particular current, and a rapid switch is required.

The gate charge curve describes what happens to a MOSFET which has a drain supply limited to a particular current and voltage. The operation of the test circuit means that during the gate charge curve, the MOSFET is provided with either a constant voltage or a constant current.

During this time, the drain-source voltage begins to fall because the increased charge on the MOSFET allows easier conduction. Consequently, although the gate-source voltage is constant, the drain-gate voltage is falling.

Eventually the capacitance stops increasing and any further increases in gate charge increase the gate-source voltage. This characteristic is sometimes referred to as the "Miller plateau" as it refers to the time during which the so-called Miller capacitance increases. The Miller plateau is also known as the gate-drain charge (Q_{GD}).

During this period, there are significant currents and voltages between the drain and source, so Q_{GD} is important when determining switching losses.

Once the end of the Miller plateau is reached, the gate-source voltage increases again, but with a larger capacitance than before Q_{GS} had been reached. The gradient of the gate charge curve is less above the Miller plateau.

The gate-charge parameters are highly dependent on the measurement conditions. Different suppliers often quote their gate-charge parameters for different conditions, demanding care when comparing gate charge parameters from different sources.

Higher currents lead to higher values of gate-source charge because the plateau voltage is also higher. Higher drain-source voltages, lead to higher values of gate-drain charge and total gate charge, as the plateau increases.

The drain-source currents and voltages during the gate charge switching period are shown in **Figure 10**

If the MOSFET starts in the off state (V_{GS} = 0 V), an increase in charge on the gate initially leads to an increase in the gate-source voltage. In this mode, a constant voltage (V_{DS}) is supplied between the source and drain.

When the gate-source voltage reaches the threshold voltage for the limiting current at that drain-source voltage, the capacitance of the MOSFET increases and the gate-voltage stays constant. This is known as the plateau voltage and the onset charge is referred to as Q_{GS}. The higher the current is, the higher the plateau voltage (see **Figure 10**).

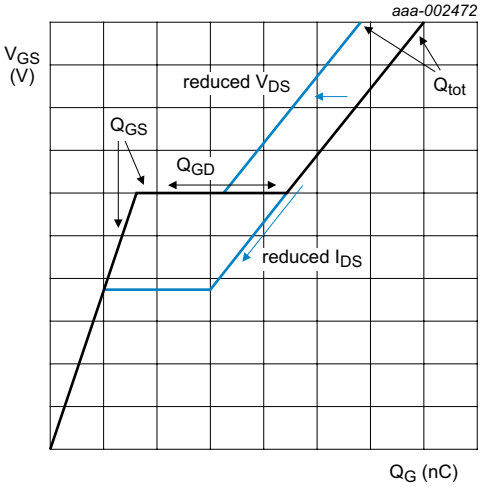


Fig 10. Features of gate charge curve

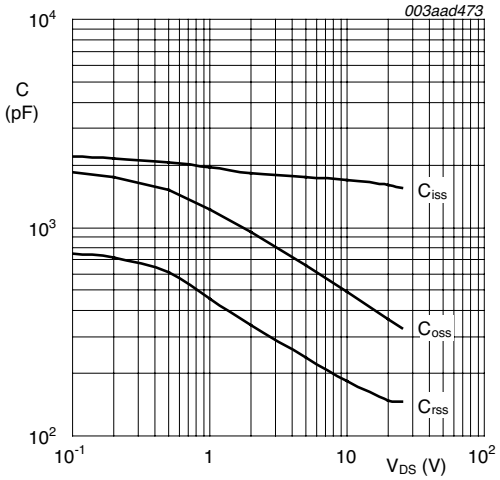
1.2.6.2.2 Capacitances

Capacitance characteristics are generally less useful than the gate charge parameters, for the reasons already discussed. However, they are still listed on data sheets. The three capacitances that are normally listed are as follows:

- **C_{ISS}** (input capacitance) is the capacitance between the gate and the other two terminals (source and drain).
- **C_{OSS}** (output capacitance) is the capacitance between the drain and the other two terminals (gate and source).
- **C_{RSS}** (reverse transfer capacitance) is the capacitance between the drain and the gate.

Semiconductor capacitances generally depend on both voltage and the frequency of the capacitance measurement. Although it is difficult to compare capacitances measured under different conditions, many suppliers specify a measurement frequency of 1 MHz. Consequently, the capacitances vary with drain-source voltage (see **Figure 11**). However, the capacitances also vary with gate-source voltage, which is why the gradients in the gate-charge curve vary for different voltages (see **Figure 9**).

The relationship between charge, voltage and capacitance in the gate charge curve is $\Delta Q = \Delta C \times \Delta V$. For different gradients at different gate voltages, the capacitance changes significantly with gate-source voltage.



V_{GS} = 0 V; f = 1 MHz

Fig 11. Capacitances as a function of drain source voltage

1.2.6.2.3 Switching times

Most manufacturers quote resistive load switching times. However, extreme care is needed when comparing data from different manufacturers, as they are highly dependent on the resistance of the gate drive circuit used for the test. In devices for fast switching applications, the gate resistance of the MOSFET is often quoted as capacitive time constants which are equally dependent on resistance and capacitance.

1.2.6.3 Diode characteristics

The diode characteristics are important if the MOSFET is being used in the so-called “third quadrant”. The third quadrant is a typical arrangement where the MOSFET replaces a diode to reduce the voltage drop from the inherent diode forward voltage drop. In such a situation, there is always a small time period when the MOSFET parasitic diode is conducting before the MOSFET turns on. For such applications, the diode switching parameters are important. In addition, diode reverse recovery contributes to the power losses as well as oscillation, which can cause EMC concern.

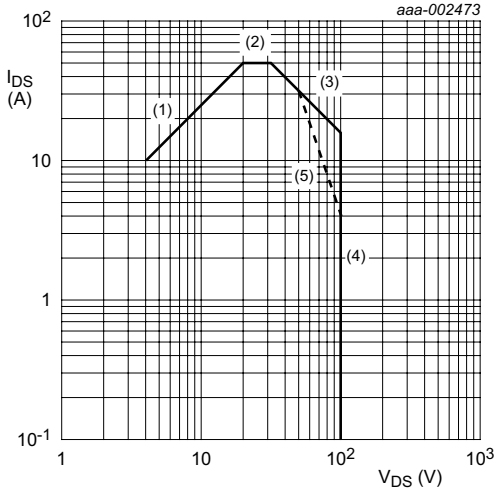
1.2.7 Package outline

This section describes the package outline dimensions and tolerances.

1.3. Appendices

1.3.1 Safe Operating Area (SOA) curves

To highlight the key features, **Figure 12** provides an idealized SOA curve for a hypothetical MOSFET. Data for a hypothetical MOSFET for a single pulse length, is shown to highlight the region where it deviates from the ideal curve.



(1) $R_{DS(on)}$ limit (V_{DS}/I_{DS} is constant)

(2) Maximum pulsed drain current (I_{DS} is constant)

(3) Maximum pulsed power dissipation ($V_{DS} \times I_{DS}$ is constant)

(4) Maximum allowed voltage (V_{DS} is constant)

(5) Linear mode derating - a departure from the ideal behavior shown in (3) due to operation within a regime of positive feedback, and potential thermal runaway

Fig 12. Idealized SOA curve at a single time pulse for hypothetical MOSFET

The dashed line (5) is to emphasize where the curve deviates from the ideal. In reality, there is a single curve with a change of gradient where the linear mode derating becomes important.

$R_{DS(on)}$ limit

$R_{DS(on)}$ is region (1) of the graph and **Equation 6** represents the limiting line:

$$(6)\quad \frac{V_{DS}}{I_{DS}} \leq R_{DS(on)}\ (175\ ^{\circ}C)$$

The limit is when the MOSFET is fully on and acting as a closed switch with a resistance that is no greater than the hot $R_{DS(on)}$.

Constant current region

The constant current region is region (2) of the graph. It is the maximum pulsed drain current, which is limited by the device manufacturer (for example, the wire-bonds within the package).

Maximum power dissipation (linear mode) limit

In this region, the MOSFET is acting as a (gate) voltage-controlled current source. This means that there are significant voltages and currents applied simultaneously, leading to significant power dissipation. Line (3) shows the idealized curve, whereas the dotted line (5) shows where it deviates from the ideal.

The limiting factor for the SOA curve in region (5), is the heating applied during a rectangular current and voltage pulse. Even in the ideal situation, this curve depends on the transient thermal impedance of the MOSFET, which is covered in **Section 1.2.5**.

The transient thermal impedance varies with the pulse length. This is due to the different materials in the MOSFET having different thermal resistances and capacities. The differences create a thermal equivalent to an RC network from the junction (where the heat is generated) to the mounting base. **Equation 7** is the calculation used to determine the ideal curve in this region.

$$(7)\quad P = I_D \times V_{DS} = \frac{T_{j(max))} - T_{mb}}{Z_{th(j\text{-}mb)}} = Constant$$

The ideal situation accurately describes the situation for sufficiently high current densities. However, it is overly optimistic for low current-densities, i.e. towards the bottom right of region (3). Low current densities and high voltages can lead to thermal runaway in the linear mode operation. Thermal runaway is discussed in the following section.

Thermal runaway in linear mode

Power MOSFETs are often considered to be immune to thermal runaway due to the temperature coefficient of resistance, which means that as temperature rises, current falls.

This is only true for MOSFETs that are fully on (i.e. in region 1), but it is not the whole story.

When a MOSFET is turned on, there are two competing effects that determine how its current behaves with increasing temperature. As the temperature rises, the threshold voltage falls. The MOSFET is effectively turned on more strongly, thereby increasing the current. In opposition, the resistance of the silicon increases with increasing temperature, thereby reducing the current. The resultant effect for a constant drain-source voltage, is shown in **Figure 13**. This situation occurs when the gate-source voltage of a MOSFET is being used to control the current, or when the MOSFET is switched sufficiently slowly.

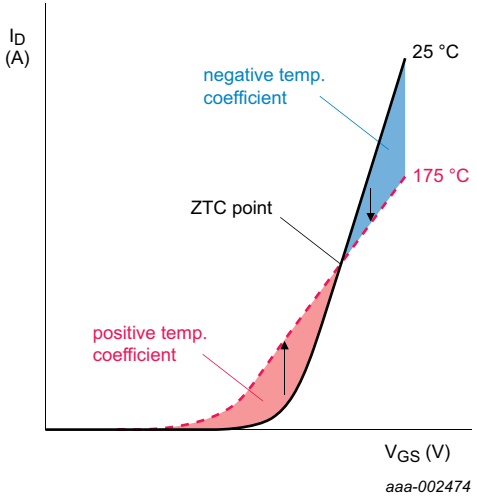


Fig 13. Transfer characteristics for a hypothetical MOSFET, showing regions of positive and negative temperature coefficient

The resistance increase dominates at high currents, meaning that localized heating leads to lower currents. The threshold-voltage drop dominates at low currents, meaning that localized heating lowers the threshold voltage. This condition effectively turns on the device more, leading to higher currents and a risk of thermal runaway.

Consequently, for a given V_{DS}, there is a critical current below which there is a positive-feedback regime and a subsequent risk of thermal runaway. Above this critical current, there is negative feedback and thermal stability. This critical current is known as the Zero Temperature Coefficient (ZTC) point.

This effect reduces the SOA performance for low currents and high drain-source voltages. The constant power line must be reduced as shown in region (5). For short switching events, this effect is insignificant. However, as the duration of the switching event becomes longer, for example to reduce electromagnetic interference, the effect becomes more important and potentially hazardous.

Voltage-limited region

The device is limited by its breakdown voltage V_{DS} which is shown in region (4). The quick reference data provides values for V_{DS} at temperatures of 25 °C and above. In the hypothetical MOSFET shown in **Figure 13**, the rating is 100 V. For the BUK7Y12-55B, the voltage is 55 V.

1.3.1.1 Safe operating area for temperatures above 25 °C

When taking measurements from the SOA curve there are two main assumptions:

1. Operation temperature of 25 °C

2. It is a rectangular pulse

However, some pulses are not rectangular and do not occur at 25 °C. For these instances, the use of **Equation 8** can be used.

$$(8)\quad T_{j(rise)\max} = T_{j(max)} - T_{j(amb)} = \frac{2}{3} P_{av} \cdot Z_{th\left(\frac{t_{av}}{2}\right)}$$

Where $T_{j(max)}$ is the maximum die temperature of 175 °C and $T_{j(amb)}$ is the ambient temperature of the system. For example, in automotive applications, the two main ambient temperatures used are 85 °C for in-cabin (inside the driver compartment) and 105 °C for under the hood (near and around the engine).

It is worth noting that using the ambient temperature in calculations for worst case analysis, can be misleading. It is misleading because the temperature of the MOSFET mounting base before it is switched on can be higher. For example, a design has 10 MOSFETs and 9 are powered. The mounting base temperature of the 10th MOSFET (which is off) is likely to be similar to that of the other 9 MOSFETs that are ON. So if the ambient is 105 °C, and the mounting base temperature of the 9 MOSFETs that are ON is 125 °C, $T_{j(amb)}$ of the 10th MOSFET is 125 °C and not 105 °C. Calculations under these conditions are conservative and are more suitable for worst case analysis (**Equation 9**).

(9) $$T_{j(rise)\max} = T_{j(max)} - T_{j(amb)} = P_{av} \cdot Z_{th(t_{av})}$$

Note: Use $R_{th(j\text{-}mb)}$ instead of $Z_{th(j\text{-}mb)}$ in a DC application (not pulsed). Above approximately 100 ms, Z_{th} is indistinguishable from R_{th}.

1.3.1.1.1 Example calculations

Calculate the max DC I_{DS} for a BUK9277-55A, with V_{DS} = 40 V at 25 °C

Rewrite **Equation 10** to bring out I_{DS} as the main subject (P_{av} is the average power, and is $I_{DS} \times V_{DS}$ for the DC situation). As it is a DC situation, replace Z_{th} with R_{th}.

(10) $$T_{j(rise)} = I_{DS} \times V_{DS} \times Z_{th(av)}$$

(11) $$\frac{T_{j(rise)}}{V_{DS} \times R_{th}} = I_{DS}$$

(12) $$\frac{175\ °C - 25\ °C}{40\ \text{V} \times 2.93\ K/W} = 1.28\ \text{A}$$

Therefore, the maximum DC current rating for these conditions is 1.28 A.

1.3.1.2 Example using the SOA curve and thermal characteristics

Consider the following application during linear mode operation:

- Device BUK7Y12-55B, square current pulses of the following:
  - I_{pulse} = 20 A
  - V_{pulse} = 40 V
  - f = 2 kHz
  - t_{pulse} = 100 µs
  - T_{amb} = 25 °C

1.3.1.2.1 Calculation steps

The SOA curve is initially checked to see whether any single pulse would cause a problem. Observing the SOA curve, it can be seen that the 20 A, 40 V pulse lies between the 100 µs and 1 ms lines. This indicates that the pulse lies within acceptable limits.

The duty cycle for the pulses is now calculated using a frequency of 2 kHz for 100 µs pulses. These values give a duty cycle of 0.2. The SOA curve demonstrates that for 100 µs, the line with the duty cycle (δ) has a transient thermal impedance of 0.4 K/W.

The power dissipation for the square pulse is 20 A × 40 V, which equals 800 W.

Using **Equation 8**, the temperature rise for the 100 µs pulse is calculated as being 800 W × 0.4 K/W, which equals 320 K. With a starting temperature of 25 °C, the temperature rise results in a finishing temperature of 345 °C. As the MOSFET junction temperature must not exceed 175 °C, the MOSFET is not suitable for this application.

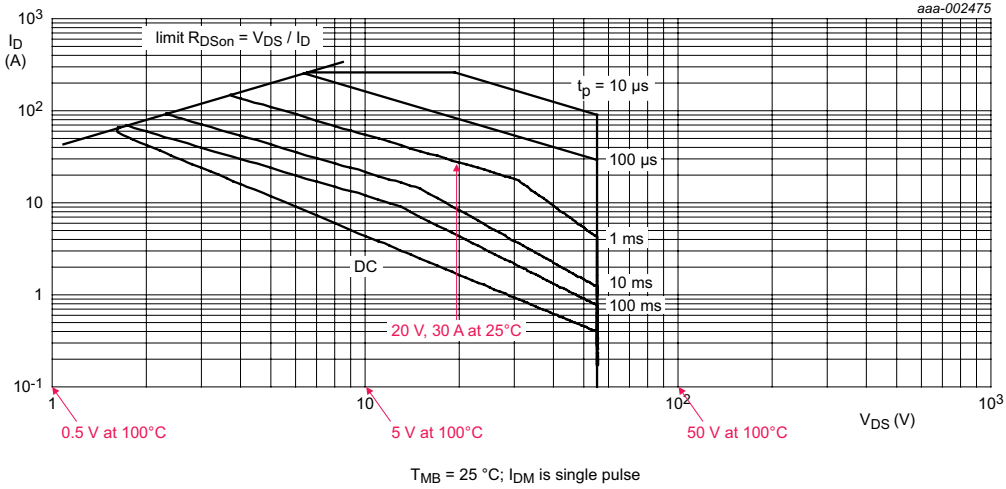
If the application requires a single pulse, then the curve shows that the transient thermal impedance for a 100 µs pulse is 0.1 K/W. As a result, the temperature rise is 800 W × 0.1 K/W which equals 80 K. The finishing temperature is then 105 °C for a starting temperature of 25 °C. The device is able to withstand this, thereby confirming what the SOA curve already indicated.

1.3.1.2.2 Derating for higher starting temperatures

The example Safe Operating Area calculations were performed for a mounting base temperature of 25 °C. At higher mounting base temperatures, the SOA curves must be derated, as the allowed temperature rise is reduced. The allowed power of the pulse is reduced proportionally to the reduced temperature rise. For example, with a mounting base temperature of 25 °C, the allowed temperature rise is 150 °C. At 100 °C, the allowed temperature rise is half of that (75 °C). The allowed power is half of that allowed at 25 °C.

Because of the effects of linear-mode operation, the current is maintained but the allowed drain-source voltage is derated.

The 100 °C derating for the BUK7Y12-55B is shown in **Figure 14**.



T_{MB} = 25 °C; I_{DM} is single pulse

Fig 14. SOA curve showing derating for 100 °C

Example:

Is a 1 ms pulse of 30 A and 15 V allowed at 100 °C for the BUK7Y12-55B?

At 25 °C, it can be seen that a V_{DS} of 20 V is allowed for 30 A, and 1 ms. Therefore, at 100 °C, a V_{DS} of 10 V is allowed.

A 1 ms pulse of 30 A and 15 V at 100 °C is outside the permitted safe operating area and is consequently not allowed.

1.4. References

[1] The Impact of Trench Depth on the Reliability of Repetitively Avalanched Low-Voltage Discrete Power Trench nMOSFETs - Alatise et al, IEE Electron Device Letters, Volume 31, No7, July 2010, pages 713-715.

[2] Semiconductor Devices - Physics and Technology S.M.Sze, 1985, John Wiley & Sons.

[3] Application Note AN10273 (Chapter 2 of this book) - Power MOSFET single-shot and repetitive avalanche ruggedness rating.

[4] Application Note AN10874 (Chapter 4 of this book) - LFPAK MOSFET thermal design guide.

Chapter 2: Power MOSFET single-shot and repetitive avalanche ruggedness rating

Chapter 2: Power MOSFET single-shot and repetitive avalanche ruggedness rating

2.1 Introduction

Electronic applications have progressed significantly in recent years and have inevitably increased the demand for an intrinsically rugged power MOSFET. Device ruggedness defines the capacity of a device to sustain an avalanche current during an unclamped inductive load switching event. The avalanche ruggedness performance of a power MOSFET is normally measured as a single-shot Unclamped Inductive Switching (UIS) avalanche energy or $E_{DS(AL)S}$. It provides an easy and quick method of quantifying the robustness of a MOSFET in avalanche mode. However, it does not necessarily reflect the true device avalanche capability (see **Ref. 1**, **Ref. 2** and **Ref. 3**) in an application.

This chapter explains the fundamentals of UIS operation. It reviews the appropriate method of quantifying the safe operating condition for a power MOSFET, subjected to UIS operating condition. The chapter also covers the discussions on repetitive avalanche ruggedness capability and how this operation can be quantified to operate safely.

2.2 Single-shot and repetitive avalanche definitions

Single-shot avalanche events are avalanche events that occur due to a fault condition in the application such as electrical overstress. The application does not have an avalanche designed into its operation.

However, repetitive avalanche refers to the applications where avalanche is an intended operation mode of the MOSFET. Here, avalanche is a designed function and is independent of the number of avalanche events.

Any customer wishing to operate outside the current avalanche ratings may be considered on an application basis. Contact your local sales team for more information.

2.3 Understanding power MOSFET single-shot avalanche events

The researchers and the industry have established single-shot avalanche capability of a device (see **Ref. 1**, **Ref. 2** and **Ref. 3**). The test is carried out on a simple unclamped inductive load switching circuit, as shown in **Figure 1**.

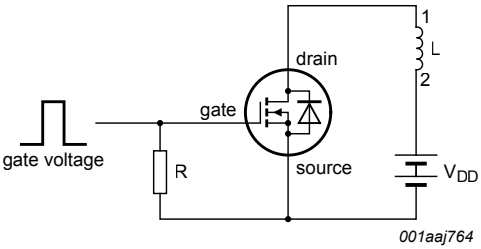


Fig 1. Unclamped inductive load test circuit for MOSFET ruggedness evaluation

2.3.1 Single-shot UIS operation

A voltage pulse is applied to the gate to turn on the MOSFET, as shown in **Figure 2**. It allows the load current to ramp up according to the inductor value (L) and the drain supply voltage (V_{DD}). The phenomenon is shown in **Figure 3** and **Figure 4**. At the end of the gate pulse, the MOSFET is turned off. The current in the inductor continues to flow, causing the voltage across the MOSFET to rise sharply. This overvoltage is clamped at breakdown voltage (V_{BR}) until the load current reaches zero, as illustrated in **Figure 3**. Typically, V_{BR} is:

$$V_{BR} \approx 1.3 \times V_{(BR)DSS} \quad (1)$$

The peak load current passing through the MOSFET before turn off is the non-repetitive drain-source avalanche current ($I_{DS(AL)S}$) of the UIS event. $I_{DS(AL)S}$ is illustrated in **Figure 4**. The following expression is used to determine the rate at which the avalanche current decays, which is dependent on the inductor value:

$$\frac{dI_{DS(AL)S}}{dt_{AL}} = -\frac{V_{BR} - V_{DD}}{L} \quad (2)$$

The peak drain-source avalanche power ($P_{DS(AL)M}$) dissipated in the MOSFET is shown in **Figure 5**. It is a product of the breakdown voltage (V_{BR}) and the non-repetitive drain-source avalanche current ($I_{DS(AL)S}$); see **Figure 3** and **Figure 4**. The avalanche energy dissipated is the area under the P_{AV} waveform and is estimated from the following expression:

$$(3)\quad E_{DS(AL)S} = \frac{P_{DS(AL)M} \times t_{AL}}{2}$$

or

$$(4)\quad E_{DS(AL)S} = \frac{1}{2} \cdot \frac{V_{BR}}{V_{BR} - V_{DD}} \cdot LI^2_{DS(AL)S}$$

Another crucial parameter involved in a MOSFET avalanche event is the junction temperature. After the avalanche event (τ) has begun, the following expression is used to determine the transient junction temperature variation during device avalanche at a given time:

$$(5)\quad \Delta T_j(\tau) = \int_0^{\tau} P_{AV}(t) \frac{dZ_{th(\tau - t)}}{dt} dt$$

where Z_{th} is the power MOSFET transient thermal impedance. Alternatively, the following expression approximates the maximum ΔT_j:

$$(6)\quad \Delta T_{j(max)} \approx \frac{2}{3} P_{DS(AL)M} Z_{th(t_{AL}/2)}$$

Assuming that $T_{j(max)}$ occurs at $t_{AL}/2$, $Z_{th(t_{AL}/2)}$ the transient thermal impedance measured at half the avalanche period t_{AL}.

Therefore, the maximum junction temperature resulting from the avalanche event is:

$$(7)\quad T_{j(max)} \approx \Delta T_{j(max)} + T_j$$

where T_j refers to the junction temperature prior to turn off.

2.3.1.1 Single-shot UIS waveforms

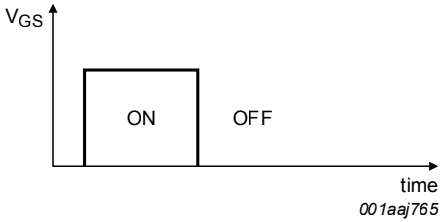


Fig 2. Gate-source voltage, V_{GS}

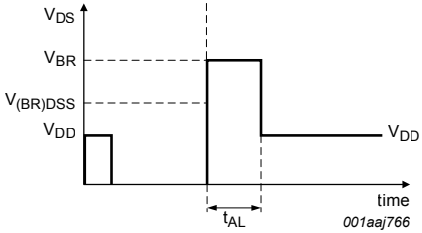


Fig 3. Drain-source voltage, V_{DS}

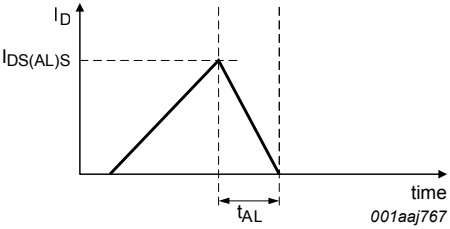


Fig 4. Drain current, I_D

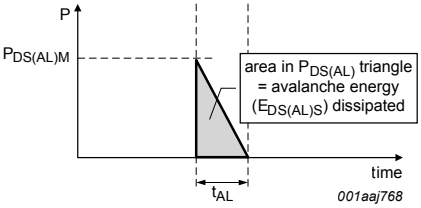


Fig 5. Peak drain-source avalanche power, $P_{DS(AL)M}$

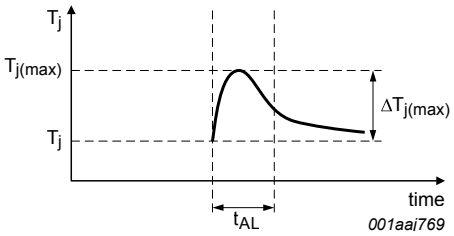


Fig 6. Transient junction temperature profile of MOSFET during an avalanche event

2.3.2 Single-shot avalanche ruggedness rating

The failure mechanism for a single-shot avalanche event in a power MOSFET is due to the junction temperature exceeding the maximum temperature rating. In such a case, catastrophic damage occurs to the MOSFET. If the transient temperature resulting from an avalanche event, as shown in **Figure 6**, rises beyond a recommended rated value, the device risks being degraded. The recommended rated value is derated from the maximum temperature for optimum reliability.

Blackburn (see **Ref. 2**) has discussed a general guideline in detail, on the appropriate method of quantifying the single-shot avalanche capability of a device. It takes the avalanche current and initial junction temperature into consideration. The maximum allowed avalanche current as a function of avalanche time defines the safe operation for a device single-shot UIS event. The maximum allowed avalanche current is set so that a safe maximum junction temperature, $T_{j(max)}$ of 175 °C, is never exceeded. Using **Equation 7**, **Figure 7** is plotted.

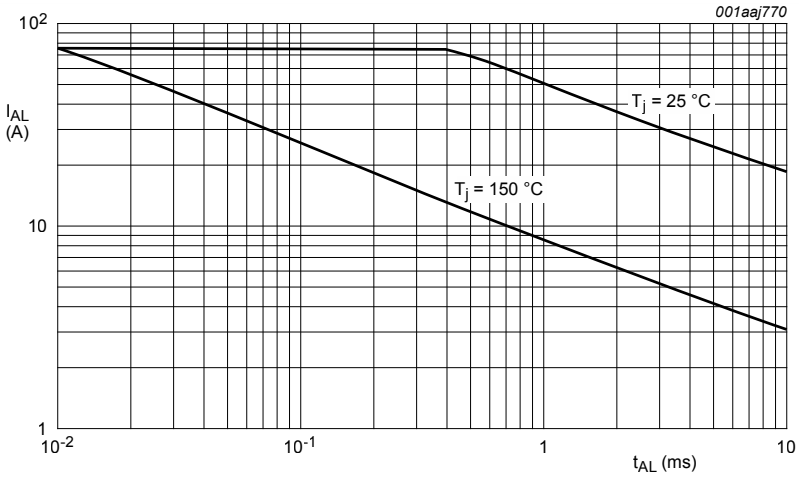


Fig 7. Single-shot avalanche ruggedness Safe Operating ARea (SOAR) curves of BUK764R0-55B limited to a $T_{j(max)}$ of 175 °C

Figure 7 shows the SOAR curves of a device single-shot avalanche capability. The 25 °C junction temperature curve shows the maximum allowable $I_{DS(AL)S}$ for a given t_{AL} at an initial T_j of 25 °C. This maximum I_{AL} results to a maximum allowable junction temperature $T_{j(max)}$ of 175 °C, which means a $\Delta T_{j(max)}$ of 150 °C.

The area under the SOAR curve is the Safe Operating ARea (SOAR). Similarly, the 150 °C junction temperature curve is the maximum operating limit for an initial T_j of 150 °C. The maximum value of $I_{DS(AL)S}$ induces a $\Delta T_{j(max)}$ of 25 °C, resulting in a $T_{j(max)}$ of 175 °C. Again the area under the curve is the SOAR.

The maximum junction temperature resulting in catastrophic device avalanche failure is approximately 380 °C, which is in excess of the rated $T_{j(max)}$ of 175 °C. However, operating beyond the rated $T_{j(max)}$ may induce long-term detrimental effects to the power MOSFET and is not recommended.

2.4 Understanding power MOSFET repetitive avalanche events

Repetitive avalanche refers to an operation involving repeated single-shot avalanche events, as discussed earlier. Until recently, most manufacturers have avoided the issues pertaining to the power MOSFET repetitive avalanche capability. It is primarily due to the complexity in such operations and the difficulties in identifying the underlying physical degradation process in the device.

Due to the traumatic nature of the avalanche event, a repetitive avalanche operation can be hazardous for a MOSFET. It is hazardous even when the individual avalanche events are below the single-shot UIS rating. This type of operation involves additional parameters such as frequency, duty cycle, and thermal resistances ($R_{th(j-a)}$ and $R_{th(j-mb)}$) of the system during the avalanche event. However, it is possible to derate the single-shot rating to define a repetitive avalanche SOAR.

2.4.1 Repetitive UIS operation

The repetitive UIS test circuit is shown in **Figure 1**. The gate is fed with a train of voltage pulses at a frequency (f) and for a duty cycle as shown in **Figure 8**. The resulting breakdown voltage (V_{BR}) and drain current (I_D) passing through the load are the same as for a single-shot UIS. However, the peak I_D is now denoted as repetitive drain-source avalanche current ($I_{DS(AL)R}$), as shown in **Figure 9**.

The repetitive drain-source avalanche power ($P_{DS(AL)R}$) resulting from the repetitive UIS operation is shown in **Figure 10.** For finding the value of $P_{DS(AL)R}$, it is necessary to first calculate $E_{DS(AL)S}$ for a single avalanche event using **Equation 3**. This resultant value of $E_{DS(AL)S}$ is substituted in the following expression, to calculate the value of $P_{DS(AL)R}$:

(8) $$P_{DS(AL)R} = E_{DS(AL)S} \times f$$

2.4.1.1 Repetitive UIS waveforms

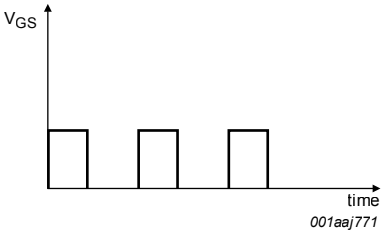


Fig 8. Gate pulse, V_{GS}

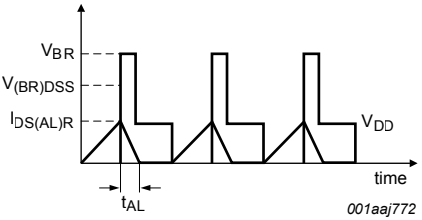


Fig 9. Drain-source voltage, V_{DS} and repetitive drain-source avalanche current, $I_{DS(AL)R}$

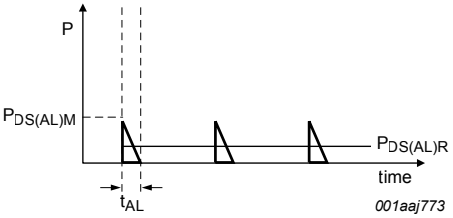


Fig 10. Repetitive drain-source avalanche power, $P_{DS(AL)R}$

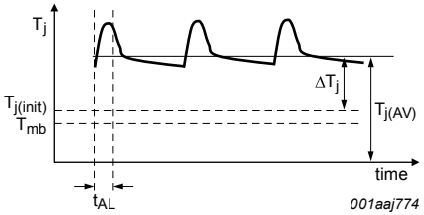


Fig 11. Transient junction temperature components of MOSFET during repetitive avalanche

2.4.2 Temperature components

The temperature rise from the repetitive avalanche mode in the power MOSFET is shown in **Figure 11**.

The temperature ($T_{j(init)}$) comprises the mounting base temperature (T_{mb}) and the temperature rise resulting from any on-state temperature difference (ΔT_{on}).

$$T_{j(init)} = T_{mb} + \Delta T_{on} \quad (9)$$

In addition, there is a steady-state average junction temperature variation (ΔT_j) resulting from the average repetitive avalanche power loss.

$$\Delta T_j = P_{DS(AL)R} \times R_{th(j\text{-}a)} \quad (10)$$

where $R_{th(j-a)}$ is the thermal resistance from junction to ambient of the device in the application. The summation of **Equation 9** and **Equation 10** gives the average junction temperature, $T_{j(AV)}$ of a power MOSFET in repetitive UIS operation.

$$T_{j(AV)} = T_{j(init)} + \Delta T_j \quad (11)$$

2.5 Repetitive avalanche ruggedness rating

Following extensive investigation, it is clear that there is more than one failure or wear-out mechanism involved in repetitive avalanche. Temperature is **not** the only limiting factor to a repetitive avalanche operation. However, by limiting temperature and the repetitive drain-source avalanche current ($I_{DS(AL)R}$), an operating environment is defined such that the avalanche conditions do not activate device degradation. It allows the power MOSFET to operate under repetitive UIS conditions safely.

Figure 12 shows the single-shot and repetitive avalanche SOAR curves of BUK764R0-55B, where 'Rep. Ava' represents the 'repetitive avalanche SOAR curve'.

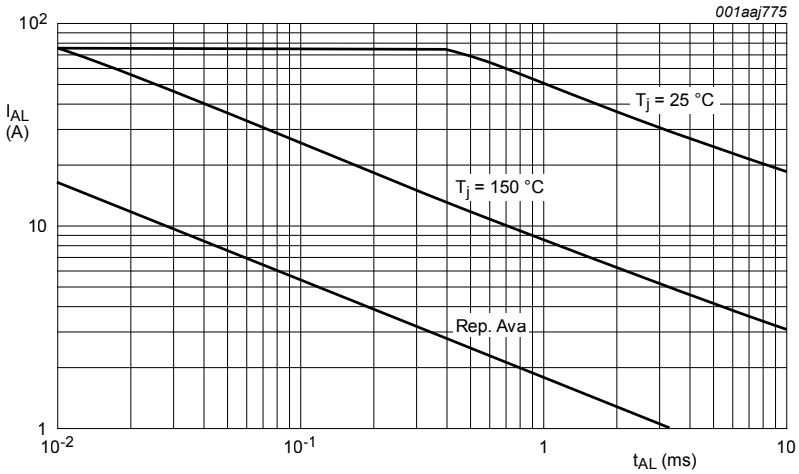


Fig 12. Single-shot and repetitive avalanche SOAR curves of BUK764R0-55B limited to $T_{j(max)}$ of 175 °C and $T_{j(AV)}$ of 170 °C, respectively

The two conditions which must be satisfied for safe operation of a power MOSFET under repetitive avalanche mode are:

1. $I_{DS(AL)R}$ should **not** exceed the repetitive avalanche SOAR curve
2. $T_{j(AV)}$ should **not** exceed 170 °C

2.6 Conclusion

Power MOSFETs can sustain single-shot and repetitive avalanche events. Simple design rules and SOAR regions are provided.

2.7 Examples

The following examples examine cases of avalanche operation acceptance:

2.7.1 Single-shot avalanche case

- Device: BUK764R0-55B; see **Figure 12**
- L = 2 mH
- $I_{DS(AL)S}$ = 40 A
- $R_{th(j-a)}$ = 5 K/W
- $V_{(BR)DSS}$ = 55 V
- V_{DD} = 0 V

2.7.1.1 Calculation steps

1. Using the above information, t_{AL} can be determined using **Equation 2**, which in this case is 1.11 ms. Transferring the I_{AL} and t_{AL} conditions onto **Figure 12**, the operating point is in between the T_j = 25 °C and T_j = 150 °C SOAR curves. It suggests that the operating condition may be feasible.
2. To check, calculate the $\Delta T_{j(max)}$ using **Equation 6**, where $Z_{th(556\ \mu s)}$ in the data sheet is approximately 0.065 K/W. It gives a $\Delta T_{j(max)}$ of 124.8 °C.

Based on the above calculations, the operating condition is acceptable if the device T_j < 50 °C.

2.7.2 Repetitive avalanche case

- Device: BUK764R0-55B; see **Figure 12**
- L = 0.5 mH
- $I_{DS(AL)R}$ = 6 A
- f = 3 kHz
- $R_{th(j-a)}$ = 5 K/W
- T_o = 100 °C
- $V_{(BR)DSS}$ = 55 V
- V_{DD} = 0 V

2.7.2.1 Calculation steps

1. From the above information, t_{AL} can be determined using **Equation 2**, which in this case is approximately 0.042 ms. Transferring the I_{AL} and t_{AL} conditions onto **Figure 12**, the operating point is under the boundary of the 'Rep. Ava' SOAR curve. It suggests that the operating condition is acceptable. Therefore, condition 1 is satisfied.
2. Calculate the non-repetitive drain-source avalanche energy ($E_{DS(AL)S}$) using **Equation 3** ($E_{DS(AL)S}$ = 9 mJ).
3. Calculate the repetitive drain-source avalanche power ($P_{DS(AL)R}$) using **Equation 8** ($P_{DS(AL)R}$ = 27 W).
4. Calculate the average ΔT_j rise from repetitive avalanche (ΔT_j) using **Equation 10** (ΔT_j = 135 °C).
5. Determine the average junction maximum temperature in repetitive avalanche operation ($T_{j(AV)}$) using **Equation 11** ($T_{j(AV)}$ = 235 °C). Therefore, condition 2 is not satisfied.

Based on the above calculations, the operating conditions meet the first requirement but not the second requirement for safe repetitive avalanche operation. It is because the maximum $T_{j(AV)}$ exceeded 170 °C.

To make the above operation viable, the design engineer has to satisfy the second condition by reducing $T_{j(AV)}$. It can be achieved by improving the heat sinking of the device. Reducing $R_{th(j-a)}$ from 5 K/W to 2.5 K/W gives a $T_{j(AV)}$ of 167.5 °C, satisfying condition 2 for safe repetitive avalanche operation.

2.8 References

[1] **Turn-Off Failure of Power MOSFETs** - D.L. Blackburn, Proc. 1985 IEEE Power Electronics Specialists Conference, pages 429 to 435, June 1985.

[2] **Power MOSFET failure revisited** - D.L. Blackburn, Proc. 1988 IEEE Power Electronics Specialists Conference, pages 681 to 688, April 1988.

[3] **Boundary of power-MOSFET, unclamped inductive-switching (UIS), avalanche-current capability** - Rodney R. Stoltenburg, Proc. 1989 Applied Power Electronics Conference, pages 359 to 364, March 1989.

Chapter 3: Using RC Thermal models

Chapter 3: Using RC Thermal models

3.1 Introduction

Networks of resistors and capacitors can be used to create a Foster RC thermal model. The model represents the thermal performance of a MOSFET within a SPICE environment. This chapter provides some basic theory behind the principle, and how to implement Foster RC thermal models. For convenience, Foster RC thermal models are referred to as RC models in the rest of this chapter. Here we describe several methods of using RC thermal models, including worked examples.

3.2 Thermal impedance

RC models are derived from the thermal impedance (Z_{th}) of a device (see **Figure 1**). This figure represents the thermal behavior of a device under transient power pulses. The Z_{th} can be generated by measuring the power losses as a result of applying a step function of varying time periods.

A device subjected to a power pulse of duration > ~ 1 s i.e. steady-state, has reached thermal equilibrium and the Z_{th} plateaus becomes the R_{th}. The Z_{th} illustrates the fact that materials have thermal inertia. Thermal inertia means that temperature does not change instantaneously. As a result, the device can handle greater power for shorter duration pulses.

The Z_{th} curves for repetitive pulses with different duty cycles, are also shown in **Figure 1**. These curves represent the additional RMS temperature rise due to the dissipation of RMS power.

To assist this discussion, the thermal resistance junction to mounting base ($R_{th(j\text{-}mb)}$) from the BUK7Y7R6-40E data sheet, has been included in **Table 1**. The Z_{th} in **Figure 1** also belongs to the BUK7Y7R6-40E data sheet.

Table 1. Steady state thermal impedance of BUK7YR6-40E

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see **Figure 1**	-	-	1.58	K/W

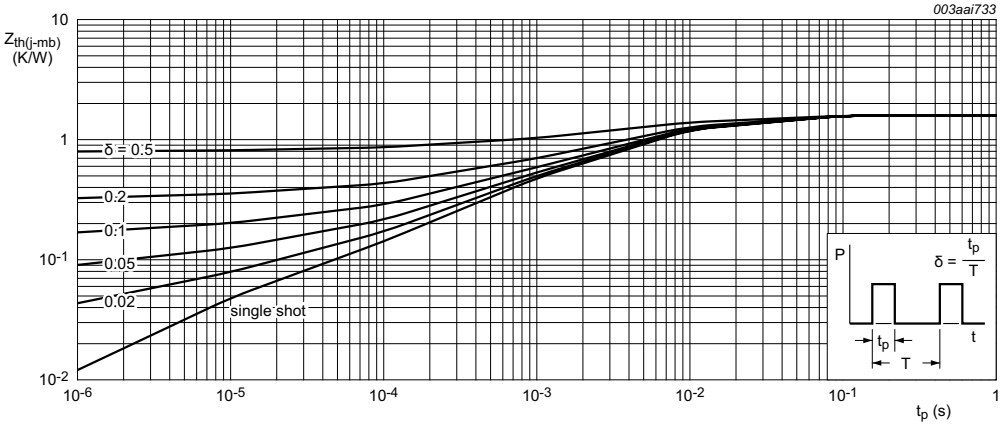


Fig 1. Transient thermal impedance from junction to mounting base as a function of pulse duration for the BUK7Y7R6-40E

3.3 Calculating junction temperature rise

To calculate the temperature rise within the junction of a power MOSFET, the power and duration of the pulse delivered to the device must be known. If the power pulse is a square, then the thermal impedance can be read from the Z_{th} chart. The product of this value with the power gives the temperature rise within the junction.

If constant power is applied to the device, the steady state thermal impedance can be used i.e. R_{th}. Again the temperature rise is the product of the power and the R_{th}.

For a transient pulse e.g. sinusoidal or pulsed, the temperature rise within the MOSFET junction becomes more difficult to calculate.

The mathematically correct way to calculate T_j is to apply the convolution integral. The calculation expresses both the power pulse and the Z_{th} curve as functions of time, and use the convolution integral to produce a temperature profile (see **Ref. 2**).

$$(1)\quad T_{j(rise)} = \int_0^{\tau} P_{(t)} \cdot \frac{d}{dt} Z_{th}(\tau - t)\, dt$$

However, this is difficult as the $Z_{th(\tau-t)}$ is not defined mathematically.

An alternative way is to approximate the waveforms into a series of rectangular pulse and apply superposition (see **Ref. 1**).

While relatively simple, applying superposition has its disadvantages. The more complex the waveform, the more superpositions that must be imposed to model the waveform accurately.

To represent Z_{th} as a function of time, draw upon the thermal electrical analogy and represent it as a series of RC charging equations or as an RC ladder. Z_{th} can then be represented in a SPICE environment for ease of calculation of the junction temperature.

3.4 Association between Thermal and Electrical parameters

The thermal electrical analogy is summarized in **Table 2**. If the thermal resistance and capacitance of a semiconductor device is known, electrical resistances and capacitances can represent them respectively. Using current as power, and voltage as the temperature difference, any thermal network can be handled as an electrical network.

Table 2. Fundamental parameters

Type	Resistance	Potential	Energy	Capacitance
Electrical (R = V/I)	R = resistance (Ohms)	V = PD (Volts)	I = current (Amps)	C = capacitance (Farads)
Thermal (R_{th}= K/W)	R_{th} = thermal resistance (K/W)	K = temperature difference (Kelvin)	W = dissipated power (Watts)	C_{th} = thermal capacitance (thermal mass)

3.5 Foster RC thermal models

The RC thermal models discussed are Foster Models. These models are derived by semi-empirically fitting a curve to the Z_{th}, the result of which is a one-dimensional RC network (**Figure 2**). The R and C values in a Foster model do not correspond to geometrical locations on the physical device. Therefore, these values cannot be calculated from device material constants as can be in other modeling techniques. Finally, a Foster RC model cannot be divided or interconnected through, i.e. have the RC network of a heat sink connected.

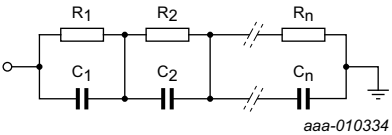


Fig 2. Foster RC thermal models

Foster RC models have the benefit of ease of expression of the thermal impedance Z_{th} as described at the end of **Section 3.2**. For example, by measuring the heating or cooling curve and generating a Z_{th} curve, **Equation 2** can be applied to generate a fitted curve **Figure 3**:

(2) $$Z_{th(t)} - \sum_{i=1}^{n} R_i * \left[1 - exp\left(-\frac{t}{\tau_i}\right)\right]$$

(3) Where: $\tau_i = R_i * C_i$

The model parameters R_i and C_i are the thermal resistances and capacitances that build up the thermal model depicted in **Figure 2**. The parameters in the analytical expression can be optimized until the time response matches the transient system response by applying a least square fit algorithm. It allows application engineers to perform fast calculations of the transient response of a package to complex power profiles.

The individual expression, "i", also draws parallels with the electrical capacitor charging equation. **Figure 3** shows how the individual R_i and C_i combinations, sum to make the Z_{th} curve.

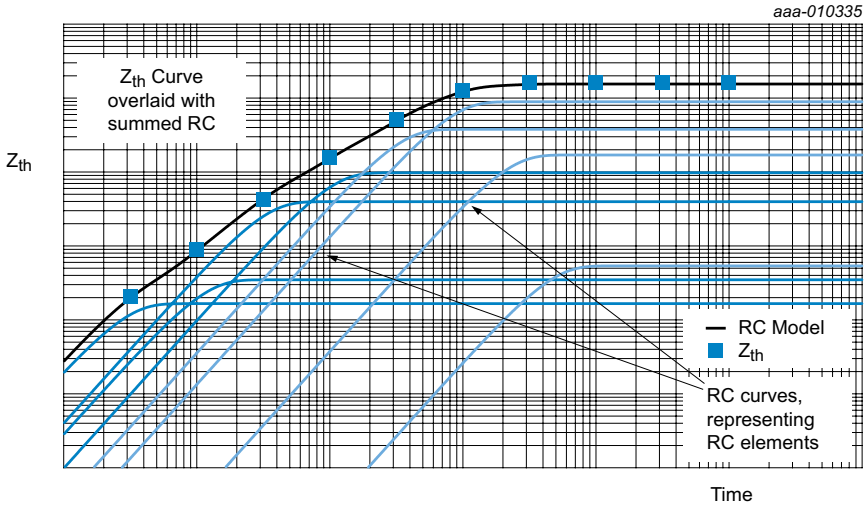
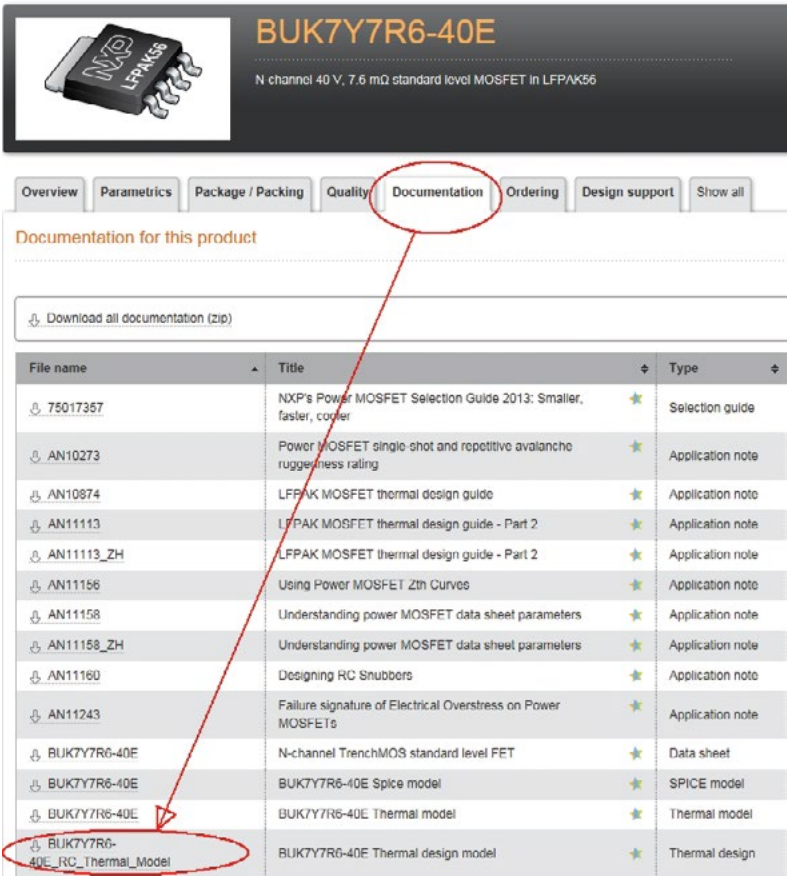


Fig 3. Foster RC thermal models

NXP provides Foster RC models for most of their Automotive Power MOSFET products. The models can be found under the tab "Documentation" > "BUK7Y7R6-40E_RC_ Thermal_Model" as demonstrated in **Figure 4**.



aaa-010336

Fig 4. NXP RC thermal model documentation

3.6 Thermal simulation examples

3.6.1 Example 1

RC thermal models are generated from the Z_{th} curve. This example shows how to work back from an RC model and plot a Z_{th} curve within a SPICE simulator. It allows for greater ease when trying to read values of the Z_{th} curve from the data sheet.

This and subsequent examples use the RC thermal model of BUK7Y7R6-40E. T_{mb} represents the mounting base temperature. It is treated as an isothermal and for this example it is set as 0 °C. A single shot pulse of 1 W power is dissipated in the MOSFET. Referring to **Figure 5**; for a single shot pulse, the time period between pulses is infinite and therefore the duty cycle $\delta = 0$. Then the junction temperature T_j represents the transient thermal impedance Z_{th}.

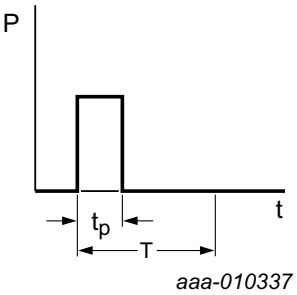


Fig 5. Single-shot pulse

Equation 4 and **Equation 5** demonstrate why T_j is used to represent the transient thermal impedance Z_{th} in this simulation.

$T_{mb} = 0$ °C

$P = 1$ W

(4) $$T_j = T_{mb} + \Delta T = 0\ °C + \Delta T = \Delta T$$

(5) $$\Delta T = P^* Z_{th} = 1\ \text{W}^* Z_{th}$$

Equation 5 demonstrates that with P = 1 W, the magnitude of Z_{th} equates to ΔT.

The following steps are used to set up and run simulations:

1. set up the RC thermal model of BUK7Y7R6-40E in SPICE as shown in **Figure 6**
2. set the value of voltage source V_{mb} to 0, which is the value of T_{mb}
3. set the value of the current source I1 to 1
4. create a simulation profile and set the run time to 1 s
5. run the simulation
6. Plot the voltage at node T_j

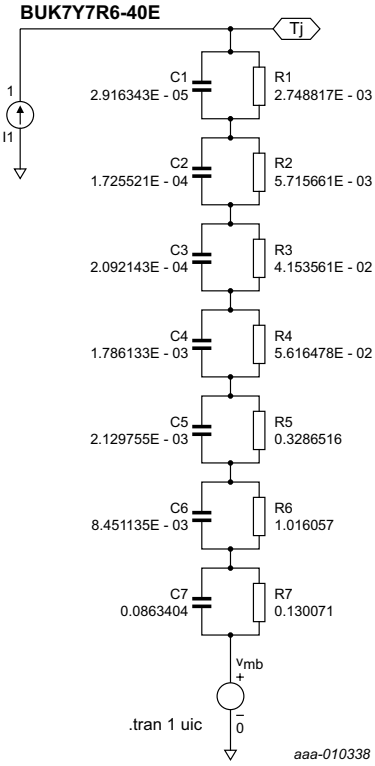


Fig 6. BUK7Y7R6-40E Thermal Model setup in SPICE

The simulation result in **Figure 7** shows the junction temperature (voltage at T_j) which is also the thermal impedance of BUK7Y7R6-40E. The values of Z_{th} at different times can be read using the cursors on this plot within SPICE.

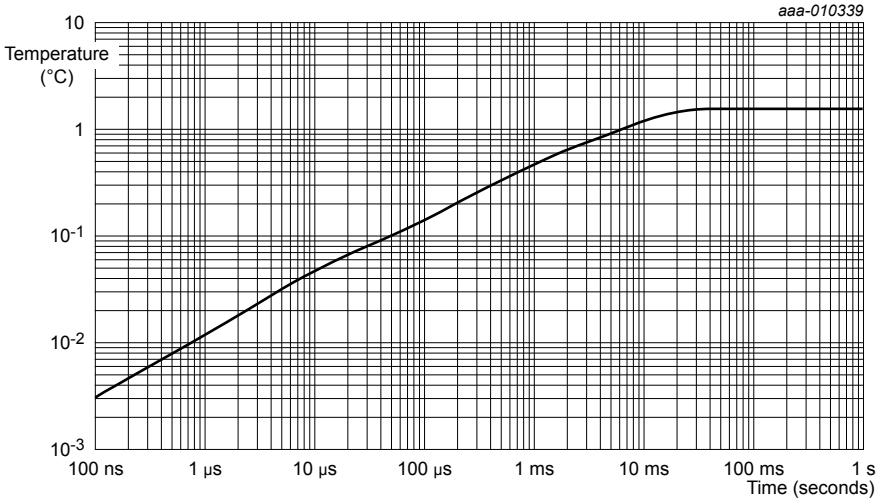


Fig 7. A plot of T_j from after simulation

The value of the current source in this example is set to 1 A to represent 1 W dissipating through the device. It can be easily changed to represent any value of power. The simulation command can be changed for any duration to represent a range of square power pulses.

3.6.2 Example 2

Another method of generating the power profile, is to use measurements from the actual circuit. This information is presented to the SPICE simulation in the form of a comma-separated value (CSV) file giving pairs of time/power values. It can be generated either as a summary of observations showing the points of change or from an oscilloscope waveform capture.

Two further methods of generating a power profile are discussed. One method is using a PWL file. The other is to generate the power from an MOSFET electrical circuit modeled in SPICE. The former is outlined first.

A source within a SPICE simulator can use a PWL file as an input. The contents of a typical PWL file is shown in **Table 3**. It can list the current, voltage or in this example, power over time. These files can be generated by typing values into a spreadsheet editor and saving as a .csv file, or alternatively exporting waveforms from an oscilloscope. The actual file itself should not contain any column headings.

To implement this procedure within a SPICE environment, follow the same steps as described in **Section 3.6.1 "Example 1"**, but with the exceptions:

1) Set the property value of the current source to read from a PWL FILE and point it to a .csv file for example: C:\Pulse file\filepulse.csv, which contains the power profile listed in **Table 3**.

2) Set the mounting base T_{mb} (V_{mb}) to 125.

3) Set the simulation run time to 3.5 s

Table 3. Data example for use in a PWL file

Time (seconds)	Power (Watts)
0	0
0.000001	30
0.015	30
0.015000001	6
1.1	6
1.100001	6
1.100002	20
1.5	20
1.500002	20
1.500003	0
1.6	0
1.600001	20
1.615	20
1.615001	6
2.9	6
2.900001	0
3	0
3.000001	30
3.015	30
3.015001	6

The simulation result is shown in **Figure 9**. The junction temperature and thermal impedance values labeled in **Figure 9**, demonstrate that the Z_{th} value at 3 ms, and R_{th} value, are in line with **Figure 10**. It represents the thermal impedance waveform shown in the BUK7Y7R6-40E data sheet.

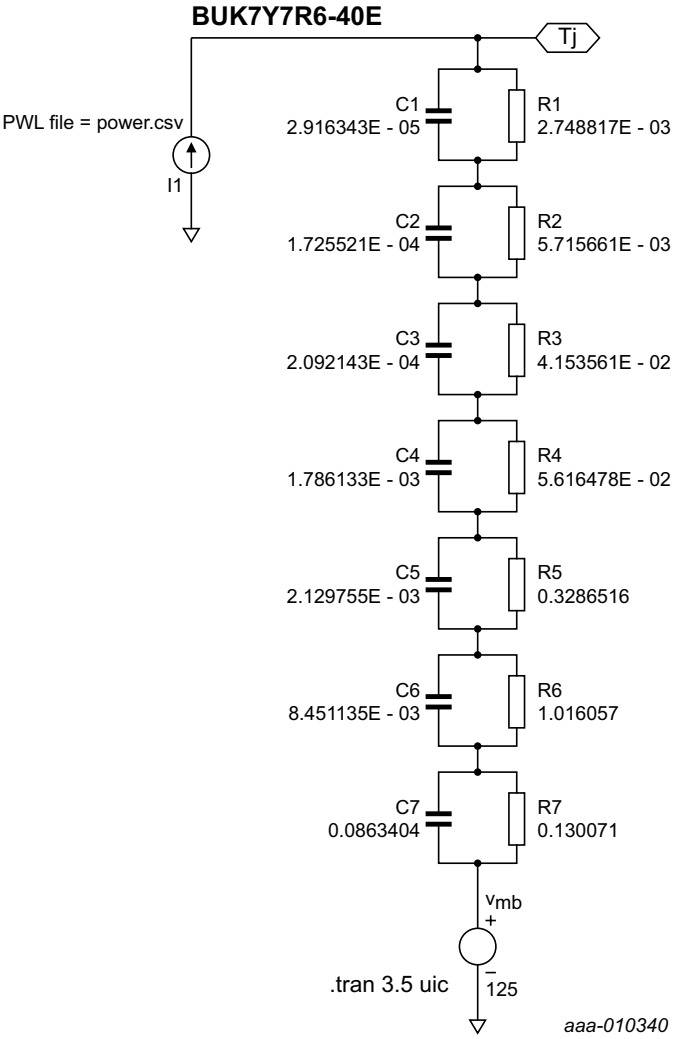


Fig 8. SPICE circuit implementing a PWL file with the thermal model of the BUK7Y7R6-40E

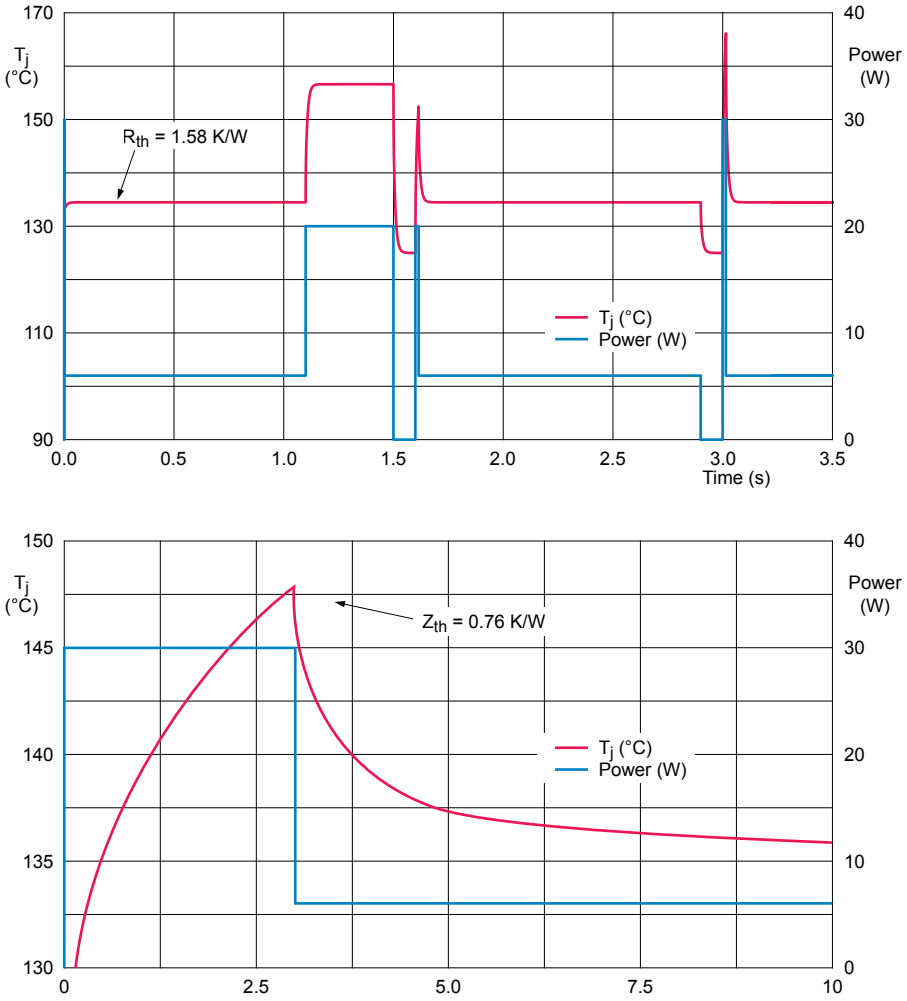
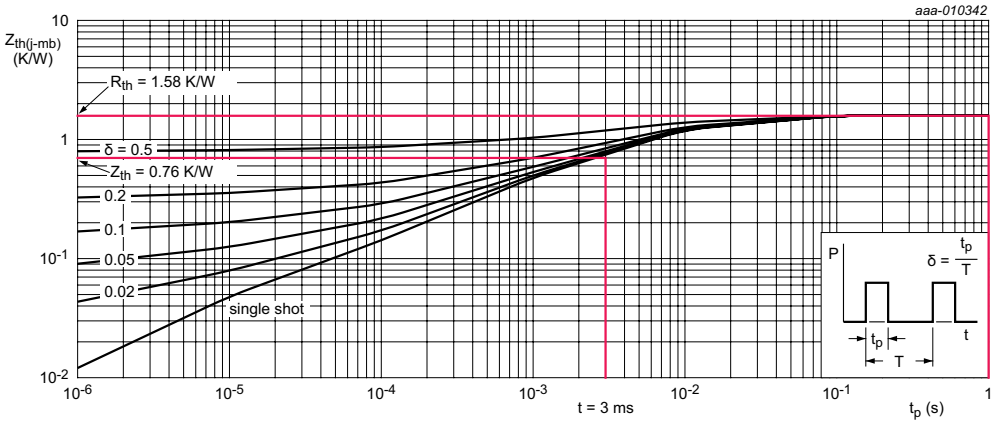


Fig 9. a. simulation results: b. reduced time axis of (a) showing the first power pulse



The red lines highlight the thermal resistance and impedance for the example shown in **Figure 9**

Fig 10. Transient thermal impedance for BUK7Y7R6-40E

3.6.3 Example 3

The aim of this example is to show how to perform thermal simulation using the power profile generated from a MOSFET circuit.

Following the steps in **Section 3.6.1**, set up the thermal model of BUK7Y7R6-40E, and set the mounting base temperature to 85 °C.

To set the power value in the current source, construct a MOSFET electrical circuit as provided in **Figure 11**. The power supply is 14 V and the load is a 0.1 Ω resistance. The gate drive supply is assigned a value of 10 V. It is set to run for 50 cycles with a 1 ms period and a 50 % duty cycle.

The power dissipated in the MOSFET can be calculated from **Equation 6** or for greater accuracy; the gate current can be included into the calculation to give **Equation 7**:

(6) $$P = V_{ds} * I_d$$

To improve accuracy:

(7) $$P = V_{ds} * I_d + V_{gs} * I_g$$

The current source into the thermal model can now be defined as:

(8) $$I = V_{(d)} * I(V_d) + V_{(g)} * I(V_g)$$

Figure 11 demonstrates the link between the electrical circuit and the thermal model circuit.

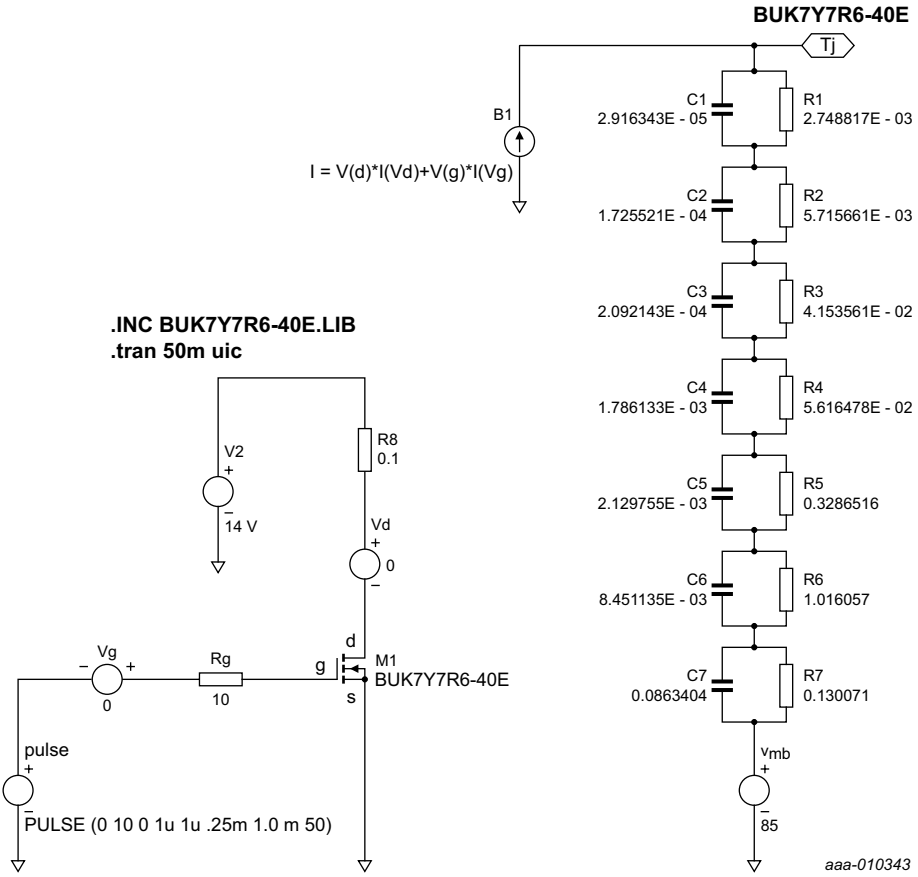


Fig 11. SPICE circuit illustrating how to integrate an electrical circuit with a thermal model

The resultant plot of T_j is shown in **Figure 12**. The maximum temperature of the junction can once again be calculated from data sheet values by following the steps outlined in **Ref. 1**.

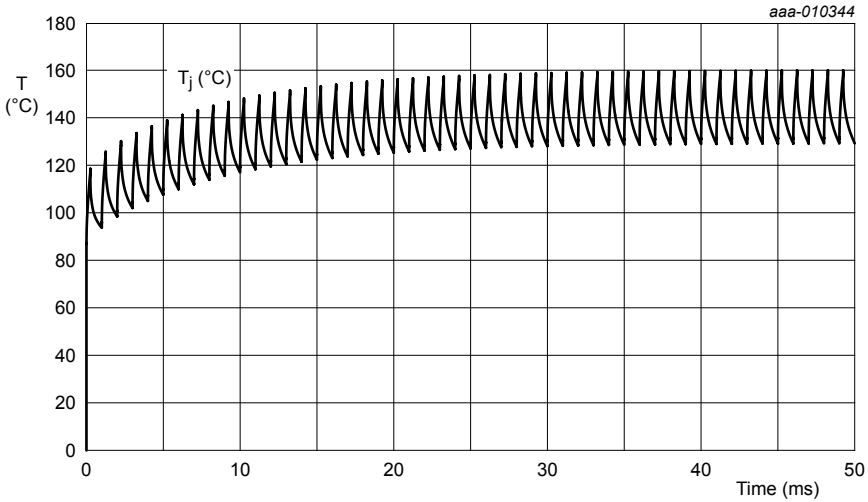


Fig 12. Inferred junction temperature (T_j) rise, provided by the circuit in **Figure 11**

3.7 Discussions

RC thermal models are not perfect. The physical materials used to build Semiconductors have temperature-dependent characteristics. These characteristics mean that thermal resistance is also a temperature-dependent parameter. Whereas in ohm's law, the ohmic resistance is constant and independent of the voltage. So the correspondence between electrical and thermal parameters is not perfectly symmetrical but gives a good basis for fundamental thermal simulations.

In power electronic systems, the thermal resistance of silicon amounts to 2 % to 5 % of the total resistance. The error resulting from the temperature dependence is relatively small and can be ignored for most cases. To obtain a more accurate analysis, replace the passive resistors in the RC model with voltage-dependent resistors. In these resistors, the change in temperature can correspond to change in voltage.

A further limitation of the models presented is that the mounting base temperature of the MOSFET T_{mb}, is set as an isothermal. This is rarely the case in real applications where a rise in the mounting base temperature must be considered. This rise is determined by calculating the temperature rise due to the average power dissipation (i.e. the heat flow) from the mounting base through to ambient. It means that the models are of limited use for pulses greater than 1 s, where heat begins to flow into the environment of the MOSFET. In this situation, the thermal model for the MOSFETs, PCB, heat sink and other materials in proximity must be included. However these components cannot be connected to the Foster RC models.

3.8 Summary

RC thermal models are available for NXP power MOSFETs on the NXP website. The models can be used in SPICE or other simulation tools to simulate the junction temperature rise in transient conditions. They provide a quick, simple and accurate method for application engineers to perform the thermal design.

3.9 References

[1] Application note AN11156 - “Using Power MOSFET Z_{th} Curves”. NXP Semiconductors

[2] Application note AN10273 (Chapter 2 of this book) - “Power MOSFET single-shot and repetitive avalanche ruggedness rating”. NXP Semiconductors

[3] Combination of Thermal Subsystems Modeled by Rapid Circuit Transformation. Y.C. Gerstenmaier, W. Kiffe, and G. Wachutka

Chapter 4: LFPAK MOSFET thermal design - part 1

Chapter 4: LFPAK MOSFET thermal design - part 1

4.1 Introduction

4.1.1 The need for thermal analysis

Power MOSFETs are commonplace in modern electronic circuit design, where they are frequently used to switch loads of many different types – ranging from a few milliamps or less to several tens of amps, depending on application. The popularity of power MOSFETs is almost certainly attributable to their ease of drive compared to their bipolar counterparts, together with the wide range of package, voltage and $R_{DS(on)}$ combinations which are now available.

Of course, MOSFETs are not perfect switches and neither are they indestructible, and the circuit designer should be aware of the following thermal considerations when designing a system employing MOSFET devices:

- Even when fully turned on, a MOSFET will dissipate power due to $I^2.R_{DS(on)}$ losses (where $R_{DS(on)}$ is the device on-state resistance)
- $I^2.R_{DS(on)}$ losses will result in temperature rises in the device and elsewhere
- MOSFETs may be damaged or destroyed by excessive device temperature

Thermal aspects are an important concern when designing with power MOSFETs, especially in applications which may be operating at elevated ambient temperatures, as the MOSFET junction temperature (T_j) must be kept below 175 °C if operation is to remain within specification. It is also important to bear in mind that the PCB to which the (surface-mount) MOSFETs are soldered will also have a maximum operating temperature of around 120 °C. The MOSFETs will be using the PCB as their primary method of heatsinking, and their dissipated heat energy will also cause PCB temperatures to rise. Care must therefore be taken that the PCB temperatures also remain within acceptable limits.

4.1.2 MOSFET R_{th} parameters and their limitations

In order to provide some measure of device thermal performance, it is normal industry practice for MOSFET data sheets to carry "thermal resistance" (R_{th}) figures. The concept of "thermal resistance" is analogous to that of electrical resistance, and is described in many texts on thermal management.

The two most common MOSFET thermal resistance values in data sheets are:

$R_{th(j-a)}$: The thermal resistance from device junction (die) to ambient. This is a single thermal resistance figure and is the net effect of all the possible series and parallel paths from junction to ambient. Typically this would include heat loss paths directly from the surface of the device package and also via the PCB to which the device is soldered.

$R_{th(j-mb)}$: The thermal resistance from junction to mounting base. "Mounting base" is defined as the point at which the device would normally be soldered to a PCB, and is primarily a conduction path only.

The methods and conditions under which device thermal resistance figures should be measured are described in the JESD51-x series of standards, and as one might expect, the standards are very precise in their descriptions of how testing should be carried out. It might therefore be expected that the thermal resistance figures would be sufficient for a designer wishing to carry out thermal analysis of a system. Unfortunately, this is not the case, for the following reasons:

- $R_{th(j-a)}$ figures are highly dependent on PCB construction and layout, and the PCBs defined in the JESD51 standards are not generally representative of those found in real applications
- The PCBs specified by MOSFET manufacturers for their $R_{th(j-a)}$ data sheet figures almost never follow the JEDEC guidelines anyway, are often described in only the vaguest of terms and are inconsistent from manufacturer to manufacturer
- The $R_{th(j-a)}$ test methods do not allow for several devices mounted in close proximity on the same PCB (a typical arrangement in a real-life application)
- Thermal resistance $R_{th(j-mb)}$ is only one part of the total thermal pathway from junction to ambient

Clearly then, the thermal resistance figures $R_{th(j\text{-}mb)}$ and $R_{th(j\text{-}a)}$ as published are of little practical use in the thermal analysis of real-life circuits and systems. In fairness to JEDEC, R_{th} figures were never intended to be used for design or system analysis, as this note from *specification JESD51-2* indicates:

"...The purpose of this document is to outline the environmental conditions necessary to ensure accuracy and repeatability for a standard junction-to-ambient ($R_{th(j\text{-}a)}$) thermal resistance measurement in natural convection. The intent of ($R_{th(j\text{-}a)}$) measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment."

Sadly, despite this clear statement from JEDEC, we still see many instances of designers attempting to use data sheet R_{th} figures in thermal design and analysis exercises.

4.1.3 Aim of this chapter

Having determined that the data sheet R_{th} figures are not appropriate for carrying out thermal analysis of real-life applications, it is natural to ask: what is the alternative? Unfortunately there is no simple method of thermal analysis which is applicable to complex situations whilst offering a reasonable degree of accuracy. The heat transfer mechanisms involved are simply too complex with too many interacting thermal pathways to allow for a simple yet valid method of analysis. In general, such analysis may only be carried out by either:

- recreating the scenario in simulation using computer-based simulation

or

- building the scenario in real-life and performing an experimental evaluation

The former approach can yield accurate, rapid results at the cost of expensive software and the necessary skills required to operate it, whilst the latter incurs the time and cost associated with building and measuring a representative model.

We recognize that a third approach may also be of use, particularly in the early stages of PCB design, which bridges the gulf between the less-than-helpful R_{th} figures at one extreme and full prototype simulation or build at the other. This chapter will illustrate, in general terms, the different techniques which may be applied to typical PCB design, in order to steer the layout towards one which has optimum thermal performance. Factors which will be considered include:

- PCB layer stack-up
- The influence of common circuit topologies on PCB layout
- PCB copper area
- The influence of thermal vias
- Device placement and spacing
- The implications of multiple dissipating devices on a single PCB

This chapter cannot hope to address all the myriad possible combinations of device placement, layer stack-up and so forth. Rather, its intention is to provide initial guidance to the engineer who, faced with a brand new design task, and a lack of helpful information, may be asking himself; “How can I be sure my devices will run at safe temperatures?”

Finally, it almost goes without saying that the information contained within this design guide is presented as a starting point only. Any new design should of course be prototyped and its thermal behavior characterized before placing the design into production.

4.2 General approach to thermal analysis

4.2.1 The use of thermal simulation software

In order to allow fast and flexible analysis of multiple parameter variations, the thermal analyses presented in this chapter have been carried out using thermal simulation software. The simulations use MOSFET models which have been validated against empirical data and are known to accurately model the thermal behavior of real-life devices.

The thermal simulation software used to carry out the analyses is the Mentor Graphics (Flomerics) “Flotherm” package. The device models used in the analysis are available for free download from the NXP Semiconductors website.

4.2.2 Simulation set-up

The PCBs to be considered have the following general characteristics:

- They are surface-mount designs and the MOSFETs are in the surface-mount LFPAK packages
- PCB stack-ups range from 1 to 4-layer construction, but always have an overall thickness of 1.6 mm
- PCB material is standard FR4, with a rated maximum operating temperature of 120 °C
- Copper thickness on all layers is 1 oz./ft^2 (35 µm)
- The PCB is suspended in free air

Other important factors:

- The ambient temperature is 20 °C
- The simulations solve for conduction, convection and radiation heat transfer
- MOSFET power dissipation is 0.5 W per device
- There is no forced air cooling applied i.e. only natural convection is modeled

4.2.3 PCB layout and stack-up

4.2.3.1 Factors influencing, PCB layout and stack-up

When laying out a PCB we do not have a completely free choice as to where we can place the MOSFET devices and other components and how we connect them together. Usually, device placement and connection is a question of reconciling various (often conflicting) requirements. The factors influencing component placement may include:

- Circuit topology
- Design for ElectroMagnetic Compatibility (EMC)
- Design for thermal performance
- The necessity to situate certain components (e.g. connectors) in pre-defined locations
- The need to provide low-resistance and low-inductance current paths in specific areas

If we are considering a PCB design from a thermal perspective, then the ideal thermal design may have to be compromised in some respects in order to accommodate the other requirements placed on the design.

4.2.3.2 Circuit topology

Circuit topology is perhaps the least flexible of all the factors influencing PCB design. After all, if the components are not connected together in the proper manner then the circuit will not function as expected. The topology will also dictate which MOSFET terminals may be connected to copper planes and hence may use those planes to help dissipate heat energy. This is particularly important for a surface-mount package such as LFPAK, where the primary thermal pathway out of the package is through the device drain tab on the underside of the device. Circuit topology therefore has a very great influence on the thermal design and consequent device operating temperatures.

Several different topologies will be considered in this guide, and it is believed that these will be relevant to a large number of typical end-user applications.

4.2.3.3 Design for ElectroMagnetic Compatibility (EMC)

The subject of design for electromagnetic compatibility is a complex one and is well beyond the scope of this publication. However, one of the simpler aspects of design for EMC is highly relevant to thermal design - the provision of a ground plane layer in the PCB.

From an EMC perspective, a multilayer PCB should have at least one copper layer which is used exclusively as a ground plane, and which has a minimum of holes and breaks in it. This requirement is not in conflict with good thermal design - indeed, the presence of a continuous layer of copper in the PCB stack-up can only enhance the thermal performance of the board as a whole. PCB layouts which incorporate a dedicated ground plane will be considered in all of the following analyses.

4.3 A single LFPAK device

This section will examine the factors influencing the thermal performance of a single LFPAK device on PCBs of several different configurations. From this point onward the phrase “thermal performance” is used when discussing the ability of a stack-up or structure to remove heat energy from the device(s). In order to build up a comprehensive picture of the factors influencing thermal performance, we will begin with the simplest 1-layer stack-up and then systematically add additional layers to the PCB.

4.3.1 Analysis 1: A single-layer PCB

The simplest possible PCB stack-up is that of a single top copper layer; a 1-layer stack-up. In analysis 1 we will examine the variation in device junction temperature (T_j) as a function of top copper area. See **Figure 1**.

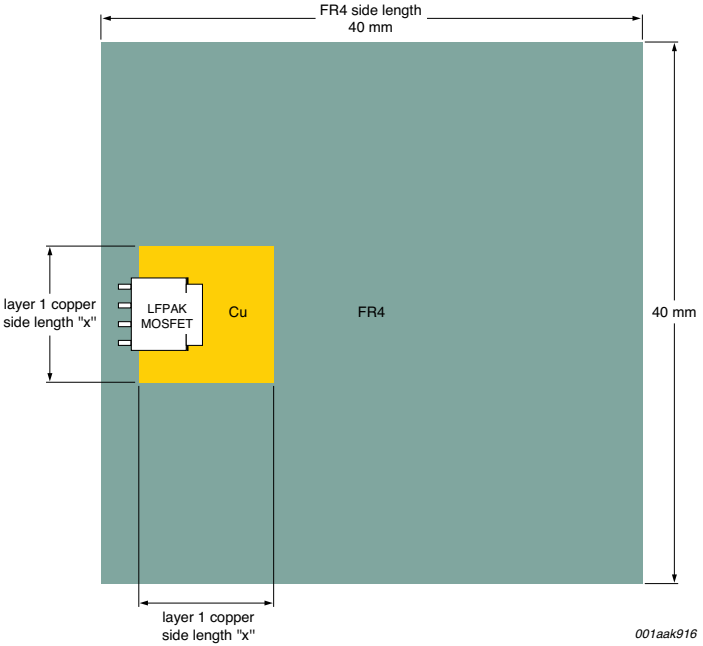
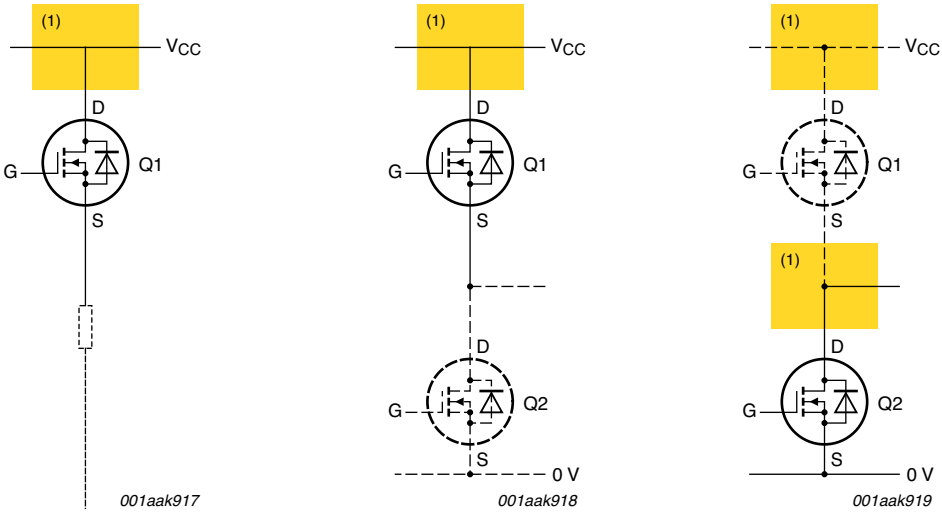


Fig 1. Single device; 1-layer stack-up

Figure 1 illustrates the MOSFET device mounted on a square area of layer 1 copper of side length "x" and with FR4 of size 40 mm x 40 mm. Three possible circuit configurations corresponding to this layout are shown in **Figure 2**.



(1) Plane available for cooling

a. High-side load switch set-up: MOSFET Q1

b. Half-bridge set-up: MOSFET Q1 and Q2

c. Half-bridge set-up: MOSFET Q2 and Q1

Fig 2. Three possible circuit configurations for the layout of **Figure 1**

Figure 2(a) shows MOSFET Q1 configured as a high-side load switch, with its drain tab connected to the V_{CC} plane (in yellow). **Figure 2**(b) and **Figure 2**(c) demonstrate MOSFETs Q1 and Q2 connected in a half-bridge configuration. Again, both devices are primarily cooled by planes connected to their drain tabs, although for Q2 the plane corresponds to the mid-point of the half-bridge rather than a power plane. A small degree of additional cooling may also be realized by attaching planes to the MOSFET sources, although the source pins are not the primary heat path out of the package and so the additional benefit is minimal. Generally speaking, the primary heat path is through the package drain tab and into whatever plane is attached to this connection, and it is this configuration which will be considered in this guide.

By carrying out simulations for several sizes of "x" we can determine how the device junction temperature (T_j) varies with copper area. The results are shown in **Figure 3**. Remember that the ambient temperature is 20 °C.

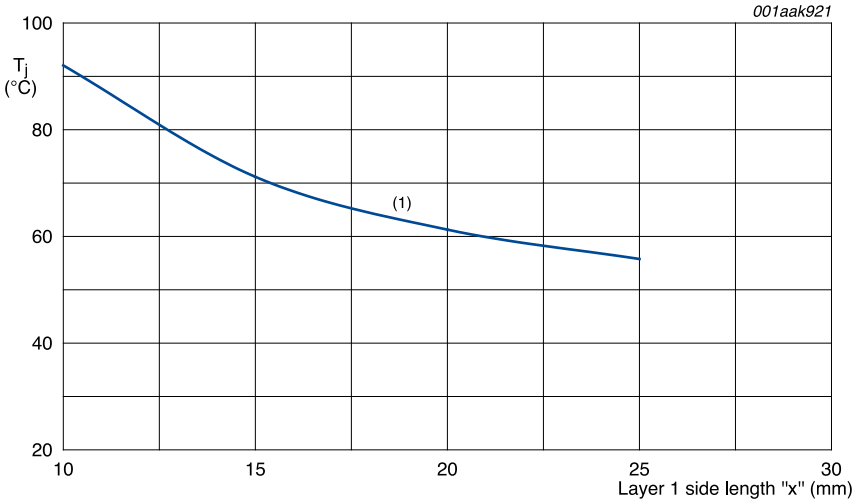


Fig 3. Device junction temperature versus layer 1 top copper side length "x"

The graph of **Figure 3** has two notable features:

- T_j depends greatly on side length "x" and hence layer 1 copper area
- The ability of the top copper to provide heatsinking for the MOSFET displays the "law of diminishing returns". In other words, we cannot keep adding more copper area to layer 1 in the hope of continuing to reduce T_j. Rather, from the shape of the curve we might conclude that T_j will never decrease below, say 50 °C no matter how much copper area we provide on layer 1

Section 4.1.1 it was stated that there are in fact two limiting temperatures which must not be exceeded - MOSFET Tj and the temperature of the PCB material T_{PCB}. For surface-mount MOSFETs, the point of maximum T_{PCB} will usually occur under the centre of the MOSFET tab, as one might expect. For MOSFETs in the LFPAK package, T_{PCB} will typically track T_j to within less than 0.5 °C, and therefore we can reasonably say that $T_{PCB} \approx T_j$. This assumption will be made for the remainder of the analyses of the LFPAK package. The results of **Figure 3** therefore indicate that, for a PCB whose T_{PCB} (max) is 120 °C, we should not encounter problems with PCB degradation for even the smaller areas of layer 1 copper area, provided that the ambient temperature stays below approximately 45 °C.

4.3.1.1 The role of FR4 size in analysis 1

The choice of FR4 PCB area in **Section 4.3.1** may seem both arbitrary and unrepresentative of the PCB size in a real-life application. In this section, however, we will see that the area of bare FR4 has almost no influence on device (T_j). To demonstrate this principle, additional simulations were carried out with FR4 dimensions of 20 mm x 20 mm, 30 mm x 30 mm, 50 mm x 50 mm, with the layer 1 copper area fixed at 10 mm x 10 mm. The results are shown in **Figure 4**.

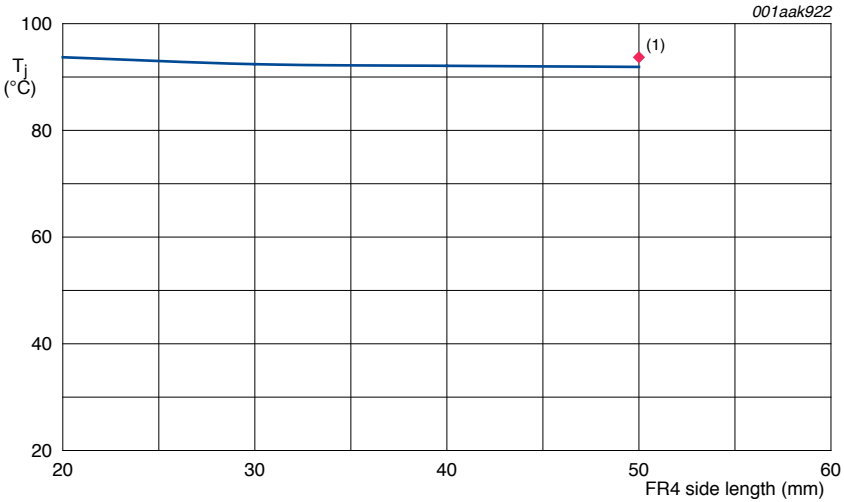


Fig 4. Junction temperature versus FR4 side length

The results of **Figure 4** demonstrate that the size of bare FR4 has almost no impact on device T_j. This is in marked contrast to the results of **Figure 3** where we varied the layer 1 copper area. The difference between the two sets of results is easily understood when we compare the thermal conductivities of copper and FR4; copper has a thermal conductivity of around 380 W/(m.K) whilst for FR4 the figure is only around 0.6 W/(m.K). As thermal conductivity is a measure of how easily heat energy travels through a substance, it should be clear that adding even a large area of FR4 (which is a poor conductor) is nowhere near as effective as adding a much smaller area of highly conductive copper

We can further illustrate the insulating properties of FR4 by adding some unconnected areas of layer 1 copper to the model, as shown in **Figure 5**.

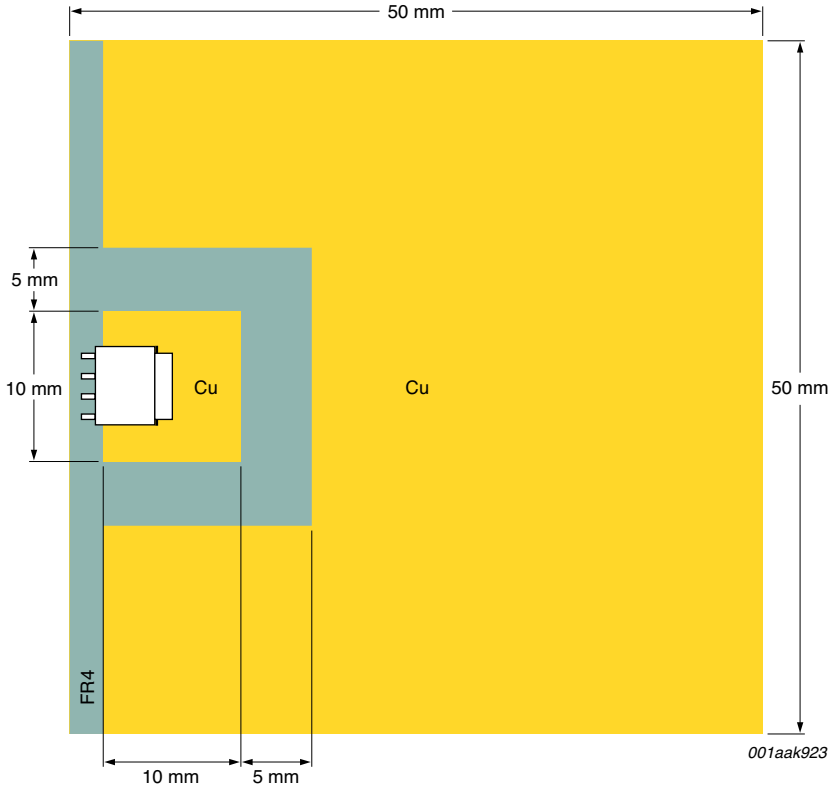


Fig 5. Adding additional layer 1 copper to the 50 mm x 50 mm FR4 board

Figure 5 shows the 50 mm x 50 mm FR4 layout with most of the layer 1 area filled with a "flood" of copper. A gap of 5 mm has been left around the device and its attached 10 mm x 10 mm copper area. Although we might have expected the additional layer 1 copper to make a significant difference to device T_j, in fact this is not the case. The heat energy is prevented from utilizing the additional "heatsinking" area by the isolation gap around the device and the poor thermal conductivity of the intervening FR4. The ability of FR4 to "thermally isolate" heat sources in this way is important and will be demonstrated again in **Section 4.4** "Two LFPAK devices" on page 103 and **Section 4.5** "Four LFPAK devices" on page 113.

4.3.2 Analysis 2: 2-layer PCB

For the purposes of this exercise we will again consider the same variations in layer 1 copper as for analysis 1. However for analysis 2 we will add the layer 4 (bottom copper) layer measuring a fixed 25 mm x 25 mm, thereby creating a 2-layer stack-up. The bottom copper layer is shown in **Figure 6**.

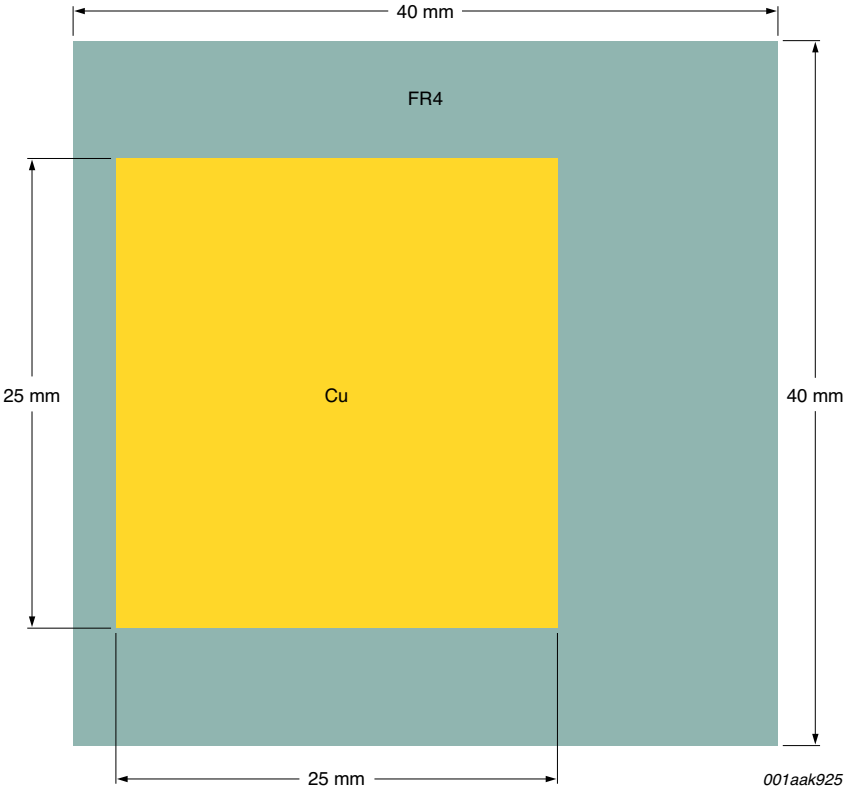


Fig 6. Layer 4 copper

In practical terms this layer might be a ground or power plane, although the device is not electrically connected to this layer.

As with analysis 1 (**Section 4.3.1** on page 88), we can again carry out simulations for various layer 1 side length “x”, keeping the size of the layer 4 plane constant at 25 mm x 25 mm. The results are shown in **Figure 7**, together with those from analysis 1 for comparison purposes.

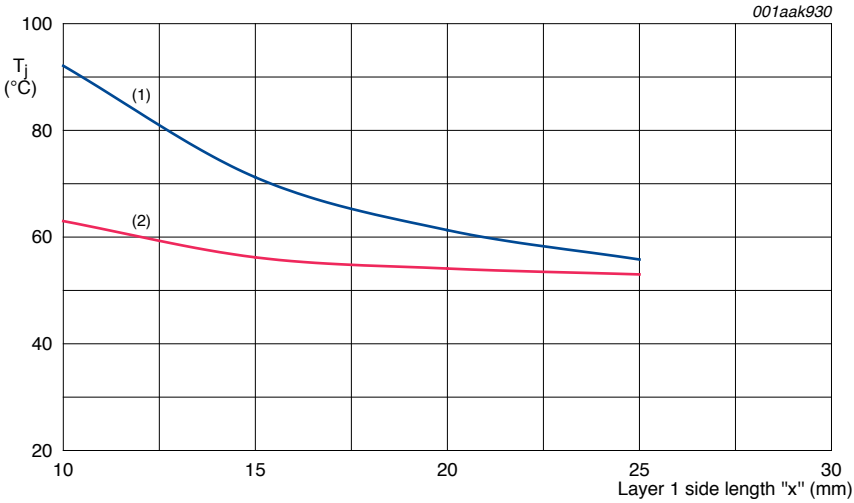
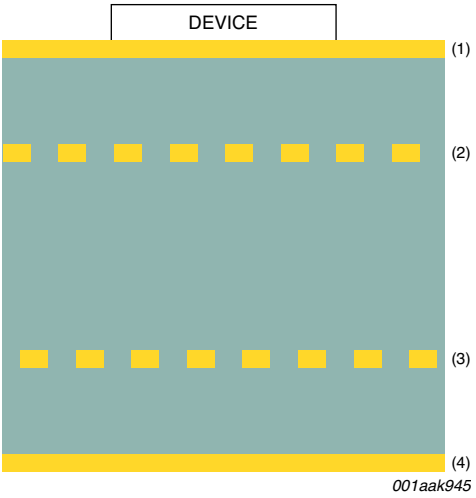


Fig 7. Device junction temperature versus layer 1 copper side length “x” for the 1 and 2-layer PCB stack-ups

Figure 7 demonstrates that adding the layer 4 copper has significantly improved the thermal performance of the PCB, even though layer 4 is not directly connected to the MOSFET. We can also see that the MOSFET T_j is now somewhat less dependent on layer 1 copper area. By adding the second layer we can reduce the top copper side length from 25 mm x 25 mm to approximately 15 mm x 15 mm whilst retaining the same thermal performance (i.e. the same device T_j). This is certainly a useful result if we wish to increase component density on layer 1!

4.3.3 Analysis 3: A 4-layer PCB part 1

This chapter will consider several different variations of the 4-layer PCB stack-up. The simplest of these variations is based on the 2-layer stack-up of analysis 2 (**Section 4.3.2**), with the addition of two additional internal signal layers. It is assumed that the additional layers would be mainly composed of many thinner signal tracks, rather than large continuous planes. Detailed simulation of these layers is obviously not feasible, and so a "percentage coverage" method is adopted instead. With this method, the average conductivity of the structure is calculated based on the percentage of total area covered in copper and the layer thicknesses. For the purposes of these exercises, we will assume that the signal layers have 50 % copper coverage and are also of 1 oz./ft^2 (35 µm) thickness. The 4-layer structure is summarized in **Figure 8**.



(1) Layer 1, 35 µm, variable area.

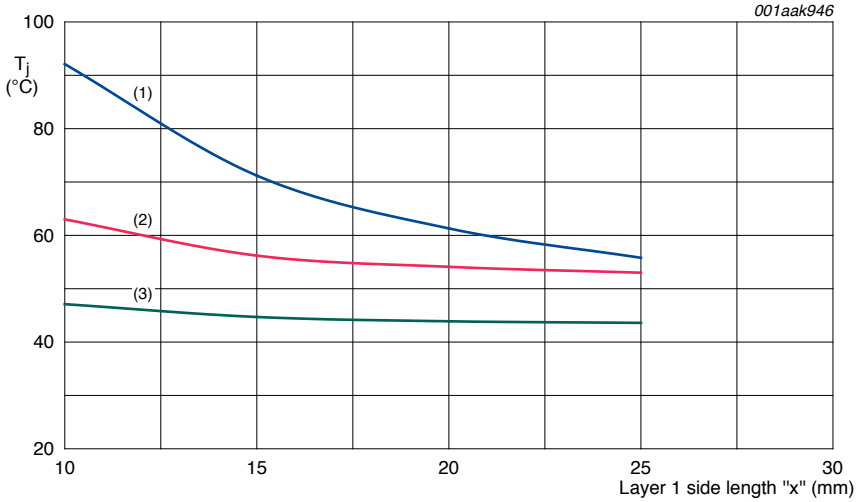
(2) Layer 2, 35 µm, 50 % coverage.

(3) Layer 3, 35 µm, 50 % coverage.

(4) Layer 4, 35 µm, 25 mm x 25 mm.

Fig 8. 4-layer stack-up for analysis 3, part 1 (not to scale)

As before, we will carry out simulations for various sizes of layer 1 copper, keeping the other layers constant. The results are shown in **Figure 9** together with those from the previous two analyses. Note that there is again no direct connection between the MOSFET and layer 4 plane, and the corresponding circuit topologies would be those shown in **Figure 2** on page 89.



(1) Layer 1 only.

(2) 2-layer.

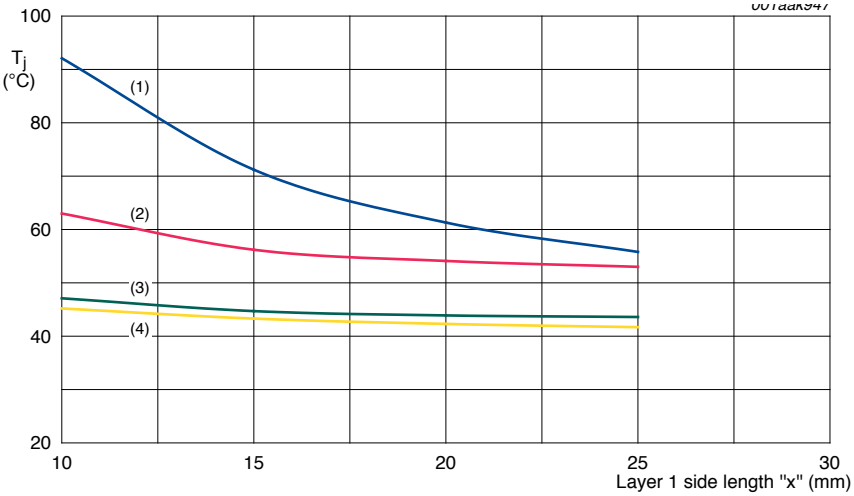
(3) 4-layer.

Fig 9. Device junction temperature versus layer 1 copper side length “x” for the 1, 2 and 4-layer PCB stack-up

Adding copper layers 2 and 3 to the design has resulted in a considerable reduction in T_j compared to the 1 and 2-layer stack-ups. In addition, it can be seen that T_j has become almost independent of layer 1 copper area. This is a useful result which indicates that, in a 4-layer PCB stack-up similar to that described here, we can reduce the layer 1 copper area to a minimum without drastically compromising the thermal performance of the design. The layer 1 copper area which has been freed up may therefore be used for mounting other devices, routing tracks, and so on.

4.3.4 Analysis 3: A 4-layer PCB part 2

The second 4-layer stack-up which will be considered is similar to that of **Figure 8**, except that layer 2 has been replaced with a plane of 100 % area coverage. This might represent an internal ground plane. Otherwise, the analysis is the same as that for part 2. The results are shown in **Figure 10**.



(1) Layer 1 only.

(2) 2-layer.

(3) 4-layer.

(4) 4-layer (layer 2 100 % coverage).

Fig 10. Device junction temperature versus layer 1 copper side length “x” for the 1, 2 and 4-layer PCB stack-ups, and for the 4-layer stack-up with layer 2 area coverage of 100 %

It is interesting to see that increasing the percentage coverage of layer 2 from 50 % to 100 % has yielded little improvement in thermal performance. In other words, an internal plane is less effective than an external plane in terms of reducing device temperature. This can be explained by understanding that an external plane is able to lose heat energy to the external environment by convection and radiation loss from its surface. An internal layer, however, is obviously not exposed to free air (except, perhaps, for a negligible amount at the plane's edges) and so the only contribution it makes to improved cooling is to increase the through-board conductivity of the PCB.

4.3.5 Analysis 4: A 4-layer PCB with thermal vias part 1

So far we have considered cases where the layer 1 copper (connected to MOSFET drain) has not been connected to any other layer. However, it is entirely possible that we would use a pattern of vias under the MOSFET tab to provide electrical connection with a V_{CC} plane on layer 4 (for instance). This approach is consistent with the topologies of **Figure 2**. As well as providing the necessary electrical connectivity, this arrangement will also provide an additional thermal pathway away from the MOSFET, whereby the "electrical vias" also function as "thermal vias".

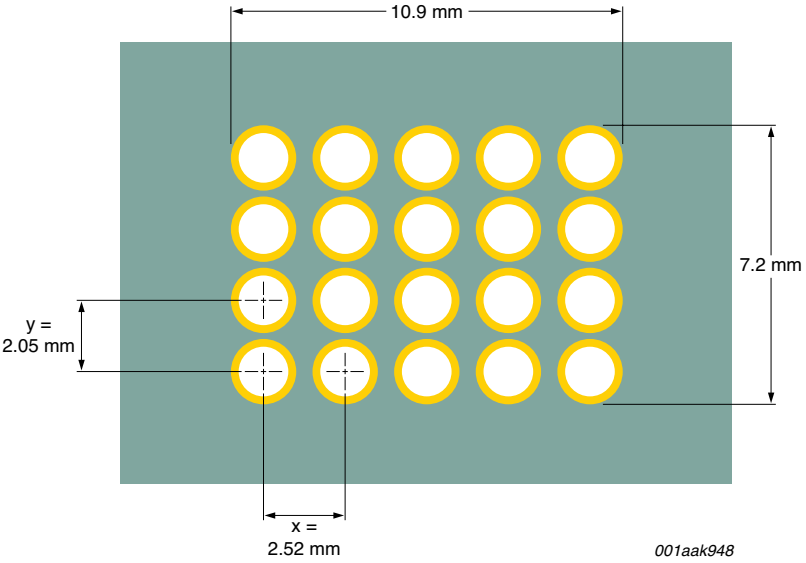
Whilst it is known that in general terms adding vias under a device will improve its thermal performance, it can be difficult to know how many vias provide an optimal solution. Obviously we do not want to add too many vias if they do not significantly improve thermal performance, as their presence may cause problems during PCB assembly (and, of course, we are paying for every via on the PCB!). The purpose of this analysis is therefore to examine the impact of various via patterns on the thermal performance of the design.

The analysis in this section will use a layer 1 copper area of side length 15 mm and will consider via patterns with the characteristics listed in **Table 1**. In all cases, vias are 0.8 mm diameter and are assumed to be air-cored. PCB stack-up is as **Figure 8**. An example via pattern is shown in **Figure 11**.

Table 1. Via patterns summarised

Number of vias			Via pitch x (mm)	Via pitch y (mm)	Overall via pattern dimensions (mm x mm)
Total	x	y			
0	0	0	-	-	-
20[1]	5	4	2.52	2.05	10.9 x 7.2
30	5	6	2.52	1.33	10.9 x 7.5
54	9	6	1.26	1.26	10.9 x 7.1
63	9	7	1.26	1.26	10.9 x 8.4
77	11	7	1.04	1.04	11.2 x 7.1

[1] See **Figure 11**.



Drawing not to scale.

Fig 11. The 5 x 4 via pattern

The results for the different via patterns are shown in **Figure 12**.

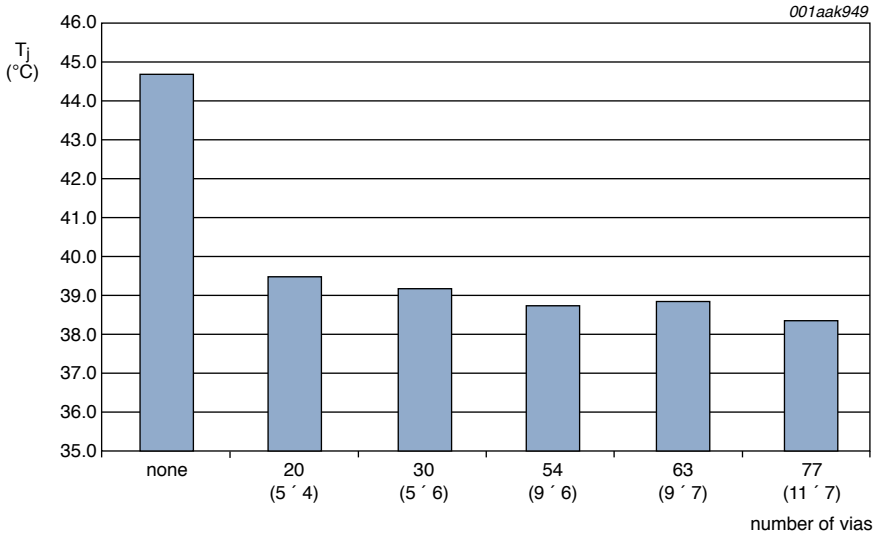
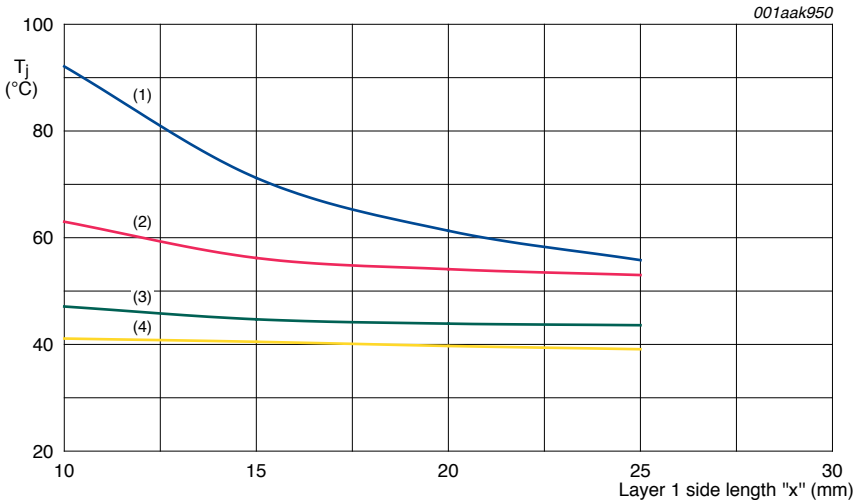


Fig 12. Device junction temperature versus the number of vias

Figure 12 demonstrates a notable decrease in device T_j when moving from a situation with no vias under the device to one of 20 vias under the device. This is a clear indicator that the heat energy is being conducted from the MOSFET drain tab to layer 4 and is exactly the result we would expect. It is interesting to note, though, that adding progressively more vias under the device results in little additional decrease in T_j. This is because, as we add more vias, so the through-board conductivity of the layout increases. However, at the same time we are also decreasing the area of contact between device and PCB as more layer 1 copper is replaced with air. Consequently we do not see much improvement in thermal performance. The conclusion we can therefore draw from this exercise is that adding some vias will improve thermal performance, but continuing to add more vias will not yield further significant performance improvements.

4.3.6 Analysis 4: A 4-layer PCB with thermal vias part 2

For completeness, the “4-layer plus vias” structure has also been simulated for several sizes of layer 1 copper, with the stack-up again as **Figure 8** on page 96. The results are shown in **Figure 13**.



(1) Layer 1 only.

(2) 2-layer.

(3) 4-layer.

(4) 4-layer; 5 x 4 vias.

Fig 13. Device junction temperature versus layer 1 copper side length “x” for the 1, 2 and 4-layer PCB stack-ups and for the 4-layer stack-up with vias

It can be seen that, once vias are added under the device, T_j becomes almost independent of top copper area, and is approximately 5 °C lower than for the 4-layer stack-up without vias.

4.3.7 Summary: factors affecting the thermal performance of a single device

- For a device mounted on a 1-layer PCB, device T_j depends heavily on copper area. However, the "law of diminishing returns" applies and simply adding more and more layer 1 copper does not yield commensurate improvements in thermal performance (see **Figure 3**). The lowest achievable T_j, with a large copper area, would be approximately 50 °C.
- Varying the size of the PCB FR4 does not significantly influence device T_j if the copper connected to drain is kept at a constant size. Similarly, adding unconnected copper areas onto an extended FR4 area also does not significantly influences T_j (see **Figure 4**).
- Adding a second copper layer (layer 4) provides a significant improvement in thermal performance and reduces the dependence of T_j on layer 1 copper area (see **Figure 7**).
- Moving to a 4-layer PCB stack-up again provides a significant improvement in thermal performance compared to 1- and 2-layer stack-ups. In addition, the dependence of T_j on layer 1 copper area is further reduced (see **Figure 9** and **Figure 10**).
- Adding vias under the device provides a further improvement in thermal performance, but once again the law of diminishing returns applies, whereby adding more and more vias yields little significant benefit (see **Figure 12**).
- With vias under the device, the dependence of T_j on layer 1 copper area is almost eliminated (see **Figure 13**).

The single device configuration with 15 mm x 15 mm top copper and 20 vias will be used as a building block in the analyses presented in the following sections (**Section 4.4.1** on page 105 to **Section 4.5.4** on page 117).

4.4 Two LFPAK devices

Section 4.3 considered the thermal performance of a single device mounted on a section of PCB. The next level of complexity in this analysis is that of two devices mounted on a PCB, where we will observe the effect of device separation on T_j. In order to restrict the number of variables to a sensible limit we will consider only the 15 mm x 15 mm side-length area for layer 1. However, the PCB size has been increased to 120 mm x 80 mm to allow more scope for investigating different device separation distances. As before, we will begin with the simple 1-layer stack-up and then progressively add layers to the board.

The PCB top copper configuration is shown in **Figure 14**.

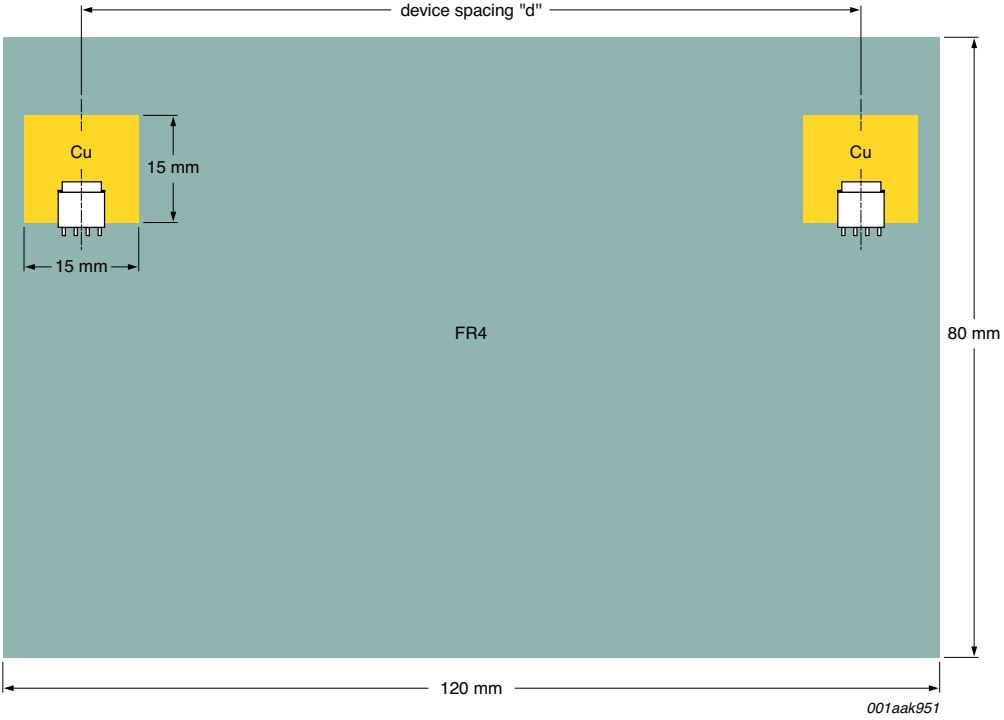
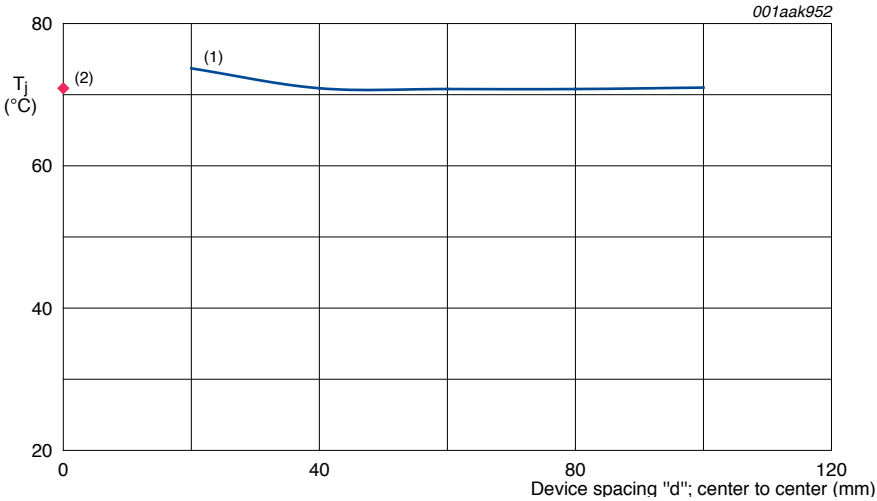


Fig 14. PCB top copper configuration for the analysis of two devices

Simulation were carried out to investigate the influence of “d” on device T_j for the various PCB stack-ups. Values of d varied from 100 mm (maximum separation, devices mounted near the PCB edges, as shown in **Figure 14**) to 20 mm, where there was only a 5 mm gap between the device layer 1 copper areas value.

4.4.1 Analysis 5: A single-layer PCB

The results for the single-layer simulations are shown in **Figure 15**. As the placement of the devices is symmetrical about the board centre line, regardless of d, the thermal performance of both devices is almost identical and so the T_j figure may be taken to be for either device. T_j for a single device, mounted near the PCB edge, is also shown.



(1) Layer 1 only.

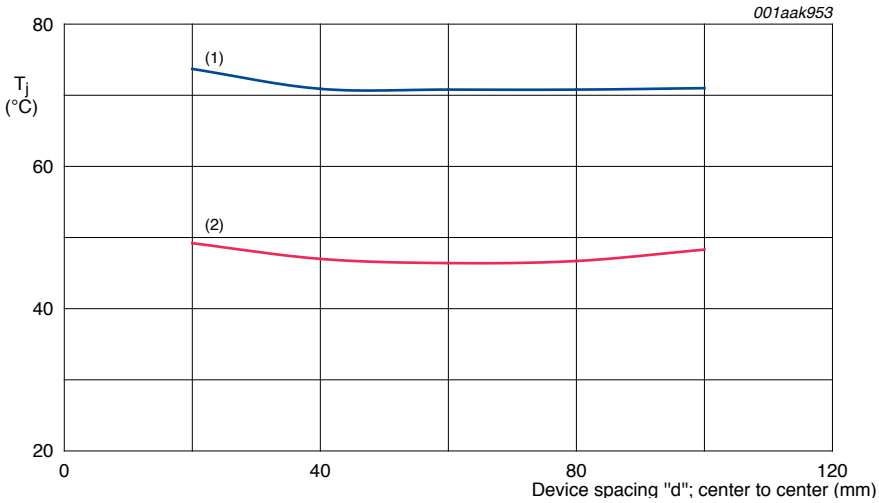
(2) Single device.

Fig 15. Simulation results for two devices of varying separation “d” on a single-layer PCB. The result for a single device mounted at the PCB edge is also shown

Even though the two devices are mounted on the same PCB, it is interesting to note that they perform as almost completely independent units – T_j is largely the same as for the single device and is not unduly influenced by device separation except for the case where the devices are mounted closest together (“d” at a minimum). This is a consequence of the poor thermal conductivity of the FR4 PCB material which effectively “isolates” the two devices in most cases, as discussed in **Section 4.3.1.1** on page 91.

4.4.2 Analysis 6: A 2-layer PCB

For the purposes of this exercise we will again consider the same variations in device spacing as for analysis 5 (see **Section 4.4.1**). However for analysis 6 we will add the layer 4 (bottom copper) layer covering the whole of the underside of the PCB and thereby creating a 2-layer stack-up. In practical terms this layer might be a ground or power plane, although as far as the board thermal performance is concerned it makes no difference as the devices are not connected to this layer. The results are shown in the graph of **Figure 16** together with those from analysis 5 for comparison purposes.



(1) Layer 1 only.

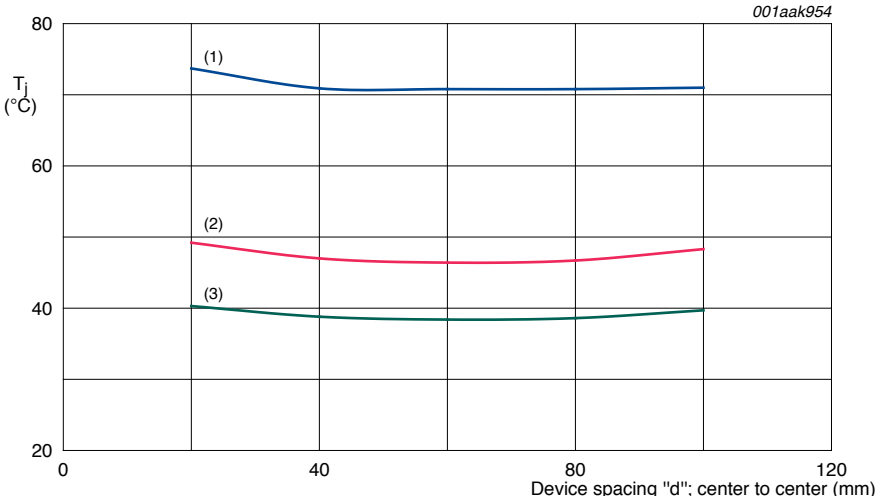
(2) 2-layer.

Fig 16. Simulation results for two devices of varying separation “d” on a 2-layer PCB

Adding the second copper layer has considerably reduced the junction temperatures of both devices, as one might expect, and temperature still remains largely independent of device separation.

4.4.3 Analysis 7: A generalized 4-layer PCB

The 2-layer stack-up of analysis 6 will now be increased to 4 layers with the addition of two internal signal layers. As before, it is assumed that these layers would be mainly composed of many thinner signal tracks, rather than large continuous planes. Simulation of the internal layers will again be by the "percentage coverage" method, with the assumption of 50 % copper coverage and 1 oz./ft^2 (35 µm) thickness. Layer 4 remains unconnected to either device, also as before. The 4-layer structure is therefore as summarized in **Figure 8**. Layer 4 remains a solid plane covering the entire underside area and junction temperatures are determined for various separation distances "d". The results are shown in **Figure 17**.



(1) Layer 1 only.

(2) 2-layer.

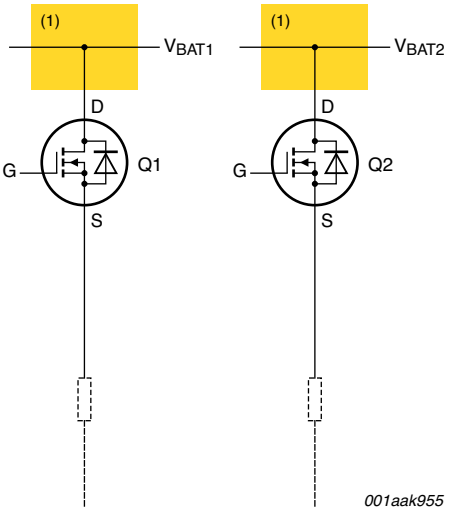
(3) 4-layer.

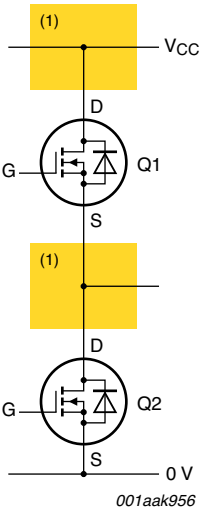
Fig 17. Simulation results for two devices of varying separation "d" on a 4-layer PCB

The addition of the two internal layers results in curve of similar shape to the 2-layer stack-up but with an overall reduction in T_j of approximately 10 °C.

4.4.4 Analysis 8: A 4-layer PCB with thermal vias part 1

In analyses 8 and 9 we will consider cases where the layer 1 copper (connected to MOSFET drains) is connected to layer 4 by thermal/electrical vias of the 5 x 4 via pattern described in **Section 4.3.6**. The layer 4 copper area will be reduced to two 15 mm x 15 mm planes, with a plane connected to each MOSFET. When using vias to connect one or more layers together for thermal reasons, we must also consider the implications for circuit topology and layer stack-up. For the configuration examined in this section, the possible circuit topologies are shown in **Figure 18**.





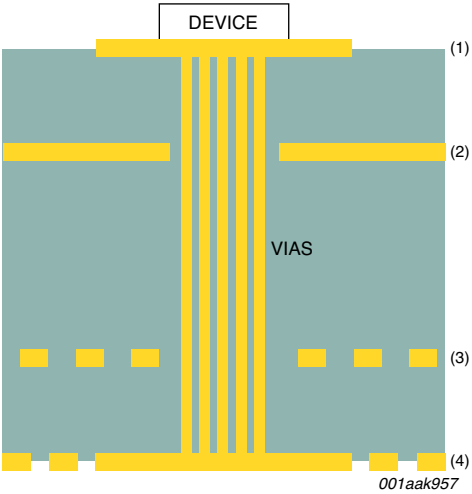
(1) Plane available for cooling

a. High-side load switches

b. Half bridge configuration

Fig 18. Possible circuit configurations for two MOSFETs with independently connected drains

Figure 18 demonstrates two possible circuit configurations for two MOSFETs with independently connected drains. **Figure 18**(a) shows two high-side load switches connected to different supply (V_{BAT}) lines – a common automotive configuration. **Figure 18**(b) we have the two MOSFETs connected in a half-bridge configuration typical of a unidirectional motor drive controller or DC-DC buck converter circuit. In both cases, the MOSFET drains do not share a common electrical connection. The modified layer stack-up corresponding to these topologies is shown in **Figure 19**.



(1) Layer 1 (power).

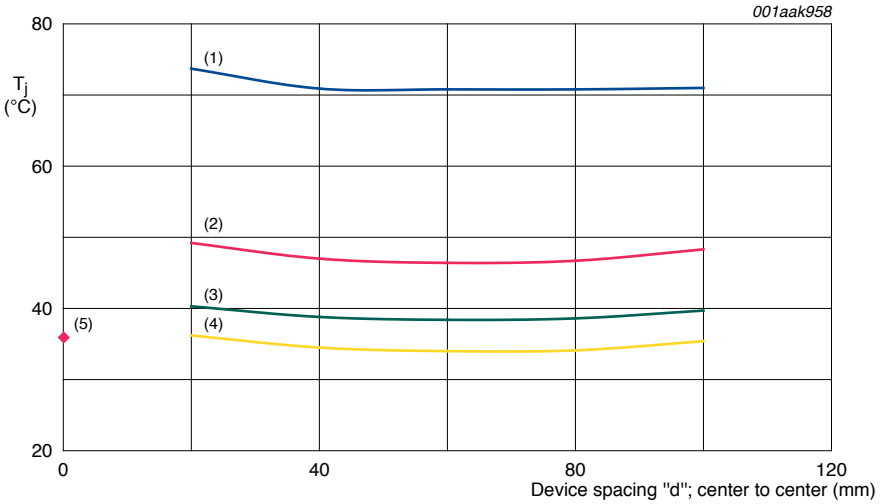
(2) Layer 2 (ground).

(3) Layer 3 (signal).

(4) Layer 4 (power and signal).

Fig 19. Modified 4-layer stack-up (not to scale)

The stack-up of **Figure 19** shows the ground plane on layer 2 with the device drain connected to areas on both layer 1 and layer 4, and with the layer 4 copper now also a square of dimensions 15 mm x 15 mm. Layer 3 remains a signal layer. Both MOSFETs are configured in this way, and once again we investigate the influence of separation distance "d" on device T_j. The results are shown in **Figure 20**, together with those for the previous analyses.



(1) Layer 1 only.

(2) 2-layer.

(3) 4-layer.

(4) 4-layer with vias, separate drains.

(5) Half-bridge configuration.

Fig 20. Simulation results for two devices of varying separation "d" on a 4-layer PCB with vias

Clearly the addition of vias under the devices results in a further decrease in T_j even though the layer 4 copper area is reduced. Once again we see that T_j has little dependence on device spacing.

Also shown in **Figure 20** is the result for the two devices positioned in a "half-bridge configuration". This refers to the circuit topology of see **Figure 18**(b), where it makes sense from an electrical point of view to position the devices one above the other rather than side by side. In this way, the source connection of Q1 is physically close to the drain connection of Q2 and connection between the two would be by a short, low inductance path. See **Figure 21**.

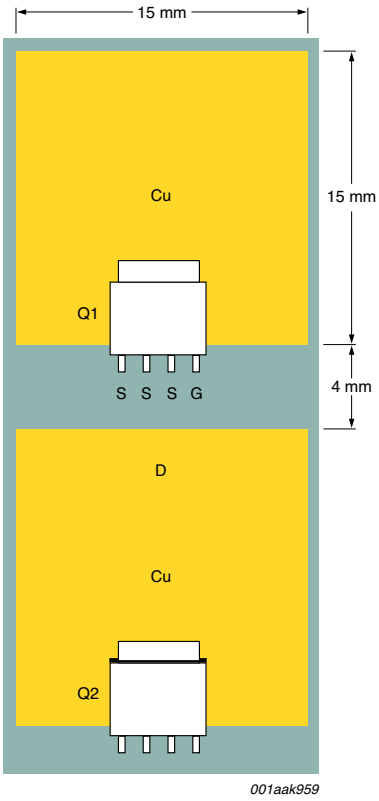
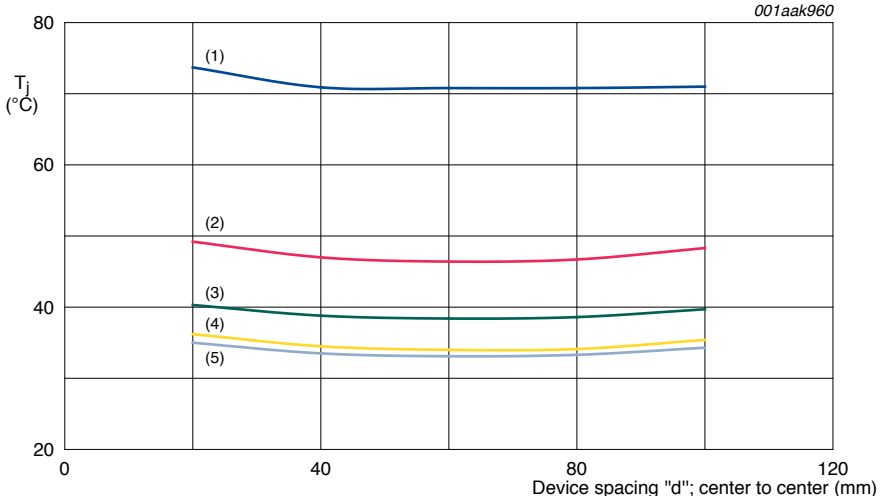


Fig 21. Two devices logically positioned for a half-bridge configuration

4.4.5 Analysis 8: A 4-layer PCB with thermal vias part 2

The second analysis will consider two devices sharing a common drain connection. This would correspond to the topology of **Figure 18**(a) with a common V_{BAT} line. The V_{BAT} line is represented by a plane measuring 25 mm x 120 mm on layer 4, with vias as per the previous analysis. Results are shown in **Figure 22**.



(1) Layer 1 only.

(2) 2-layer.

(3) 4-layer.

(4) 4-layer with vias, separate drains.

(5) 4-layer with vias and common V_{BAT} plane.

Fig 22. Simulation results for two devices of varying separation “d” on a 4-layer PCB with vias and common V_{BAT} plane

The improvement in thermal performance is practically negligible compared to the previous example (**Section 4.4.4**) with independent drain copper areas.

4.4.6 Summary: factors affecting the thermal performance of two devices

To reiterate, the following results were obtained with layer 1 copper side lengths of 15 mm.

- For two devices mounted on a single-layer PCB, device T_j is largely independent of device spacing "d". A significant increase in T_j vias only observed when the devices are mounted very close together. There is also little difference compared to the single device case (see **Figure 15**). Device T_j is approximately 71 °C
- Adding a second copper layer (layer 4) reduces T_j by roughly 20 °C to 25 °C compared to the single-layer case. Some minor dependence of T_j on "d" is apparent, with slightly higher T_j occurring when the devices are mounted closest together or at the PCB edges (see **Figure 16**)
- Moving to a 4-layer PCB stack-up yields a further reduction in T_j of ~9 °C compared to the 2-layer design (see **Figure 17**)
- Adding a 4 x 4 pattern of vias under the devices provides a further small improvement in thermal performance, whereby T_j is reduced by an additional ~4 °C (see pcb)
- Making the device layer 4 copper areas common, rather than separate, has almost no effect on device T_j (see **Figure 22**)

4.5 Four LFPAK devices

In this final section the number of devices will be increased to four. We will adopt the same PCB size as for the analyses in **Section 4.4** on page 103, and a similar approach in building up the PCB stack-up from a simple structure to one which is more complex. As before, in order to restrict the number of variables to a sensible limit we will consider only the 15 mm side-length area for layer 1. This section will mainly concentrate on the four devices equally spaced apart in a single line (see **Figure 23**), but will also consider two of the "half bridge" configurations described in **Section 4.4.3** on page 107.

The PCB top copper configuration is shown in **Figure 23**.

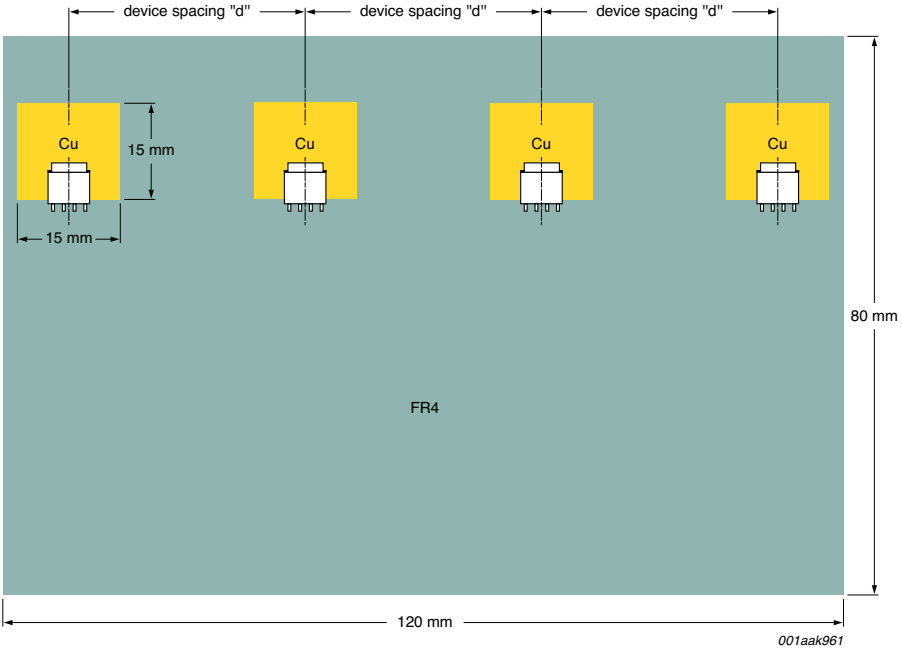
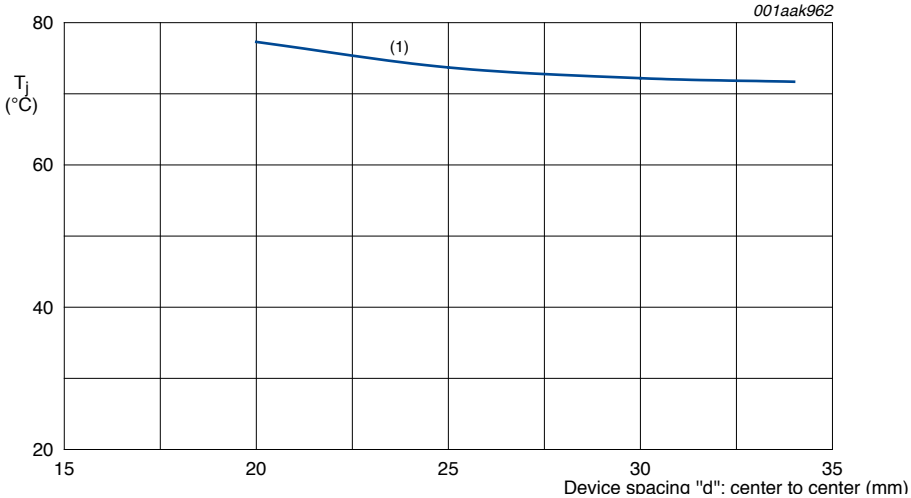


Fig 23. Four devices: PCB top copper configuration

Simulation were carried out to investigate the influence of "d" on device T_j for the various PCB stack-ups. Values of d varied from 34 mm (maximum separation, as shown in **Figure 23**) to 20 mm where there was only a 5 mm gap between the device layer 1 copper areas.

4.5.1 Analysis 9: A single-layer PCB

The results for the single-layer simulations are shown in **Figure 24**. Unlike the analyses of two devices in the previous section, the thermal environment is not exactly the same for all four devices in this configuration. The two inner devices are at a slight disadvantage as they have additional heat sources on both their left- and right-hand sides, whilst the outer devices have a heat source on one side only. In the worst case, this results in a difference in T_j value of approximately 3 °C between inner and outer devices. In the interests of presenting a conservative set of results, the graphs which follow show the temperatures for the inner, slightly hotter, devices.



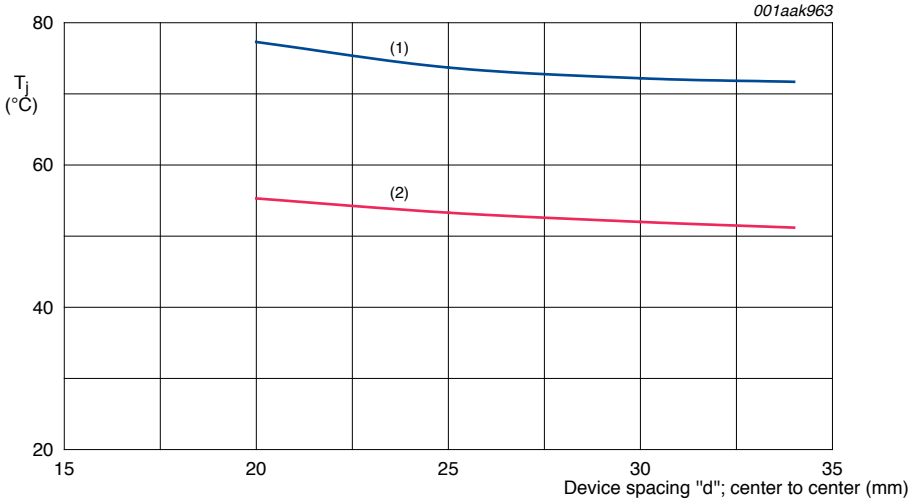
(1) Layer 1 only.

Fig 24. Simulation results for four devices of varying separation “d” on a single-layer PCB

Again, we see the law of diminishing returns exhibited in these results: as the spacing between devices increases, so the curves flattens out. Therefore, increasing the centre – center spacing beyond approximately 30 mm would have little influence on device temperatures.

4.5.2 Analysis 10: A 2-layer PCB

For the purposes of this exercise we will again consider the same variations in device spacing as for analysis 9. However for analysis 10 we will add the layer 4 (bottom copper) layer covering the whole of the underside of the PCB and thereby creating a 2-layer stack-up. In practical terms this layer might be a ground or power plane, although it remains unconnected to the devices. The results are shown in the graph of **Figure 25** together with those from analysis 9 for comparison purposes.



(1) Layer 1 only.

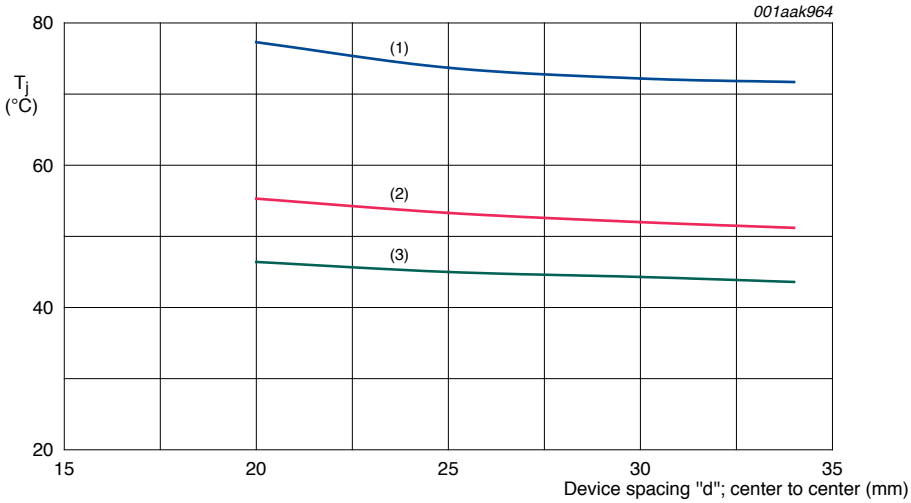
(2) 2-layer.

Fig 25. Simulation results for four devices of varying separation “d” on a 2-layer PCB

Adding the second copper layer increases the thermal conductivity of the PCB and reduces device temperatures by approximately 20 °C. This is exactly the result we would expect and is in keeping with the results for the one and two-device configurations.

4.5.3 Analysis 11: A generalized 4-layer PCB

The 2-layer stack-up of analysis 10 will now be increased to 4 layers with the addition of two internal signal layers. The signal layers are assumed to be composed of numerous thin signal tracks, and simulation of the internal layers will again be by the “percentage coverage” method, 50 % copper coverage and 1 oz./ft^2 (35 µm) thickness. Layer 4 remains a solid unconnected plane covering the entire underside area. See **Figure 8**. Junction temperatures were determined for various separation distances d and the results are shown in **Figure 26**.



(1) Layer 1 only.

(2) 2-layer.

(3) 4-layer.

Fig 26. Simulation results for four devices of varying separation “d” on a 4-layer PCB

Adding the internal signal layers has resulted in an overall reduction in T_j of approximately 8 °C.

4.5.4 Analysis 12: A 4-layer PCB with thermal vias part 1

In analysis 12 we will consider cases where the layer 1 copper areas (connected to MOSFET drains) are connected to 15 mm x 15 mm copper areas on layer 4 by thermal/electrical vias of the 5 x 4 pattern described in **Section 4.3.5** on page 99. The corresponding circuit topologies are as shown in **Figure 18**, but for twice the number of devices. We could therefore have four high-side load switches connected to four different V_{BAT} lines (**Figure 18**(a)). Alternatively we could have two of the half-bridge topologies shown in **Figure 18**(b). For either possibility, each MOSFET’s drain connections are independent, and layer 2 in the PCB stack-up is a full-coverage ground plane (see **Figure 19**).

For the four high-side load switches we will vary the spacing between devices as in analyses 9 to 11. In the case of the two half-bridges, however, we can consider each half-bridge as a single “unit”, and examine the effect of varying the spacing between half-bridge units. See **Figure 27**). The results are shown in **Figure 28**.

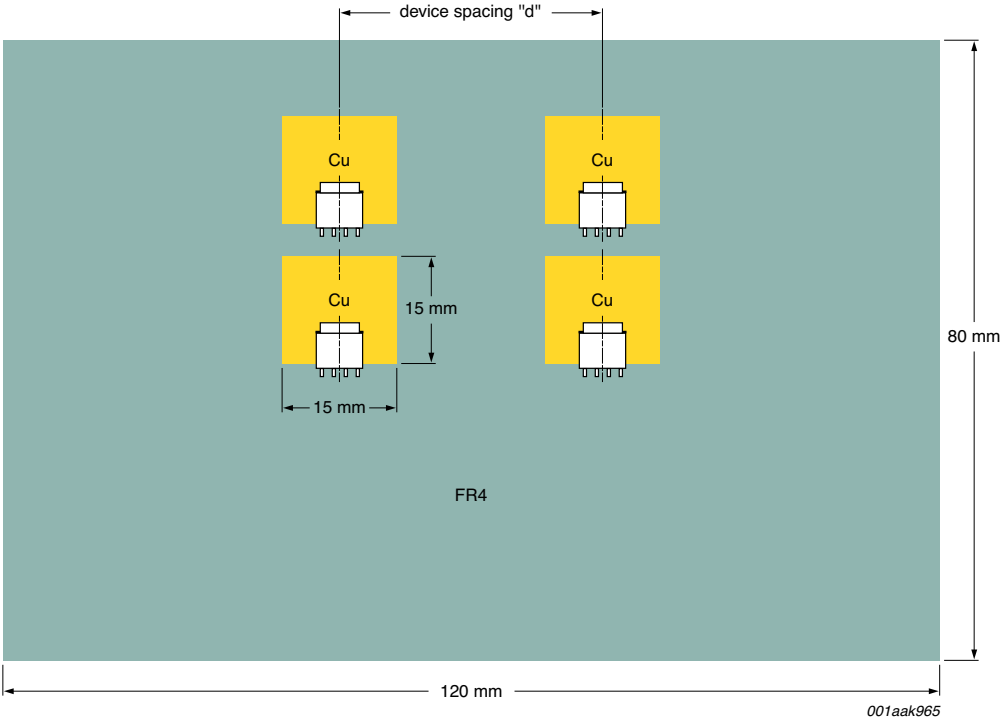
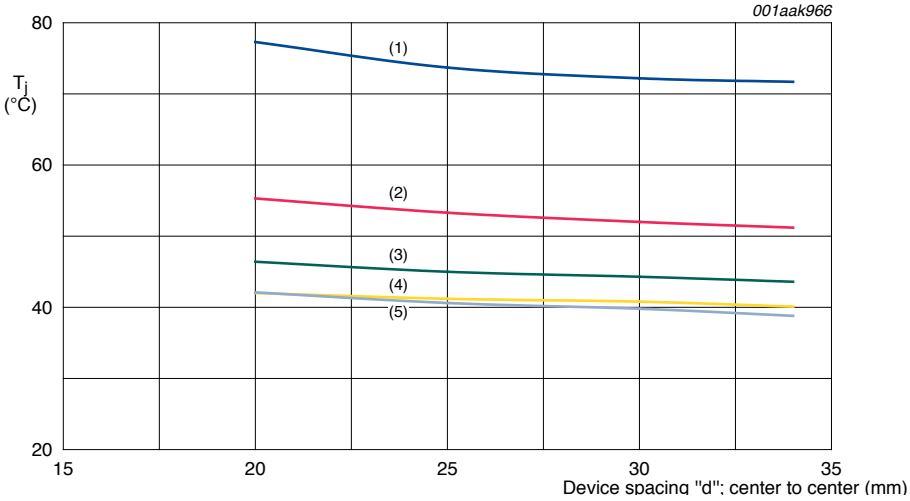


Fig 27. Four devices positioned as two half-bridges configurations



(1) Layer 1 only.

(2) 2-layer.

(3) 4-layer.

(4) 4-layer with vias, half-bridge configuration.

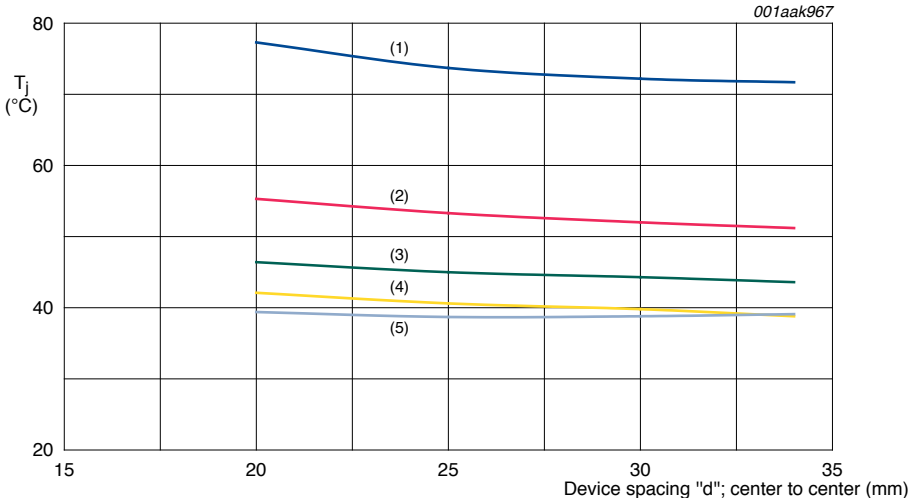
(5) 4-layer with vias, separate drains.

Fig 28. Simulation results for four devices of varying separation “d” on a 4-layer PCB with vias

Adding vias under the devices results in an overall reduction in T_j of approximately 4 °C to 5 °C for both topologies.

4.5.5 Analysis 12: A 4-layer PCB with thermal vias part 2

The final analysis will consider four devices sharing a common drain connection. This would correspond to the topology of **Figure 18**(a) with a common V_{BAT} line. The V_{BAT} line is represented by a plane measuring 25 mm x 120 mm on layer 4, and stack-up is as **Figure 19**. The results are shown in **Figure 29**.



(1) Layer 1 only.

(2) 2-layer.

(3) 4-layer.

(4) 4-layer with vias, separate drains.

(5) 4-layer with vias and common V_{BAT} plane.

Fig 29. Simulation results for four devices of varying separation “d” on a 4-layer PCB with vias and common V_{BAT} plane

Connecting the four devices does make a small difference to T_j when the devices are close together, however as “d” increases the effect tends to diminish.

4.5.6 Summary; factors affecting the thermal performance of four devices

For layer 1 copper side lengths of 15 mm.

- For four devices mounted on a single-layer PCB, device T_j is somewhat independent of device spacing "d". The inner two devices tend to run slightly hotter, by approximately 3 °C in the worst case. Device T_j is approximately 72 °C (see **Figure 24**)
- Adding a second copper layer (layer 4) reduces T_j by roughly 20 °C compared to the single-layer case (see **Figure 25**)
- Moving to a 4-layer PCB stack-up yields a further reduction in T_j of ~8 °C compared to the 2-layer design (see **Figure 26**)
- Adding a 4 x 4 pattern of vias under the devices provides a further small improvement in thermal performance, whereby T_j is reduced by an additional ~4 °C (see **Figure 28**)
- Making the device layer 4 copper areas common, rather than separate, has little effect on device (see **Figure 29**)

4.6 Summary

Increasingly there is a need to pay attention to the thermal aspects of PCB design, in order that safe operating temperatures are not exceeded. For designs employing surface-mount power MOSFETs, which use the PCB as their primary method of heatsinking, it is important that both MOSFET junction temperature (T_j) and PCB temperature (T_{PCB}) are kept within safe limits. Typically the maximum permissible T_j figure is 175 °C whilst the maximum T_{PCB} figure may be 120 °C. As there is close thermal coupling between the MOSFET device and the PCB to which it is soldered we can say that $T_{PCB} \approx T_j$ and so the operating temperature upper limit is that of the PCB (120 °C) rather than the MOSFET junction.

The PCB designer may be faced with a lack of useful resources when attempting to lay out a PCB for "safe" thermal operation. At one extreme, the MOSFET data sheet R_{th} figures are too vague to be of use and will probably have been measured under conditions which differ greatly from those of his target application. At the other extreme, a detailed analysis of the thermal performance of a design may be carried out using simulation software and/or actual prototype build. Simulation software can give excellent results in a relatively short space of time, but is generally expensive and its use has a steep learning curve.

Prototype build, on the other hand, will almost certainly be required at some stage in the product development, for design verification, but is an expensive and time-consuming option in the early stages of the design cycle. There is therefore a need for thermal design guidelines, which bridge the gulf between the less-than-helpful R_{th} figures at one extreme and full prototype simulation or build at the other, and which may be employed at an early stage in the PCB design in order to steer the designer in the right direction. The purpose of this chapter is to provide those guidelines for designs employing the NXP Semiconductors range of LFPAK MOSFETs

This design guide has considered the thermal performance of a variety of different PCB configurations and stack-ups for one, two and four MOSFET devices. Factors which have been considered include; PCB layer stack-up, the influence of common circuit topologies on PCB layout, PCB copper area, the influence of thermal “vias”, device placement and spacing and the implications of multiple dissipating devices on a single PCB. This document cannot hope to address all the myriad possible device usages, however it is hoped that the chosen range of different configurations is representative of typical “real life” device usage.

Finally, we should reiterate again that the information contained within this design guide is presented as a starting point only. Any new design should of course be prototyped and its thermal behavior characterized before placing the design into production.

Chapter 5: LFPAK MOSFET thermal design - part 2

Chapter 5: LFPAK MOSFET thermal design - part 2

5.1 Introduction

In the previous chapter the impact of various different PCB and device configurations on thermal behavior was considered. By analyzing and comparing multiple scenarios, it was possible to draw numerous conclusions regarding the optimum way to provide heatsink cooling of LFPAK MOSFETs.

All of the PCB configurations considered in chapter 4 had one thing in common - they were situated in free air at an ambient temperature of 20 °C. No enclosures or housing were included in the scenarios. In most real-life applications, however, it is likely that we would not have an exposed PCB with no enclosure present. The need to protect the PCB from environmental factors, plus possible considerations for ElectroMagnetic Compatibility (EMC) would almost certainly dictate that the PCB would be mounted in an enclosure of some form. Inevitably the enclosure would interfere with the free flow of air around the PCB, and so would also have an impact on the thermal performance of the system.

In this chapter we will take a close look at how the construction and configuration of an enclosure can have an impact on the operating temperatures of the power MOSFET devices within. Factors which will be examined include:

- Enclosure material and surface finish
- Internal spacing above, below and around the PCB
- Bottom-side cooling of the PCB (i.e. PCB bottom surface in contact with an internal surface of the enclosure)
- Top-side cooling of the MOSFET devices (top of the device packages in contact with an internal surface of the enclosure)
- The role of encapsulation within the enclosure, where the air gap around the PCB is partially or completely filled with an encapsulation compound
- Proximity of the “module” to a bulkhead

In order to rationalize the number of possible variables, we will consider only one PCB configuration, taken from chapter 4. The enclosure plus PCB will be referred to hereafter as the “module”.

As with chapter 4, the thermal analyses presented in this chapter have been carried out using thermal simulation software. The simulations use MOSFET models which have been validated against empirical data and are known to accurately model the thermal behavior of real-life devices.

The thermal simulation software used to carry out the analyses is the Mentor Graphics (Flomerics) “FloTHERM” package. The device models used in the analysis are available for free download from the NXP web site, together with a selection of the scenarios used in the preparation of this book.

5.2 The module model

5.2.1 PCB characteristics

In the interests of minimizing the number of possible variables, we will consider only one PCB configuration, taken from **Section 4.5.4** of this book. The PCB is shown in **Figure 1**.

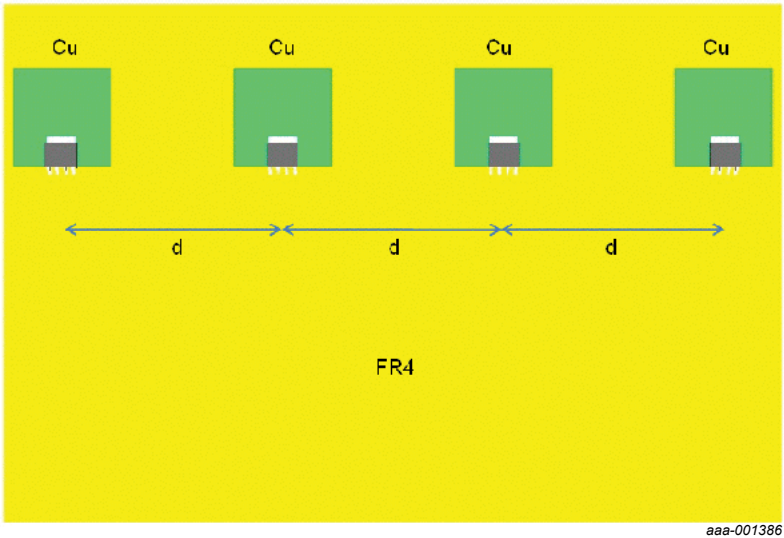


Fig 1. The PCB model

The main PCB characteristics are:

- Overall PCB size 80 mm x 120 mm, thickness 1.6 mm
- Standard FR4 PCB material
- All copper layers 1 oz/35 µm thickness
- Top copper - 15 mm x 15 mm area per device, attached to the device tab (as shown)
- Bottom copper - also 15 mm x 15 mm area per device, connected to the top copper by vias
- Internal layers - average 50 % area coverage
- Vias - under each device a pattern of 5 x 4 vias of 0.8 mm internal diameter
- Device spacing d = 25 mm
- Power dissipation is 0.5 W per device

Chapter 4 indicated that the placement of the individual MOSFETs actually had very little influence on their operating temperatures - varying by only around ±1 °C.

5.2.2 Enclosure characteristics

Several enclosure characteristics will be varied throughout the course of this chapter.

However, some general features will remain the same throughout:

- The enclosure is completely sealed with no holes or cutouts.
- The walls of the enclosure are 2 mm thick, irrespective of enclosure material.
- The enclosure is able to lose heat energy to the outside environment by the mechanisms of convection, conduction and radiation.

There are potentially many different enclosure materials which could be considered in this Design Guide. To keep the number of variables to a manageable level, while also providing a usefully realistic analysis of typical materials, we will restrict ourselves to the following three variations as shown in **Table 1**.

Table 1. Enclosure materials and their properties summarized

Material	Thermal conductivity (W/m.K)	Surface emissivity
Black plastic	0.2	0.95
Polished aluminium	201	0.04
Anodized (black) aluminium	201	0.8

Surface emissivities apply to both inner and outer surfaces of the enclosure.

An example module is shown in **Figure 2**. Note that the enclosure top and one side have been made transparent so that the position of the PCB can be seen.

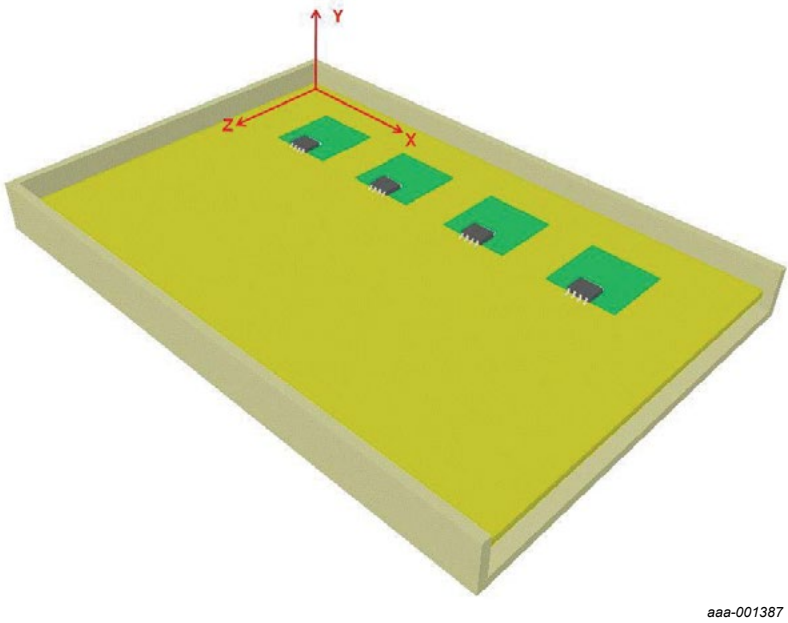


Fig 2. An example module

5.2.3 Axes naming convention

Throughout this chapter we will consider the effects of moving or resizing objects in the three spatial directions. We therefore need a convention for referring to these directions, as shown by the arrows in **Figure 2**.

So for example, when we are increasing the gap between the PCB and enclosure at the short edges of the PCB (the x-direction), this will be referred to as the "x-gap". Similarly, the gaps above and below the PCB will be referred to as being in the "y-gap", and so on.

5.2.4 The ambient environment

The module is situated in an environment with the following characteristics:

- The module is surrounded by free air at an ambient temperature of 20 °C
- There is no applied airflow, although the module is able to create airflow by the process of natural convection from its outer surfaces
- The environment is free to exchange heat energy with the module by the processes of convection, conduction and radiation

5.2.5 Potential heat paths

There are numerous possible paths along which the heat may travel from the PCB. These paths utilize the three heat transfer mechanisms of conduction, convection and radiation and are illustrated in **Figure 3**.

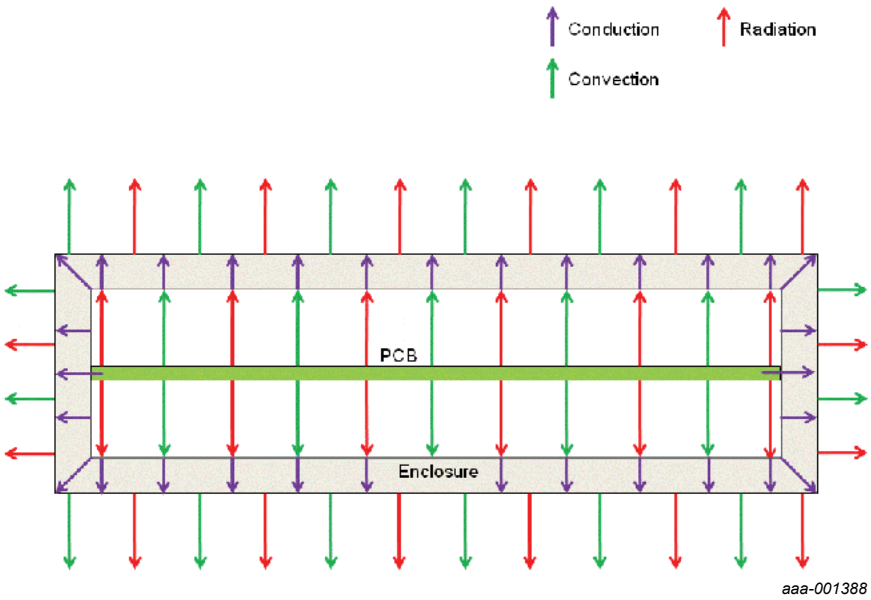


Fig 3. Potential heat paths

5.3 The influence of y-gap on T_j

5.3.1 Black plastic enclosure; x- and z-gaps = zero

In the first analysis, we will reduce the variables to the smallest number possible. The x-and z-gaps around the board will be set to zero, so the edges of the PCB will actually be in contact with the internal walls of the enclosure, and we will consider only the black plastic enclosure material. The y-gap above and below the PCB will be varied, as illustrated in **Figure 4**.

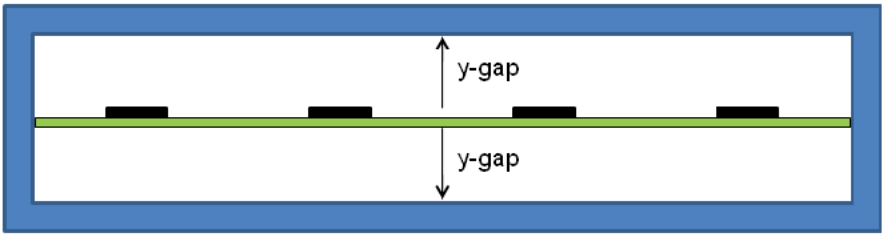
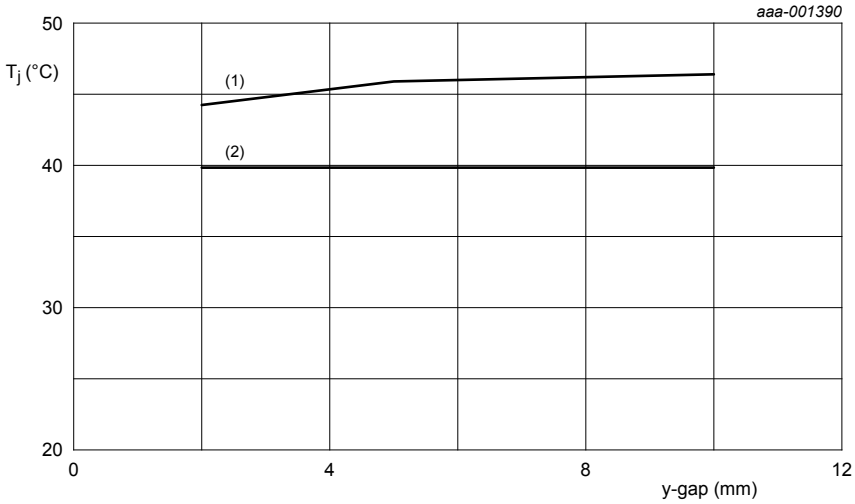


Fig 4. Varying the y-gap above and below the PCB

We will run the model for y-gap values of 2 mm, 5 mm and 10 mm and observe what happens to the device T_j. The results are shown in the graph of **Figure 5**, together with the temperature observed with no enclosure present. Temperatures shown are the average for the four devices.



(1) T_j (black plastic enclosure).

(2) T_j (no enclosure).

Fig 5. The variation of T_j with y-gap

The graph of **Figure 5** has some interesting features:

- Surrounding the PCB with an enclosure has resulted in an elevated T_j compared to the case where no enclosure was present
- As the y-gap increases, so T_j also increases slightly

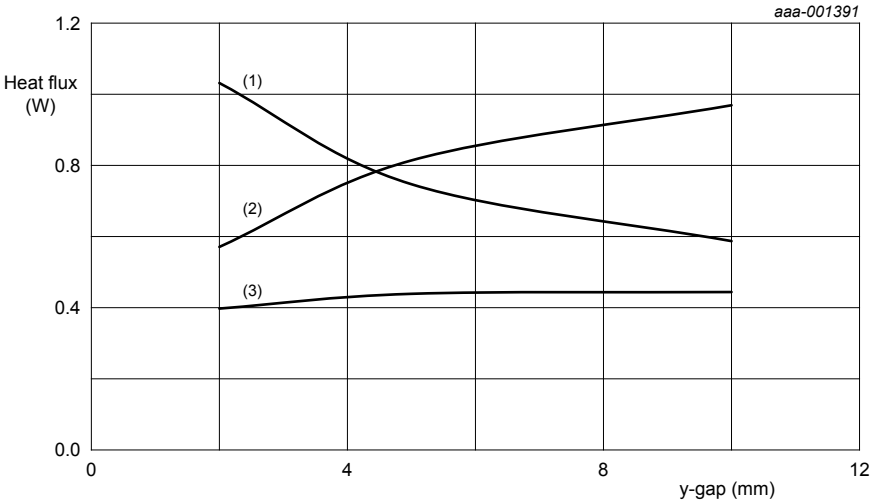
The first of these observations is in keeping with the expectation expressed in the Introduction, as the enclosure tends to interfere with heat loss by natural convection from the surfaces of the PCB and devices. It is therefore reasonable to expect T_j to rise with the enclosure in place.

The second observation is a more counter-intuitive result! Surely as we add more air gap around the PCB, the cooling of the PCB should become more effective? In order to answer this question, we need to consider the various potential heat paths present within the module (**Figure 3**).

Altering the y-gap should increase the volume of air available to circulate around the PCB surfaces, even though the air cannot escape, and hence provide for better cooling. However, this is not the effect which we see. The reason is that air will only circulate under natural convection if there is sufficient room for it do so. The air experiences "drag" forces where it contacts solid surfaces, and if these forces are sufficiently dominant (because the volume is small) then natural convection cannot occur. The air is stationary and is said to be "stagnant"[1]. The simulations suggest this is exactly what is happening in this case, even when the y-gap is 10 mm, with reported air velocities within the enclosure being effectively zero. The end result is that the natural convection heat loss mechanism does not occur within the enclosure and instead we have only conduction heat loss through the air, whose conductivity is very low (typically 0.003 W/m.K for air at 20 ^{o}C).

FloTHERM allows us to examine the magnitude of the heat transfer mechanisms in a scenario, and applying this analysis to the scenario results in the graph of **Figure 6**.

1. This is also the reason why, for instance, the air gap in double glazing is such an effective insulator. For a more detailed explanation of this phenomenon, the reader is encouraged to research the terms "Nusselt number" and "Rayleigh number".



(1) Conduction (through air).

(2) Radiation.

(3) Conduction (through solids).

Fig 6. Variation in heat loss mechanisms with y-gap

In **Figure 6** we can see that conduction through the air does indeed decrease as the y-gap increases, while conduction from the edge of the PCB to the enclosure walls remains much more constant. At the same time, radiation loss from the PCB increases as the y-gap increases - why should this be?

Radiation heat exchange occurs between the PCB and inside walls of the enclosure. All the surfaces involved are radiating heat energy, but as the PCB is at a higher temperature than the enclosure walls, the net effect is the transfer of heat from the PCB to the enclosure. The amount of heat energy exchanged depends on several factors, including:

- The temperatures of the surfaces
- The emissivities of the surfaces (related to surface color, finish, etc.)
- The "view factor" existing between the surfaces

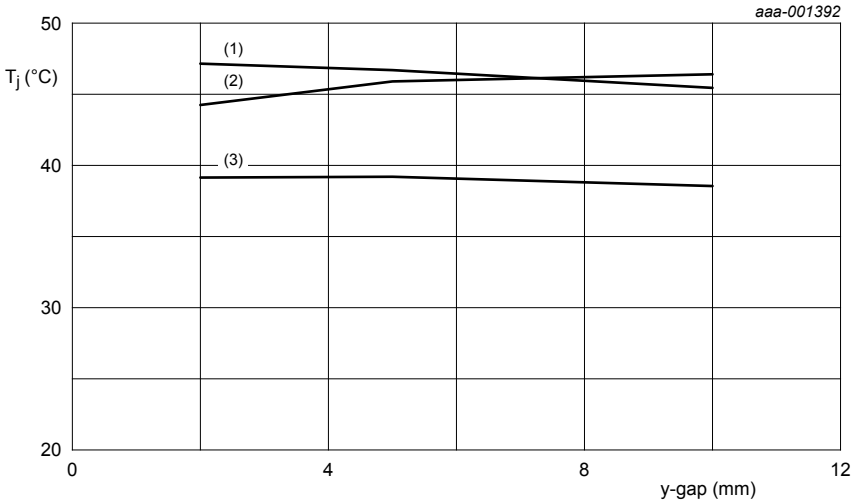
The "view factor" is a measure of how much of the receiving surface can be "seen" by the transmitting surface. In this case, as we increase the y-gap we also increase the surface area of the inside of the enclosure, and hence more area is made available to receive heat energy from the PCB by the process of radiation. Hence, in **Figure 6**, as the y-gap increases so the heat loss by radiation increases. Note also that for any value of y-gap, the total heat loss by the three mechanisms must always add up to the total dissipated within the enclosure, which is 4 x 0.5 W = 2 W in this case.

5.3.2 Two more enclosure materials

So far we have only considered the flow of heat within the enclosure. Of course, as illustrated in **Figure 3**, there are other heat paths through the enclosure walls and from the enclosure outer surfaces which will also have an impact on the overall module thermal performance. The nature of the heat flow will depend very much on the thermal properties of the enclosure material:

- Conduction through the enclosure walls, which will be influenced by the conductivity of the enclosure material.
- Radiation heat loss from the enclosure's outer surface, which will be influenced by the emissivity of the module surface.

In addition, the module dimensions (which vary as we vary the y-gap) will also determine the nature of heat flow within the enclosure, as we have already seen, plus heat loss through the enclosure walls and from the module outer surface both by convection and radiation. Clearly these factors are interlinked, and do not lend themselves to a simple, manual analysis. We have therefore re-run the simulations with the two new enclosure materials, and the results are shown in **Figure 7**.



(1) T_j (polished aluminium).

(2) T_j (black plastic).

(3) T_j (anodized aluminium).

Fig 7. Variation in T_j with y-gap for the three enclosure materials

We can summarize the properties of the three materials in a simple way, as shown in **Table 2**.

Table 2. A simple summary of the material properties

Material	Heat transfer by radiation	Heat transfer by conduction
Black plastic	good	bad
Polished aluminium	bad	good
Anodized aluminium	good	good

The black plastic and polished aluminium materials are both good in one respect and less good in another. Hence the temperatures for these two materials tend to be higher, although the property variations do not exactly cancel out. On the other hand, the anodized aluminium material has “the best of both worlds”, being both a good conductor and good for radiation exchange, so the temperature results for this material are lower.

5.3.3 Summary: the influence of y-gap on T_j

The following list is a summary of observations from this section:

1. The presence of the enclosure can cause an increase in device temperatures compared to the case where no enclosure is present - this was seen for the black plastic and polished aluminium materials.
2. However, an enclosure made from anodized aluminium was found to reduce device temperatures slightly.
3. Air inside the enclosure is “stagnant” and so the process of natural convection cannot occur.
4. The heat loss mechanisms inside the enclosure are therefore:
   a. conduction through the stagnant air
   b. direct conduction from the PCB edges to the enclosure
   c. radiation
5. Radiation heat exchange depends on the “view factor” between radiating surfaces and tends to increase as the enclosure internal dimensions increase.
6. The enclosure material influences overall module thermal performance. In particular, the material thermal conductivity and surface emissivity.
7. Of the three materials considered, anodized aluminium has the best combination of thermal conductivity and surface emissivity.

5.4 Adding x- and z-gaps around the PCB

So far, all the cases we have considered have had physical contact between the edges of the PCB and the enclosure walls. Although the area of contact was small, the graph of **Figure 6** has shown that the amount of heat transferred through this path is significant, amounting to approximately 20 % of the total in the case of the black plastic enclosure.

It is probable, though, that some real-life configurations may have an air gap between the PCB edges and enclosure walls - perhaps to provide electrical isolation or for other mechanical reasons. Introducing such an air gap would alter the available heat paths within the module, and inevitably have an effect on the temperatures of the MOSFET devices mounted on the PCB.

To investigate the effect of the air gap around the PCB, the previous models were re-run, but this time with x- and z-gaps of 5 mm and 10 mm. See **Figure 8**.

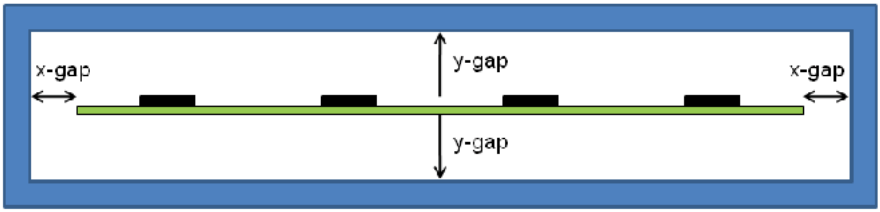
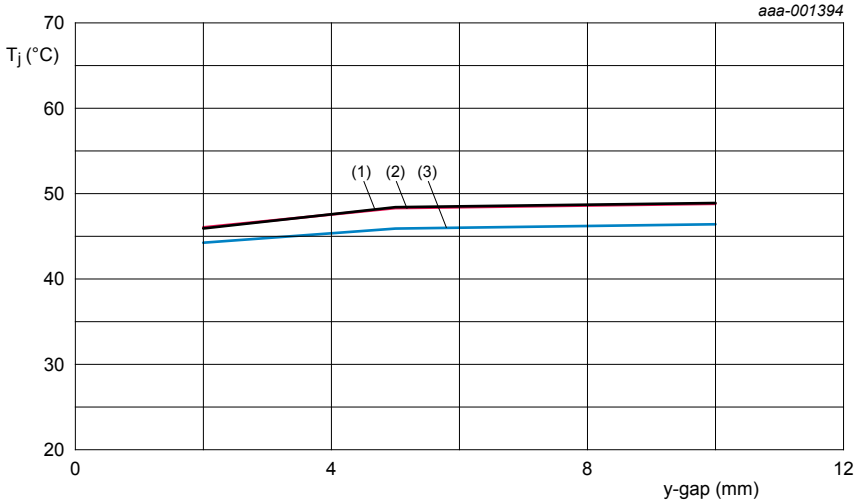


Fig 8. Gaps added around the PCB

5.4.1 The black plastic enclosure

The results for the black plastic enclosure are shown in **Figure 9**.



(1) T_j black plastic (5 mm gap).

(2) T_j black plastic (10 mm gap).

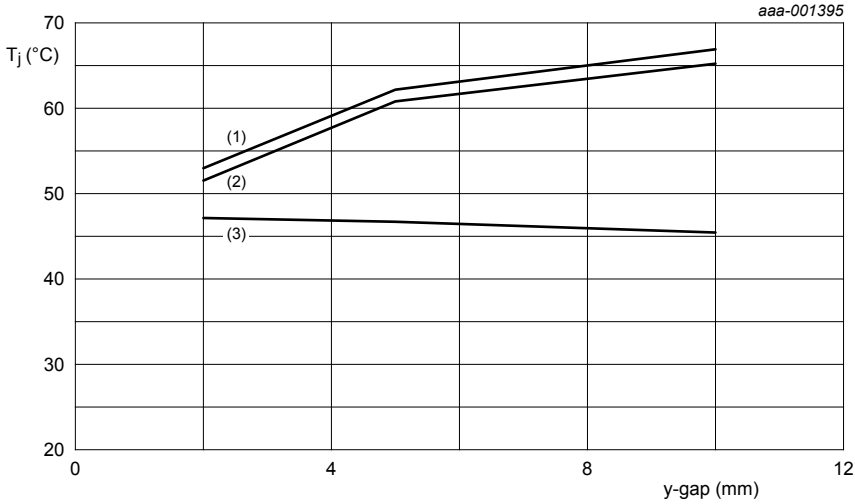
(3) T_j black plastic (no gap).

Fig 9. The effect of x- and z-gaps on T_j for the black plastic enclosure

Although we can see some difference when the gap is introduced, it could be argued that the effect is not dramatic - around 2.5 °C. This is because the plastic material is not a good conductor of heat energy, and so conduction into the enclosure is not a dominant heat path (see **Figure 6**). In addition, the increased view factor results in an improved transfer of heat by radiation. Hence removing the conduction heat path does not result in a dramatic change in temperatures.

5.4.2 The polished aluminium enclosure

We would expect to see a more significant effect for the aluminium enclosures, as aluminium is a better conductor of heat than plastic, and so removing this conduction path should have more effect on T_j. The results for the polished aluminium enclosure are shown in **Figure 10**.



(1) T_j polished aluminium (5 mm gap).

(2) T_j polished aluminium (10 mm gap).

(3) T_j polished aluminium (no gap).

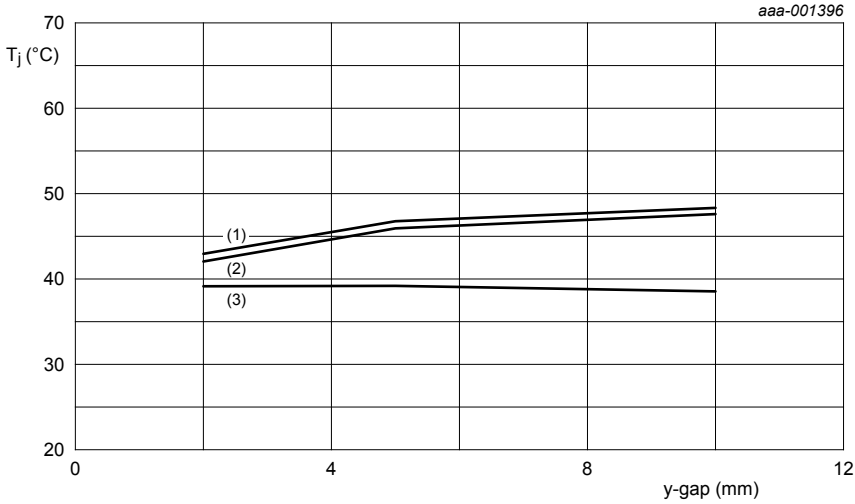
Fig 10. The effect of x- and z-gaps on T_j for the polished aluminium enclosure

The effect of adding the x- and z-gaps around the PCB is much more noticeable in this case, especially as the y-gap increases, resulting in a difference of ~20 °C when the y-gap is 10 mm. By removing the conduction path from the PCB edges we have increased the thermal isolation between the PCB and enclosure:

- Direct conduction between the PCB and enclosure is eliminated.
- Heat flow through the air remains poor as the air is still stagnant.
- Radiation heat exchange is also poor as the surface emissivity of the aluminium is very low.

5.4.3 The anodized aluminium enclosure

For the anodized aluminium enclosure, the effect of adding the x- and z-gaps is less pronounced. See **Figure 11**.



(1) T_j anodized aluminium (5 mm gap).

(2) T_j anodized aluminium (10 mm gap).

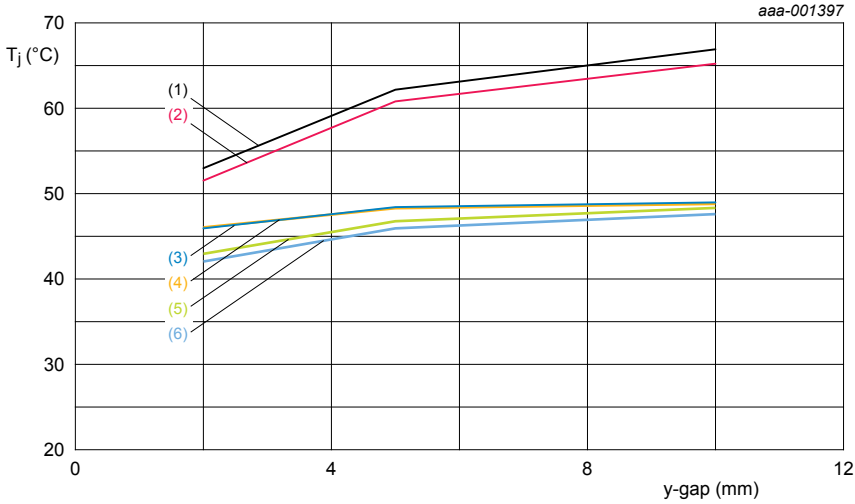
(3) T_j anodized aluminium (no gap).

Fig 11. The effect of x- and z-gaps on T_j for the anodized aluminium enclosure

Although in this case we have lost the direct conduction heat path within the module, the radiation heat path is still quite effective, owing to the surface finish of the enclosure material. Hence the variation in T_j is not as great as for the polished aluminium material.

5.4.4 The three enclosures side-by-side

The results for all three enclosure types are shown on the single graph of **Figure 12**. This graph enables us to compare the influence of the three material types when there is no direct conduction between the PCB and enclosure.



(1) T_j polished aluminium (5 mm gap).

(2) T_j polished aluminium (10 mm gap).

(3) T_j black plastic (5 mm gap).

(4) T_j black plastic (10 mm gap).

(5) T_j anodized aluminium (5 mm gap).

(6) T_j anodized aluminium (10 mm gap).

Fig 12. The effect of x- and z-gaps on T_j for the three enclosure materials

It should be remembered that the surface finish of the enclosure also influences how its outer surfaces will lose heat energy to the environment by the process of radiation. So for instance, the polished aluminium material will not only have poor radiation heat transfer between its inner surfaces and the PCB, but also between its outer surfaces and the local environment.

5.4.5 Summary: adding x- and z-gaps around the PCB

- Adding a gap between the PCB and enclosure removes the direct conduction heat path between these items
- For the black plastic enclosure, the effect on T_j of the air gap is not dramatic as plastic is a poor conductor of heat anyway, and radiation exchange between the surfaces is good
- For the polished aluminium enclosure with larger y-gap, the effect is more dramatic as aluminium is a good thermal conductor and radiation exchange is poor
- The change in temperatures for the anodized aluminium material lies somewhere between the previous two sets of results. This is because, although aluminium has good thermal conductivity, the surface properties of anodized aluminium allow for good heat exchange by radiation
- Viewed side-by-side, the temperatures observed for the anodized aluminium and black plastic materials are quite similar, while the polished aluminium results are higher - especially for the larger y-gap
- Enclosure thermal conductivity and emissivity also influence the heat paths through the enclosure and from the enclosure outer surface to ambient

5.5 Encapsulating the PCB

So far we have only considered cases where the PCB has been surrounded by air within the enclosure. However, it is sometimes the case that the interior of the enclosure may be partially or completely filled with an encapsulation (or “potting”) compound. This is generally done to provide the PCB with additional protection from dirt and moisture, as well as improving the mechanical reliability of the module as a whole.

Clearly, if we fill some or all of the enclosure with a solid material then we will alter the thermal behavior of the module. Even without carrying out any detailed analysis, it seems likely that the following aspects will be affected:

- Assuming that the encapsulant is opaque, some or all of the radiation paths will be eliminated
- Some or all of the conduction paths through the air within the enclosure will be improved, provided the encapsulant has a higher thermal conductivity than stagnant air

In the following analyses, we will examine the influence of a typical encapsulant with thermal conductivity of 0.55 W/m.K. For comparison purposes, the thermal conductivity of still air is around 0.003 W/m.K, so although the thermal conductivity of the encapsulant is not very high in absolute terms, it is considerably higher than the air which it may replace. We will consider two methods of encapsulation - one where the level of encapsulant just reaches the top surface of the PCB and one where the whole space within the enclosure is filled with encapsulant. See **Figure 13**.

We will only examine configurations where the x- and z-gaps are 5 mm. In other words, where the PCB edge is separated from the enclosure walls by a gap of 5 mm. The rationale for this is as follows:

- The need to keep the number of variables to a manageable level
- The likelihood that, in a real design, there would be a need to provide an electrical insulation gap between the PCB and enclosure, when an aluminium enclosure is utilized
- The further probability that, in the x- and z-directions, the PCB would be the largest single item in the module, and hence the enclosure would probably not be much larger than the PCB in these directions

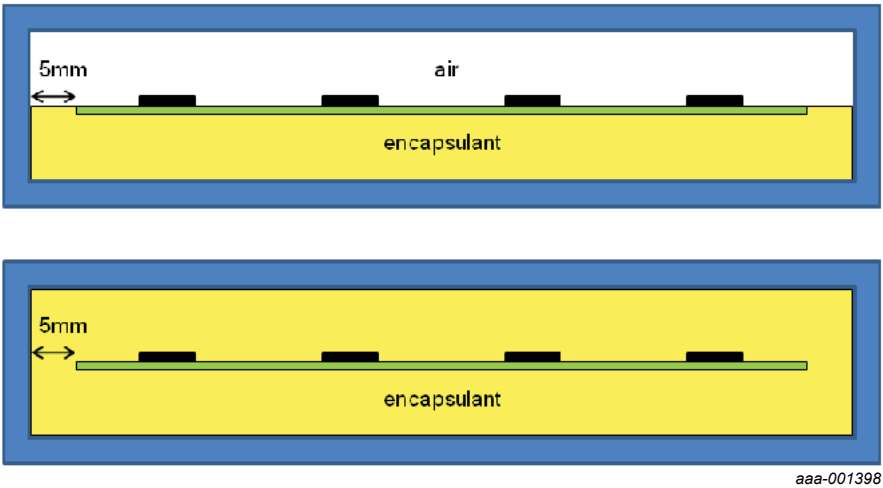
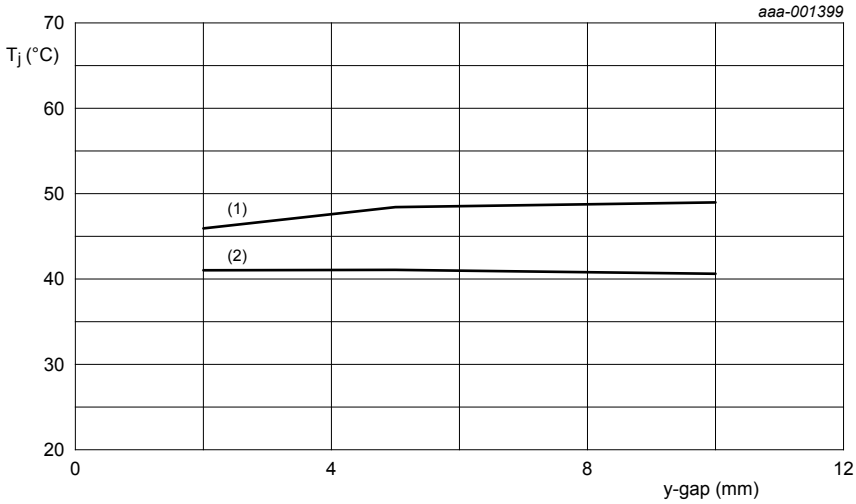


Fig 13. The enclosure partially filled with encapsulant (top) and completely filled (bottom)

5.5.1 Partial encapsulation

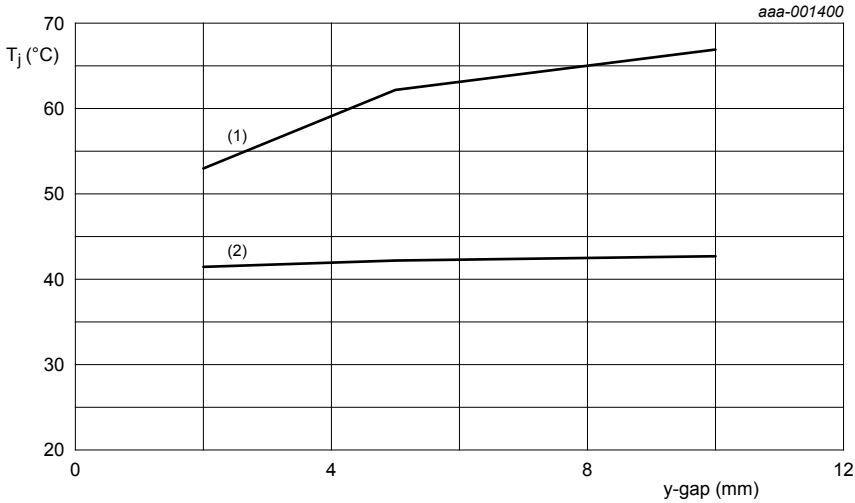
The results for the three enclosure types are shown in **Figure 14**, **Figure 15** and **Figure 16**. Results without encapsulation are also shown in each graph, for the purpose of comparison.



(1) 5 mm gap, no encapsulation.

(2) 5 mm gap, partial encapsulation.

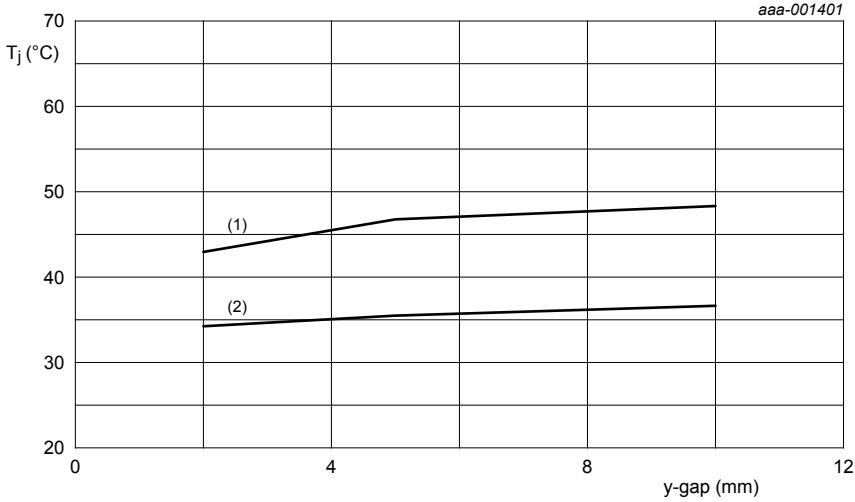
Fig 14. Partial encapsulation - black plastic enclosure



(1) 5 mm gap, no encapsulation.

(2) 5 mm gap, partial encapsulation.

Fig 15. Partial encapsulation - polished aluminium enclosure



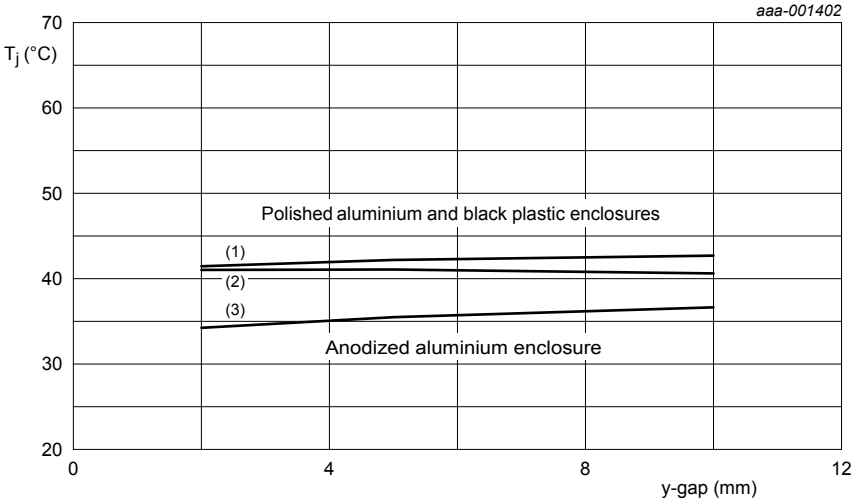
(1) 5 mm gap, no encapsulation.

(2) 5 mm gap, partial encapsulation.

Fig 16. Partial encapsulation - anodized aluminium enclosure

In all three cases, partial encapsulation results in major reductions in temperature. This strongly suggests that the new conduction paths introduced by the encapsulant are thermally better than those which it replaces. This is particularly noticeable for the polished aluminium material, where (relatively) poor radiation heat paths are replaced by more effective conduction paths.

The results are collated onto the single graph of **Figure 17**, again for the purpose of comparison.



(1) 5 mm gap, polished aluminium, partial encapsulation.

(2) 5 mm gap, black plastic, partial encapsulation.

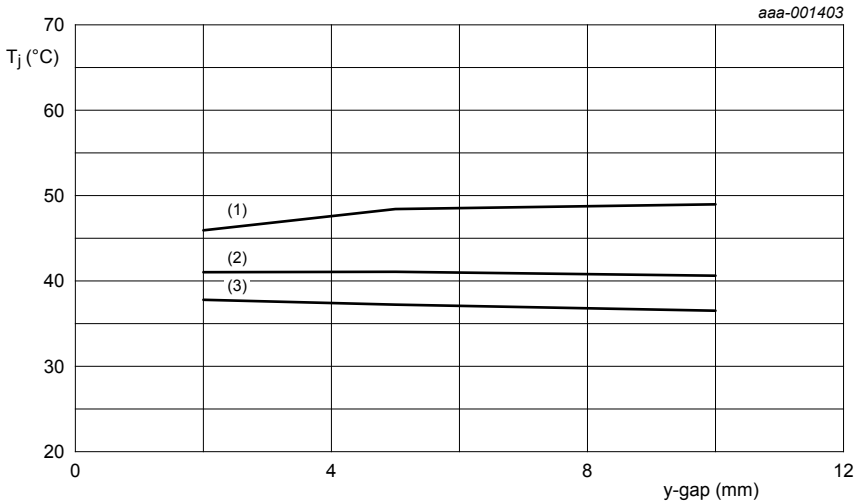
(3) 5 mm gap, anodized aluminium, partial encapsulation.

Fig 17. Partial encapsulation - the three enclosure types summarized

It is also interesting to note that the results have become largely independent of y-gap.

5.5.2 Full encapsulation

The results for the three enclosure types are shown in **Figure 18**, **Figure 19** and **Figure 20**. Results with half- and no encapsulation are also shown on each graph, for the purpose of comparison.

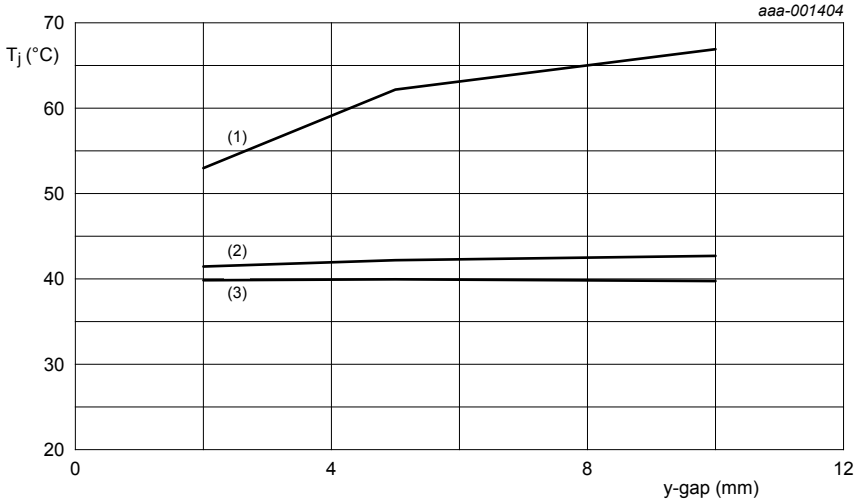


(1) 5 mm gap, no encapsulation.

(2) 5 mm gap, partial encapsulation.

(3) 5 mm gap, full encapsulation.

Fig 18. Full encapsulation - black plastic enclosure

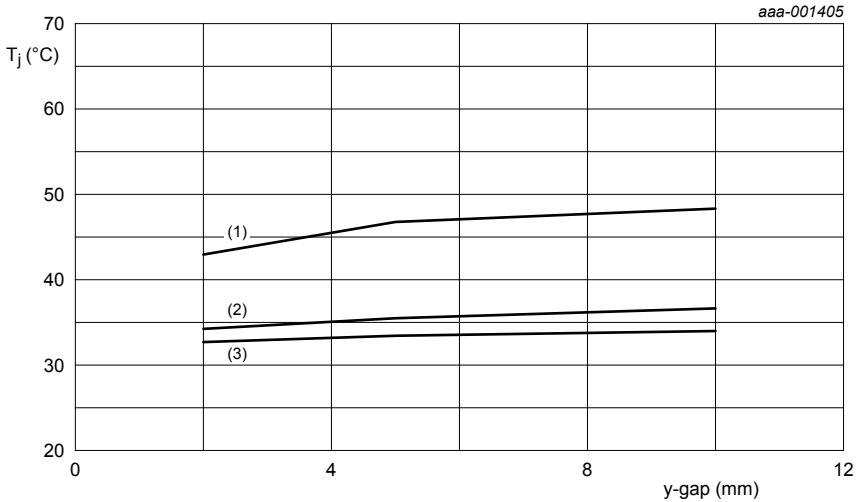


(1) 5 mm gap, no encapsulation.

(2) 5 mm gap, partial encapsulation.

(3) 5 mm gap, full encapsulation.

Fig 19. Full encapsulation - polished aluminium enclosure



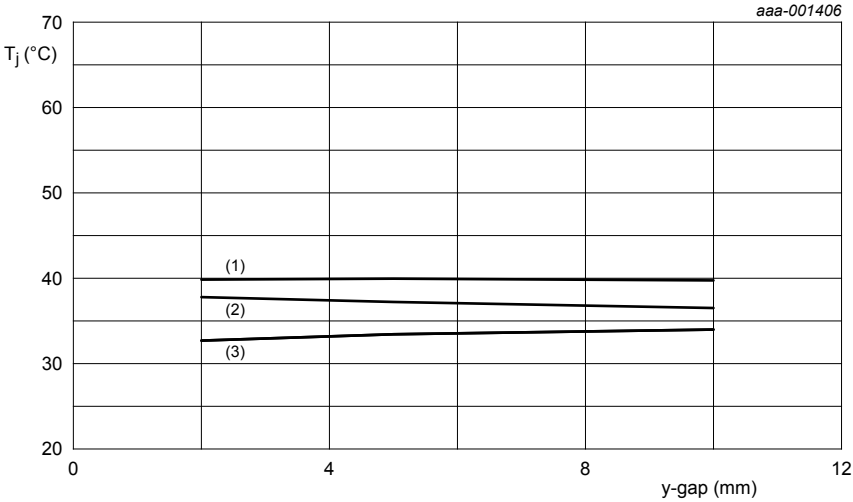
(1) 5 mm gap, no encapsulation.

(2) 5 mm gap, partial encapsulation.

(3) 5 mm gap, full encapsulation.

Fig 20. Full encapsulation - anodized aluminium enclosure

The results are very similar to those for partial encapsulation, with a general overall reduction in temperature, which is sometimes quite substantial, and a general independence of y-gap. The results are collated onto the single graph of **Figure 21**, again for the purpose of comparison.



(1) 5 mm gap, polished aluminium, full encapsulation.

(2) 5 mm gap, black plastic, full encapsulation.

(3) 5 mm gap, anodized aluminium, full encapsulation.

Fig 21. Full encapsulation - the three enclosure types summarized

By fully encapsulating the enclosure internal space we have made the thermal pathways identical, irrespective of enclosure material. However, we still see a difference in the thermal performance of enclosures of the same size but differing materials. This is because the thermal pathways within the enclosure are only part of the total path which the heat energy takes from source to ambient. The heat energy still has to travel through the walls of the enclosure by conduction, and then from the outside of the enclosure to ambient by convection and radiation. As these thermal pathways are heavily dependent on material properties, we still see differences in thermal performance for enclosures of the same size when fully encapsulated.

5.5.3 Summary: encapsulating the PCB

1. Encapsulation, whether partial or full, removes some or all of the radiation heat paths within the module and replaces still air with a more conductive material.
2. Both partial and full encapsulation result in a general decrease in device temperatures.
3. The results have become largely independent of y-gap.

5.6 Direct cooling through the enclosure

So far we have considered cases where the area of direct contact between PCB and enclosure has either been very small (only at the edges of the PCB) or non-existent. In this section, we will consider two cases where the contact between PCB and enclosure is much more direct.

5.6.1 Bottom-side cooling of the PCB

Bottom-side cooling (BSC) of the PCB is an arrangement whereby the underside of the PCB is brought close to the inner surface of the enclosure, separated by a thin insulating layer. See **Figure 22**.

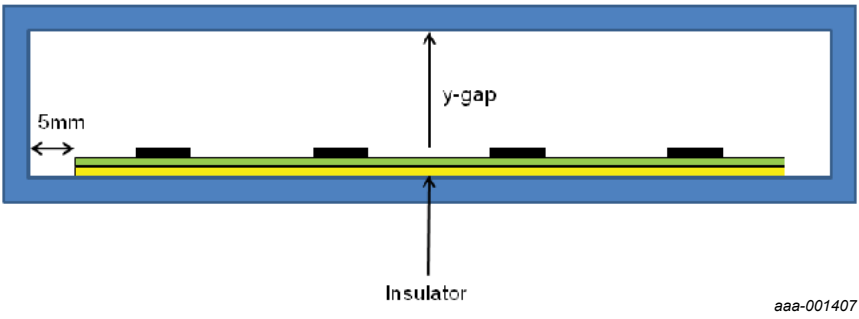
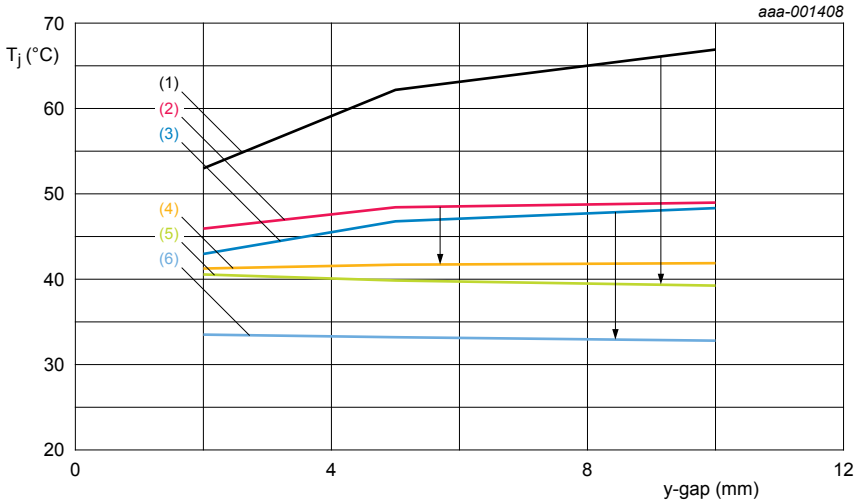


Fig 22. Bottom-side cooling of the PCB

The goal of bottom-side cooling is to channel the heat energy from the MOSFETs' die, through the bottom of the MOSFET device packages, through the PCB vias and into the enclosure. Within the enclosure the intention is to make conduction the primary heat transfer mechanism. Once the heat energy arrives at the enclosure it is dispersed to the local environment from the enclosure outer surface by convection and radiation in the usual way.

The insulator we have chosen has a thermal conductivity of 2.6 W/m.K and a thickness of 2.54 mm, and is representative of common insulating materials. The y-gap is now relevant to only one side of the PCB and, as in the previous section, we will only consider configurations where the PCB edge is separated from the enclosure walls by a gap of 5 mm. The results for all three enclosure types are shown in **Figure 23**, together with the corresponding results for non-bottom-side cooling, for comparison purposes.



(1) T_j polished aluminium.

(2) T_j black plastic.

(3) T_j anodized aluminium.

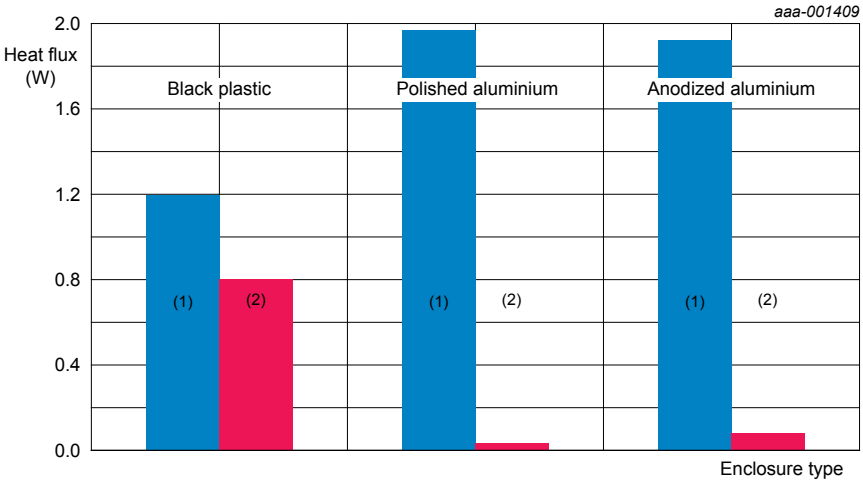
(4) T_j black plastic BSC.

(5) T_j polished aluminium BSC.

(6) T_j anodized aluminium BSC.

Fig 23. Bottom-side cooling (BSC) applied to the three enclosure types

The application of bottom-side cooling has resulted in a reduction in temperatures in all three cases, with results which are almost independent of y-gap. The extent to which we have succeeded in making conduction the dominant mechanism is shown in **Figure 24**. As T_j is now almost independent of y-gap, **Figure 24** shows only the results for y = 10 mm. A 10 mm gap is considered reasonable to allow for other components (connectors, capacitors, etc.) on the top side of the PCB.



(1) Conduction.

(2) Other paths.

Fig 24. Comparison of conduction heat transfer for the three enclosure types with bottom-side cooling applied (y-gap = 10 mm)

For the two aluminium enclosures the amount of heat transferred by conduction within the enclosure is in every case greater than 95 %. This should not be a surprise as aluminium is a relatively good conductor of heat (see **Table 1** and **Table 2**) and so does not present a significant barrier to the conduction of heat energy. Even for the plastic enclosure, the amount of heat transferred by conduction within the enclosure is still almost 60 %. When considered in conjunction with the graphs of **Figure 23**, this fact suggests that bottom-side cooling is an effective strategy for removing heat from the PCB. Finally, as we have seen before, the overall best performance is achieved with the anodized aluminium enclosure, which benefits both from good conduction and effective heat transfer by radiation.

5.6.2 Bottom-side cooling of the PCB, with encapsulation

For the final part of the bottom-side cooling analysis, we can also look at the effect of adding encapsulant to the inside of the enclosure. In **Section 5.5** we saw that replacing some or all of the air space inside the enclosure with encapsulant tended to reduce device temperatures, as the encapsulant has a better thermal conductivity than stagnant air. In the first part of **Section 5.6** we also saw that applying bottom-side cooling had a significant impact on device temperatures due to the presence of a direct conduction heat path through the wall of the enclosure. For the aluminium enclosure materials in particular, the majority of the heat was found to be passing through the enclosure wall by conduction (**Figure 24**). It will therefore be interesting to see, for instances when we already have good conduction through the enclosure wall, whether adding encapsulant will make any further significant difference to device temperatures. See **Figure 25**.

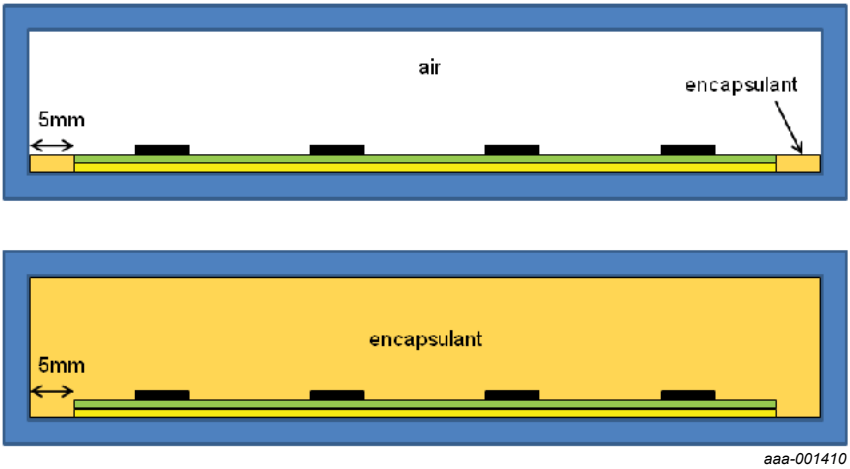
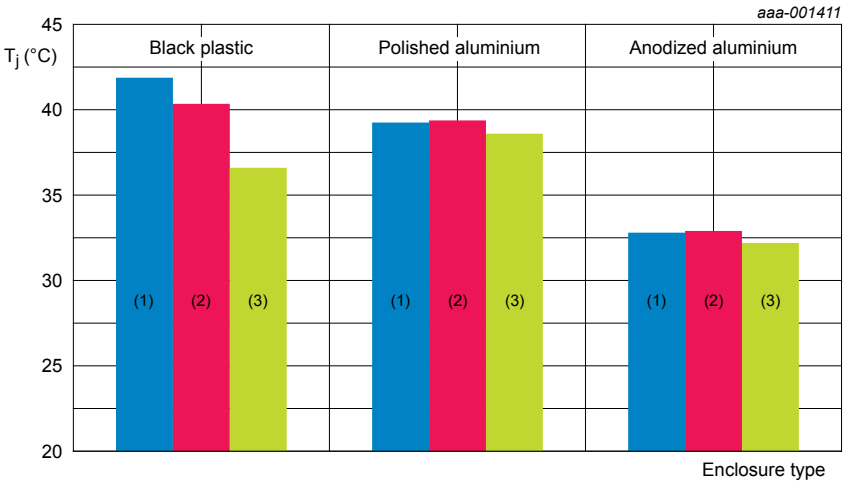


Fig 25. Bottom-side cooling with partial encapsulation (top) and full encapsulation (bottom)

The three bottom-side cooling scenarios from **Section 5.6.1** have been simulated with partial- and full encapsulation, and the results are shown in the graph of **Figure 26**.



(1) No encapsulation.

(2) Partial encapsulation.

(3) Full encapsulation.

Fig 26. Bottom-side cooling, with and without encapsulation

For the aluminium enclosures, the presence of encapsulation has made almost no difference to device temperature. These results are not surprising, as most of the heat energy is being transferred from the PCB to the enclosure by direct conduction anyway, and so adding encapsulant makes little additional difference. In the case of the plastic enclosure, however, the presence of the encapsulant makes a more significant difference as less heat is being transferred to the enclosure by direct contact (**Figure 24**).

5.6.3 Top-side cooling of the PCB

Top-Side Cooling (TSC) is an arrangement whereby the tops of the device packages are brought close to the inner surface of the enclosure, separated by a thin insulating layer. See **Figure 27**. Although there is no need for an electrical insulator between the device packages and the enclosure, a thermal "gap filler" is usually employed to allow a consistent contact between all the devices and the enclosure surfaces. For the purposes of this exercise we will use the same insulating material as in the bottom-side cooling cases.

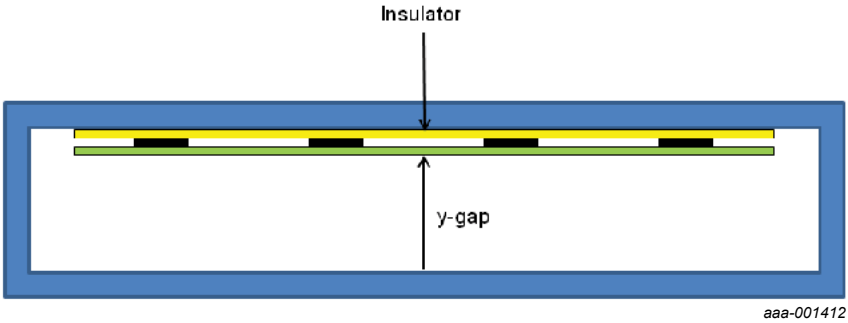
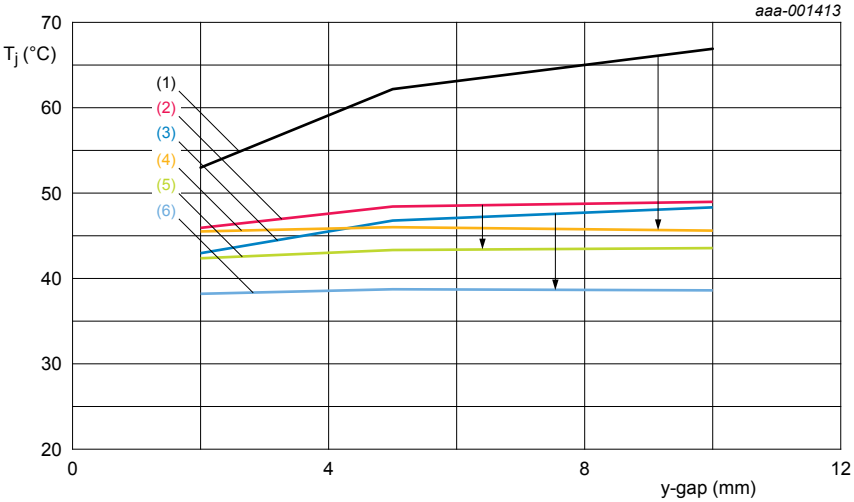


Fig 27. Top-side cooling of the devices

This arrangement is intended to channel the heat energy from the MOSFETs' die, through the top of the MOSFET device packages and into the enclosure.

The y-gap is again relevant to only one side of the PCB and, as in the previous section, we will only consider configurations where the PCB edge is separated from the enclosure walls by a gap of 5 mm. The results for all three enclosure types are shown in **Figure 28**, together with the corresponding results for non-top-side cooling, for comparison purposes.



(1) T_j polished aluminium.

(2) T_j black plastic.

(3) T_j anodized aluminium.

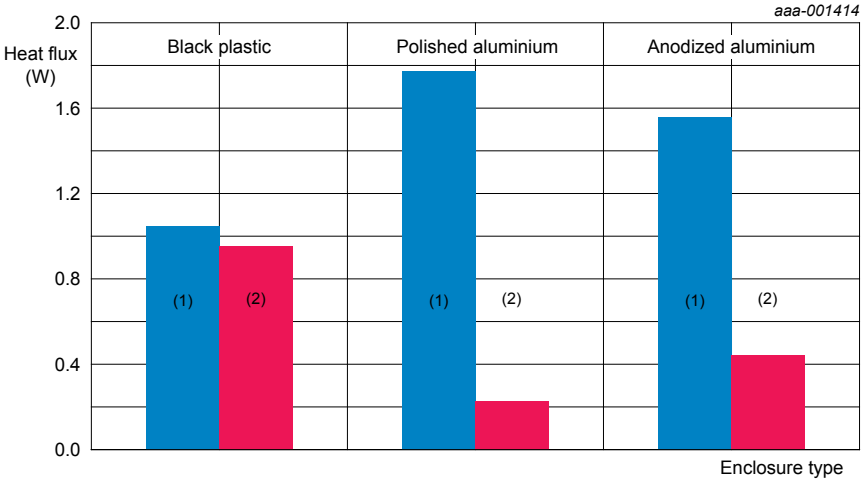
(4) T_j polished aluminium TSC.

(5) T_j black plastic TSC.

(6) T_j anodized aluminium TSC.

Fig 28. Top-side cooling applied to the three enclosure types

The results are strikingly similar to those for bottom-side cooling, shown in **Section 5.6.2**: the application of top-side cooling has again resulted in a reduction in temperatures in all three cases. Similarly, the results are also virtually independent of y-gap. The degree to which we have made conduction the dominant mechanism is shown in **Figure 29**.
As before, T_j is now almost independent of y-gap, and so **Figure 29** shows only the results for y = 10 mm.



(1) Conduction.

(2) Other paths.

Fig 29. Comparison of conduction heat transfer for the three enclosure types with top-side cooling applied (y-gap = 10 mm)

Compared to the figures for bottom-side cooling (**Figure 24**) we can see that, for the aluminium enclosures, conduction is not quite so dominant, and for the plastic enclosure the split is almost equal between conduction and the other paths combined. This is perhaps not surprising, as in the top-side cooling scheme the heat energy must pass through the (admittedly thin) layer of plastic on the package tops before reaching the insulator and enclosure, and as we have seen, plastic is a relatively poor conductor of heat energy. On the other hand, for the bottom-side cooling scheme, the heat energy has a relatively high conductivity path (solder, PCB planes, thermal vias) before reaching the insulator, and is not impeded by a layer of plastic.

5.6.4 Top-side cooling of the PCB, with encapsulation

Following the same progression as for bottom-side cooling, we will also look at the effect of adding encapsulant to the top-side cooling scheme. See **Figure 30**.

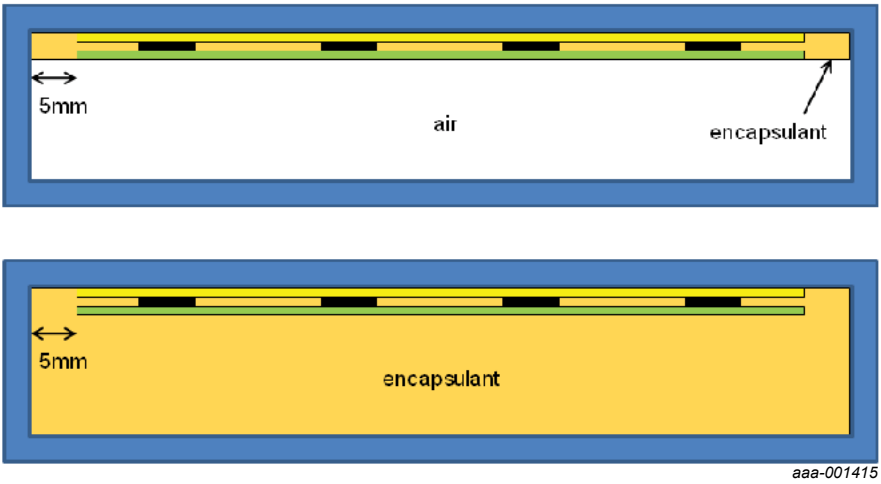
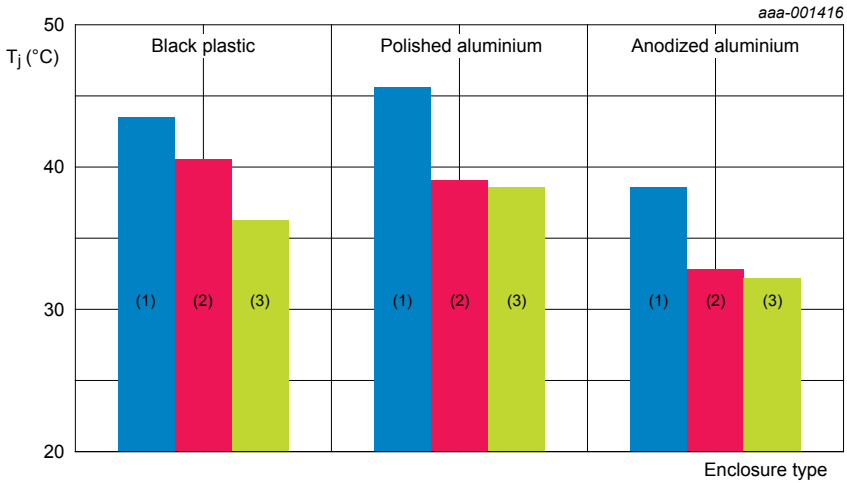


Fig 30. Top-side cooling with partial encapsulation (top) and full encapsulation (bottom)

In the bottom-side cooling scheme we saw that adding encapsulation tended to lower device temperatures for the plastic enclosure, but made little difference for the aluminium enclosures. This was because, for the aluminium enclosure material, the majority of the device heat energy was found to be passing through the PCB and enclosure wall by conduction, and so adding the encapsulant material made little difference to thermal pathways which were already very effective.

In the top-side cooling scheme we have already identified the device plastic as a potential barrier to the flow of heat energy, so it will therefore be interesting to see whether adding encapsulant will make any significant difference to device temperatures.

The three top-side cooling scenarios from **Section 5.6.3** have been simulated with partial and full encapsulation, and the results are shown in the graph of **Figure 31**.



(1) No encapsulation.

(2) Partial encapsulation.

(3) Full encapsulation.

Fig 31. Top-side cooling, with and without encapsulation

It is interesting to compare these results with those for bottom-side cooling (**Figure 26**). For the aluminium enclosures with bottom-side cooling, the presence of encapsulation made almost no difference to device temperatures. However, for top-side cooling, we see a notable decrease in temperature when encapsulation is applied. This is a reflection of the fact that the thermal pathway from the devices in a top-side cooling scheme is not as direct as it is for bottom-side cooling, and so improving the path from the bottom of the PCB (by replacing the air with encapsulant) results in a reduction in device temperature.

5.6.5 Summary: direct cooling through the enclosure

Bottom-side cooling:

- The application of bottom-side cooling results in a reduction in device temperature. The degree to which temperature is reduced is dependent on the enclosure material
- Results become almost independent of y-gap
- For the aluminium enclosures, the presence of encapsulation makes almost no difference to device temperatures. For the plastic enclosure, the encapsulant results in reduced device temperatures.

Top-side cooling:

- The application of top-side cooling also results in a reduction in device temperature. Again, the degree to which temperature is reduced is dependent on the enclosure material.
- However, top-side cooling is not as effective as bottom-side cooling
- Results become almost independent of y-gap
- For all three enclosure types, there is a notable decrease in device temperature when top-side cooling is applied

5.7 Mounting the enclosure on a bulkhead

All of the cases we have looked at so far have the module located horizontally in free air. In this last chapter we will consider the module's thermal performance when located in a manner more representative of actual usage i.e. mounted vertically, close to a steel bulkhead.

For the purposes of this exercise, we will consider the following module variations:

1. Module x- and z-gaps fixed at 5 mm.
2. Module y-gap(s) fixed at 10 mm.
3. Three enclosure materials (black plastic, polished aluminium, anodized aluminium).
4. PCB mounted centrally in the enclosure.
5. PCB with bottom-side cooling applied.
6. PCB with top-side cooling applied.

5.7.1 Vertical orientation of the module

Before considering the effect of the steel bulkhead, we will first examine what happens when we orientate the module vertically rather than horizontally. See **Figure 32**.

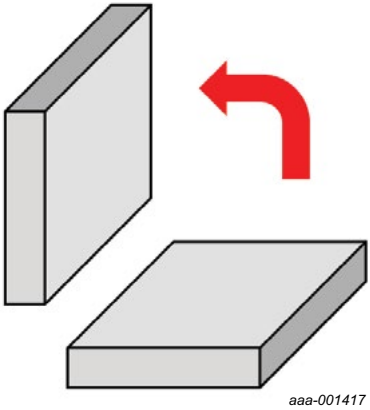
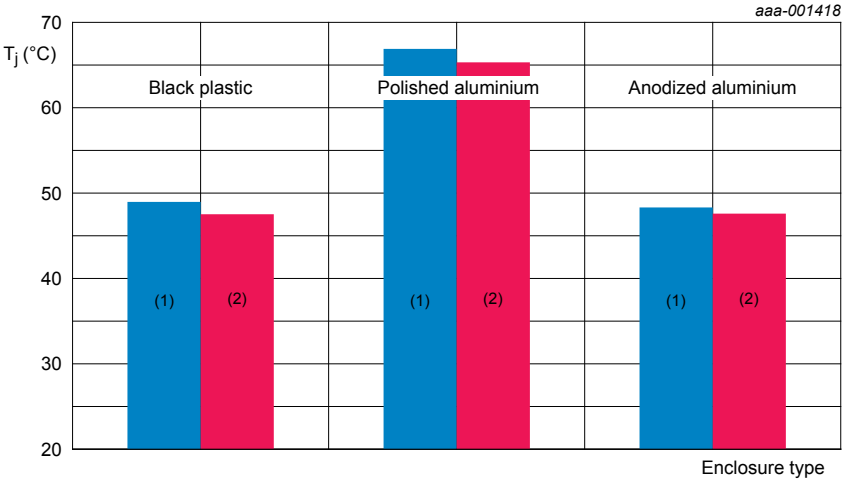


Fig 32. Orientating the module vertically

The effect on device temperatures is shown in the graph of **Figure 33**.



(1) Module horizontal.

(2) Module vertical.

Fig 33. The effect of module orientation on device temperature

At most, the change in orientation has resulted in a decrease in device temperature of 1.5 °C. Remember that at this stage the PCB is still mounted centrally within the enclosure i.e. the y-gaps above and below the PCB are 10 mm.

5.7.2 Adding the bulkhead

The next stage is to add the bulkhead to the scenario. Rather than mount the module directly against the bulkhead, with perfectly flat adjoining surfaces, we have instead chosen to mount the module using 5 mm plastic "standoffs". This means that there is an air gap of 5 mm between the surface of the module and surface of the bulkhead. This is felt to better represent reality, as any real-life module would probably be mounted using some form of plastic clips. See **Figure 34**.

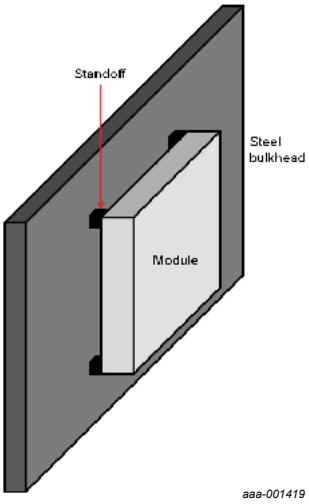


Fig 34. The module mounted on the bulkhead

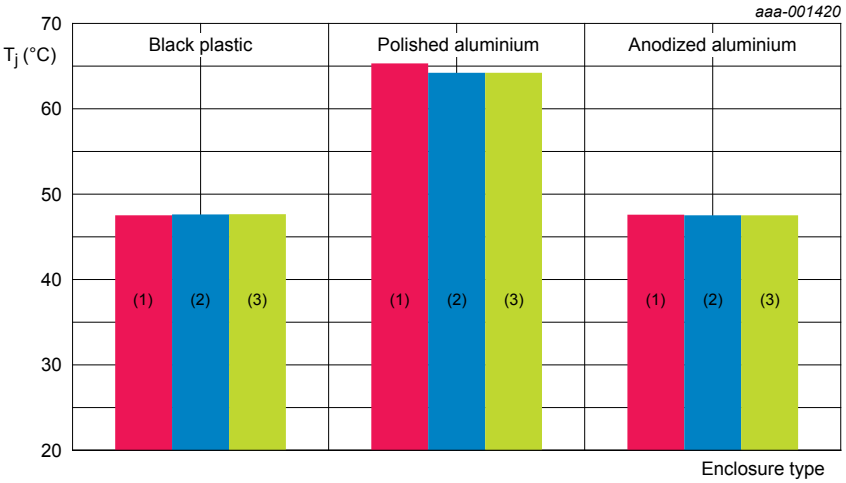
The bulkhead itself is modeled as a piece of steel measuring 220 mm x 170 mm x 5 mm. As the bulkhead is now a part of the overall thermal system, we have to decide how to model its thermal characteristics. On the one hand, we could model the bulkhead as a normal piece of conducting material which is capable of transferring heat by the processes of conduction, convection and radiation. However, if we take this approach then we have to consider how the section of bulkhead will itself lose heat energy to its surroundings, and the danger with this approach is that we could end up trying to model the entire vehicle!

An alternative approach, and the one adopted here, is to define the bulkhead as a fixed temperature block at the ambient temperature of 20 °C. This means that, no matter how much heat energy is passed into the bulkhead, its temperature will remain at a fixed, uniform 20 °C. The justification for this approach is that, in reality, the bodywork of the vehicle is so much more massive than the module that, for all practical purposes, the bulkhead is almost the "perfect heatsink" used in the model.

A final point which must be addressed is that of which of the two sides of the module should be nearest to the bulkhead. This could be an important consideration in scenarios where, for instance top-side or bottom-side cooling of the PCB is employed. We will therefore consider both cases, where both the bottom and top of the module are nearest to the bulkhead. The "bottom" of the module is considered to be the side nearest to the solder side of the PCB, and the "top" of the module is the side nearest to the component side of the PCB.

5.7.3 Results for the PCB mounted centrally in the module

The results for the module with PCB mounted centrally (y-gaps above and below the PCB are 10 mm) are shown in **Figure 35**. Results are shown for the module mounted bottom-side to the bulkhead, top-side to the bulkhead and without any bulkhead.



(1) No bulkhead.

(2) Module bottom side to bulkhead, with 5 mm gap.

(3) Module top side to bulkhead, with 5 mm gap.

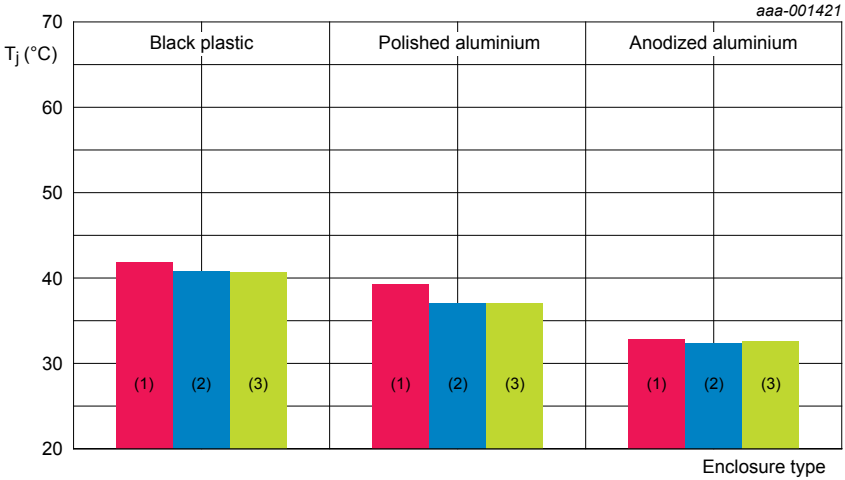
Fig 35. Results for the module mounted on the bulkhead (PCB central)

For a given enclosure material, there is little difference in temperature whether the module is mounted on the bulkhead or not, and also whether the bottom or top side of the module is nearest to the bulkhead.

We might consider this an unexpected result, as the presence of the bulkhead should be interfering with the process of natural convection occurring on one side of the module. While this is undoubtedly true, and the air on the affected sides remains "trapped" and stationary against the side of the module, the air (and hence the side of the module in contact with it) is maintained at a lower than normal temperature by the fixed-temperature bulkhead. We might think of this effect as "heat sinking at a distance". Hence the lack of convection on one side is compensated for and there is almost no effect on device temperature.

5.7.4 Results for the PCB with bottom-side cooling

The results for the module with bottom-side cooling (y-gap above the PCB is 10 mm) are shown in **Figure 36**. The vertical scale in **Figure 36** has been deliberately made the same as for **Figure 35** in order to facilitate comparison of the results.



(1) Horizontal (no bulkhead).

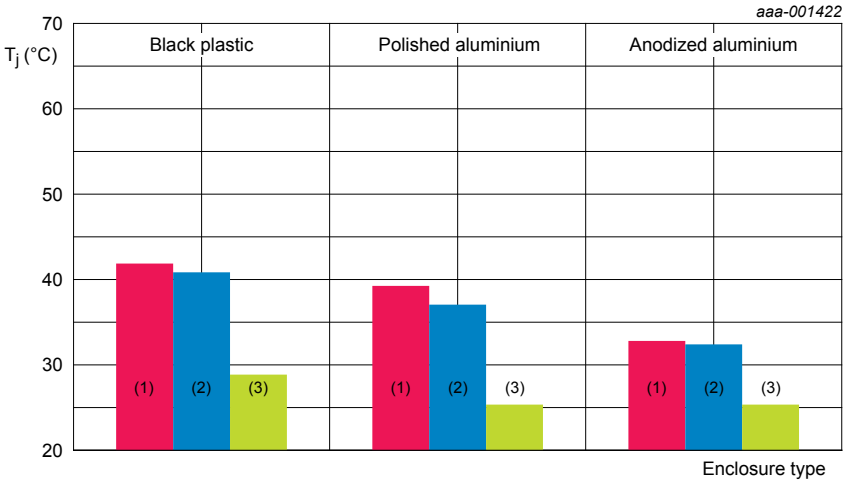
(2) Module bottom side to bulkhead, with 5 mm gap.

(3) Module top side to bulkhead, with 5 mm gap.

Fig 36. Results for the module mounted on the bulkhead (PCB utilizing bottom-side cooling)

Once again, for a given enclosure material, we do not see a dramatic difference when the module is mounted on the bulkhead. This might seem a little surprising as, inside the module, there is a good conduction path from the devices, through the PCB and into the enclosure material. However, the heat energy is still required to bridge the air gap between the module outer surface and the bulkhead, and so any heat sinking effect from the bulkhead is effectively eliminated.

In order to illustrate this point a little better, we will consider the same scenario once more (PCB bottom-side cooled within the module) except that this time we will attach the module face directly to the bulkhead. This will be a "perfect attachment" with no contact resistance and complete, uniform contact between the surfaces. Such a perfect arrangement could never be achieved in real life, and the results are shown here simply for interest (**Figure 37**).



(1) Horizontal (no bulkhead).

(2) Module bottom side to bulkhead, with 5 mm gap.

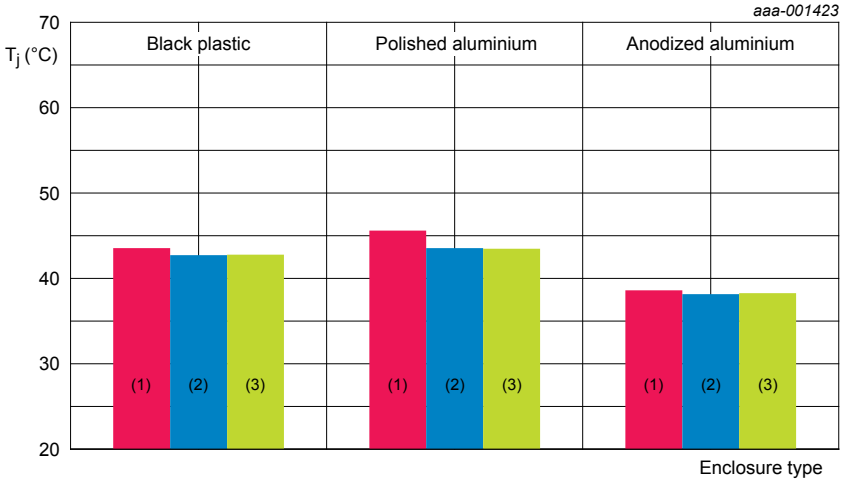
(3) Module bottom side in contact with bulkhead.

Fig 37. Results for the module mounted "perfectly" on the bulkhead

As one might expect, with an uninterrupted conduction path between the module and the bulkhead, there is a significant reduction in device temperature.

5.7.5 Results for the PCB with top-side cooling

The results for the module with top-side cooling (y-gap below the PCB is 10 mm) are shown in **Figure 38**.



(1) Horizontal (no bulkhead).

(2) Module bottom side to bulkhead, with 5 mm gap.

(3) Module top side to bulkhead with 5 mm gap.

Fig 38. Results for the module mounted on the bulkhead (PCB utilizing top-side cooling)

The trend in results is very similar to that seen for the bottom-side cooled PCB i.e. the presence of the bulkhead actually makes little difference to the device temperatures.

5.7.6 Summary: mounting the enclosure on a bulkhead

- Altering the module orientation from horizontal to vertical has little effect on device temperatures - at most a decrease of 1.5 °C was observed
- Adding the bulkhead to the module with central PCB also makes little difference to device temperatures
- The bulkhead limits convection heat loss from the surface of the enclosure, but also provides an effect of "heat sinking at a distance". These two phenomena tend to cancel each other out.
- The bottom-side cooling version of the module does not benefit from the presence of the bulkhead unless mounted directly on it with "perfect" thermal contact. This is an arrangement which is likely to be unachievable in practice.
- The top-side cooling version of the module also does not benefit from the close proximity of the bulkhead
- Overall, mounting the module vertically and close to a bulkhead does not make things dramatically better or worse

5.8 Summary

Thermal aspects are an important concern when designing with power MOSFETs. Both MOSFET junction temperature and PCB temperature must be kept within safe limits if reliable operation is to be ensured.

Chapter 4 considered the impact of various different PCB and device configurations on thermal behavior. The factors considered included PCB layer count, the impact of thermal vias and the placement of multiple devices.

The scenarios considered in chapter 4 utilized PCBs situated in free air, with no enclosures or housings included in the scenarios. The primary heat loss mechanism from the PCBs was therefore natural convection, unimpeded by the presence of any other physical structure.

This design guide has addressed the likelihood that, in most real-life applications, the need to protect the PCB from environmental factors, plus possible considerations for electromagnetic compatibility would almost certainly dictate that the PCB would be mounted in an enclosure of some form. The investigations have examined how the enclosure, and the bulkhead on which it may be mounted, have impacted on the thermal performance of the system.

The design guide has considered three enclosure materials with differing thermal properties and dimensions. Encapsulation within the enclosure, and the role of bottomand top-side cooling has also been examined, as has the effect of locating the module in close proximity to a bulkhead. From this investigation we have been able to draw several interesting conclusions:

1. Adding an enclosure around the PCB may or may not increase device temperatures - this depends on several other factors.

2. The air within the enclosure is not able to move, and hence the normal process of heat loss by convection does not occur. Instead, the air behaves as a stationary conductor with low thermal conductivity.

3. In the absence of convection, heat loss by radiation becomes of more significance, and hence the surface finish of the materials employed also becomes significant.

4. Partially or completely filling the enclosure with encapsulant results in a lowering of temperatures, as the encapsulant has a higher thermal conductivity than the stationary air it replaces.

5. The use of bottom- and top-side cooling techniques can reduce device temperatures significantly. Of the two, bottom-side cooling is more effective.

6. Altering the module orientation from horizontal to vertical has almost no effect on device temperatures.

7. The presence of the bulkhead makes little difference to device temperatures.

While this chapter cannot hope to address all possible different module configurations, it is hoped that those presented here are representative of typical “real life” usage.

Finally, we should reiterate that the information contained within this design guide is presented as a starting point only. Any new design should of course be prototyped and its thermal behavior characterized before placing the design into production.

Chapter 6: Using power MOSFETs in parallel

Chapter 6: Using power MOSFETs in parallel

6.1 Introduction

One much publicized benefit of power MOSFETs (compared to other semiconductor devices) is that it is easy to parallel them to create a group with increased capability. Although this feature is superficially true, there are several potential problems that can catch out the unwary circuit designer.

A MOSFET consists of a group of paralleled 'cells' fabricated on the surface of a silicon die. All the cells are created at the same time under the same conditions. When the MOSFET is fully enhanced and conducts channel current, the temperatures of all the cells are very similar. As the cells are structurally and thermally closely matched, they share current and power well and the parameters of the MOSFET can be well-defined.

There is a range of values for the parameters of the MOSFET dies on a wafer. There is a wider range for MOSFET dies on different wafers in the same production batch. The range is even wider for all batches even though the MOSFETs are the same type. MOSFETs with parameter values outside the data sheet limits are rejected.

The MOSFETs in a paralleled group should all be the same type, but their parameters could be anywhere within the data sheet range. Their die temperatures are unlikely to be the same. Consequently their power sharing is not perfect.

This chapter contains guidelines on how to design a group of MOSFETs to get the best performance from them. The design must accommodate MOSFET variations within the data sheet limits. It must also allow for MOSFET parameter variations over the range of electrical and environmental conditions. If all the MOSFETs in the group work within their safe maximum limits, the paralleled group of MOSFETs operates reliably.

It is technically and commercially undesirable to have to select MOSFETs and it should be unnecessary. The circuit should be designed to accommodate any MOSFET within the worst case $R_{DS(on)}$ range.

The key data sheet limit which must not be exceeded is the maximum junction temperature $T_{j(max)}$ of 175 °C.

6.2 Static (DC) operation

This situation is the simplest condition where current flows through a group of paralleled MOSFETs that are fully enhanced (switched ON). A proportion of the total current flows through each MOSFET in the group. At the initial point of turn on, the die temperatures of all the MOSFETs in the group are the same. The drain current I_D flowing in each MOSFET is inversely proportional to its $R_{DS(on)}$ (the drain-source voltage V_{DS} across all the MOSFETs is the same).

The MOSFET with the lowest $R_{DS(on)}$ takes the highest proportion of the current and dissipates the most power (power dissipation $P = V_{DS} \times I_D$).

All the MOSFETs heat up, but the MOSFET with the lowest $R_{DS(on)}$ heats up most (assuming the $R_{th(j-a)}$ of all the MOSFETs is the same).

MOSFET $R_{DS(on)}$ has a positive temperature coefficient. $R_{DS(on)}$ increases as T_j increases. The die temperatures and $R_{DS(on)}$ values of all MOSFETs in the group rise, but the die temperature of the lowest $R_{DS(on)}$ MOSFET increases disproportionately. The effect of this behavior is to redistribute the current towards the other (higher $R_{DS(on)}$) MOSFETs in the group.

Stable thermal equilibrium is reached after a period of operation. The lowest $R_{DS(on)}$ MOSFET is the hottest, but carries a lower proportion of the current than it did initially.

The Positive Temperature Coefficient (PTC) of $R_{DS(on)}$ is a stabilizing influence that promotes power sharing between the MOSFETs in the group. However, as stated earlier the most important criterion is that the maximum junction temperature of any MOSFET in the group must not exceed 175 °C.

The cooling of each MOSFET in the group depends on its thermal resistance from junction to ambient. Die temperature influences the heat flow from adjacent MOSFETs. Rather than considering the thermal resistance paths between the MOSFET dies, the main influence is the temperature of the common heatsink. All the MOSFET mounting bases are bonded electrically and thermally to this heatsink.

The lowest $R_{DS(on)}$ MOSFET could be located anywhere in the group. The thermal resistance from mounting base to ambient of all the MOSFETs in the group should be as similar as possible and as low as possible. Cooling is optimized and independent of location.

This thermal resistance solely depends on the thermal characteristics and design of the assembly [Printed-Circuit Board (PCB) or heatsink] to which the MOSFET is thermally bonded.

Sometimes a value for $R_{th(j-a)}$ is given in data sheets but this parameter is of very limited value. It cannot be treated as a well-defined parameter because it also depends on other external factors such as PCB construction, PCB orientation and air flow. The only guaranteed thermal parameter is the thermal resistance from the MOSFET junction to mounting base $R_{th(j-mb)}$.

6.2.1 Worked examples for static operation

The worked examples that follow are based on the BUK764R0-40E.

Table 1. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.82	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a PCB	-	50	-	K/W

A typical group of MOSFETs has a range of $R_{DS(on)}$ values. The distribution has a peak at around the typical data sheet $R_{DS(on)}$ value; none should have an $R_{DS(on)}$ higher than the data sheet maximum. The $R_{DS(on)}$ of about half of the samples is less than the typical value.

Minimum $R_{DS(on)}$ is not given in the data sheet, but a good estimate is

(1) $$R_{DS(on)(min)} \approx R_{DS(on)(max)} - 2(R_{DS(on)(max)} - R_{DS(on)(typ)})$$

The $R_{DS(on)}$ value range means that a group of typical MOSFETs is very unlikely to share power equally when they are operated in parallel.

The worst case would be when one of the MOSFETs has the minimum $R_{DS(on)}$ and all the others have the maximum $R_{DS(on)}$.

Modeling of the electro-thermal system is complex because its electrical and thermal characteristics are mutually dependent. However, an electro-thermally convergent Excel model can be used to estimate the performance characteristics of a paralleled group. As an example, in a worst case situation three BUK764R0-40E MOSFETs are connected in parallel; two have maximum $R_{DS(on)}$ of 4 mΩ. The other has a lower than typical $R_{DS(on)}$ of 2.6 mΩ.

The MOSFET with the lowest $R_{DS(on)}$ value takes the highest proportion of the current. It therefore has the highest power dissipation.

The target is to keep the junction temperature of the hottest MOSFET below 175 °C under worst case operating conditions.

These estimations are simplified illustrations. The thermal representation of the MOSFET group is less complex than a real application. In a real application, there are other factors such as neighboring components and orientation that would influence cooling. However, they show the approximate behavior of the group with two different $R_{th(j-a)}$ values.

The first scenario shows the system with the thermal resistance from junction to ambient for each MOSFET ($R_{th(j-a)}$ = 20 K/W; T_{amb} = 125 °C).

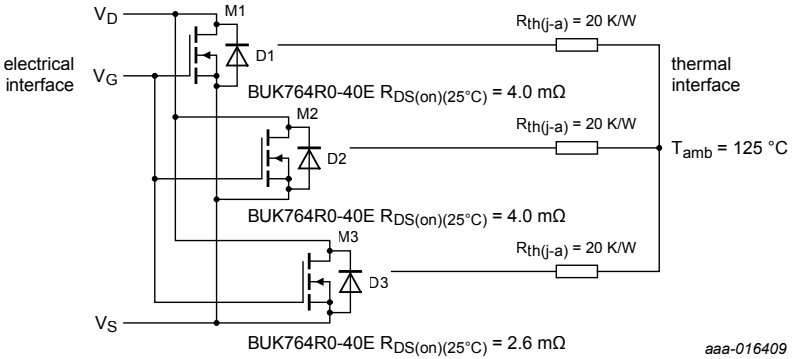


Fig 1. Electrical and thermal schematic diagram of the three paralleled BUK764R0-40E MOSFETs

Table 2 shows the maximum safe limits of V_{DS}, I_D, P and T_j for all the MOSFETs at thermal equilibrium. At this point, the junction temperature of the hottest MOSFET is almost 175 °C.

Table 2. MOSFET maximum conditions for $R_{th(j-a)}$ = 20 K/W and T_{amb} = 125 °C

MOSFET	V_{DS} [V]	$R_{th(j-a)}$ [K/W]	RDS(on) (25 °C) [mΩ]	Initial RDS(on) (125 °C) [mΩ]	Initial current ID [A]	Initial power P [W]	Initial power share [%]	Final $R_{DS(on)}$ [mΩ]	Final current I_D [A]	Final power P [W]	Final T_j [°C]	Final power share [%]
M1	0.11	20	2.6	4.16	42.31	4.65	43.5	4.92	22.36	2.46	174	42.3
M2	0.11	20	4	6.4	27.50	3.03	28.3	7.21	15.26	1.68	159	28.9
M3	0.11	20	4	6.4	27.50	3.03	28.3	7.21	15.26	1.68	159	28.9

Total initial power P(M1 + M2 + M3) = 10.70 W

Total final power P(M1 + M2 + M3) = 5.82 W

The second scenario relates to the same electrical system, but with ideal thermal characteristics. The thermal resistance $R_{th(j-a)}$ of each MOSFET is 0.82 K/W. This situation corresponds to the ideal but unrealistic situation where each MOSFET is perfectly thermally bonded to an infinite heatsink (a heatsink with zero thermal resistance).

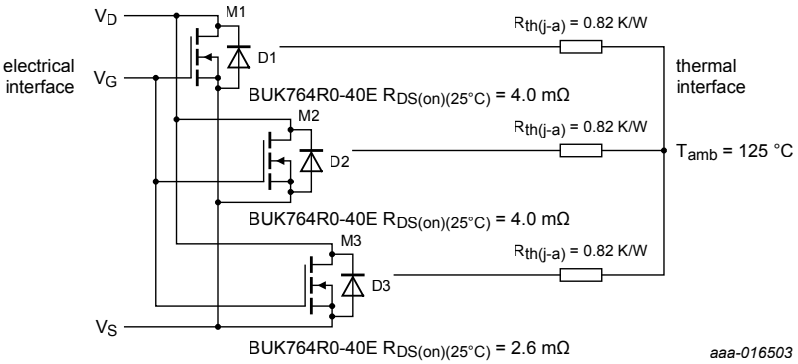


Fig 2. Electrical and thermal schematic diagram of the three paralleled BUK764R0-40E MOSFETs with ideal thermal conditions

Table 3 shows the values of V_{DS}, I_D, P and T_j for all the MOSFETs at thermal equilibrium. At this point, the junction temperature of the hottest MOSFET is almost 175 °C.

Table 3. MOSFET maximum conditions for $R_{th(j-a)}$ = 0.82 K/W and T_{amb} = 125 °C

MOSFET	V_{DS} [V]	$R_{th(j-a)}$ [K/W]	RDS(on) (25 °C) [mΩ]	Initial RDS(on) (125 °C) [mΩ]	Initial current ID [A]	Initial power P [W]	Initial power share [%]	Final $R_{DS(on)}$ [mΩ]	Final current I_D [A]	Final power P [W]	Final T_j [°C]	Final power share [%]
M1	0.55	0.82	2.6	4.16	211.54	116.35	43.5	4.92	111.79	61.48	174	42.3
M2	0.55	0.82	4	6.4	137.50	75.63	28.3	7.21	76.28	41.96	159	28.9
M3	0.55	0.82	4	6.4	137.50	75.63	28.3	7.21	76.28	41.96	159	28.9

Total initial power P(M1 + M2 + M3) = 267.60 W

Total final power P(M1 + M2 + M3) = 145.39 W

Note: This scenario is ideal and unrealistic. It is included to illustrate the benefit of reducing $R_{th(j-a)}$ to maximize the usage of the MOSFET capabilities.

In practice, $R_{th(j-a)}$ is always greater than $R_{th(j-mb)}$. The thermal bonding between the MOSFET mounting base and the heatsink is never perfect and an infinite heatsink does not exist in the real world.

In this case, the drain current (I_D) of the MOSFETs becomes the limiting factor (the data sheet maximum I_D is 75 A).

To optimize MOSFET utilization, the MOSFETs must be able to dissipate as much power as possible. At the same time, the junction temperature of the hottest MOSFET must remain below the maximum safe temperature of 175 °C.

The following conclusions can be drawn from **Table 2** and **Table 3**:

1. It is beneficial to reduce $R_{th(j-a)}$ as much as possible to optimize the MOSFET die cooling.
2. It is beneficial to reduce the maximum ambient temperature to increase the available thermal ‘headroom’.
3. As a result of **Table 2** and **Table 3**, it is clear that junction temperature difference between the MOSFETs depends only on their $R_{DS(on)}$ values (assuming the $R_{th(j-a)}$ for each MOSFET is the same).

4. When the paralleled (fully enhanced) MOSFETs heat up during use, their power distribution changes such that the cooler MOSFETs take a greater proportion of the power. This effect is due to the PTC of $R_{DS(on)}$ and it acts to promote thermal stability.

6.3 MOSFET mounting for good thermal performance and power sharing

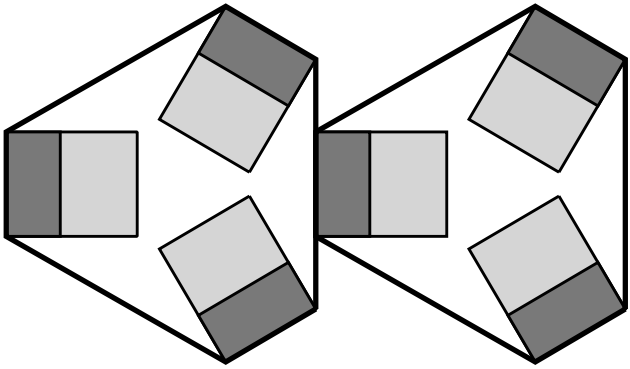
To get the most from the MOSFET group, the individual MOSFET should be mounted in a way that causes their mounting base temperatures to be as similar as possible and also as low as possible.

To realize this goal, the thermal resistance between each MOSFET (mounting base) and the mounting bases of all the other MOSFETs in the group should be matched and minimized. They should be mounted symmetrically and as close together as possible on a thermally conductive surface.

Heat flow can be considered to be analogous to electric current flow; so the thermal bonding points of the MOSFETs (usually the drain tabs) should be on a thermal 'ring main'. The low thermal resistance path allows heat to flow easily between the MOSFETs. When heat flows easily between all the MOSFETs in the group, their mounting base temperatures track together closely.

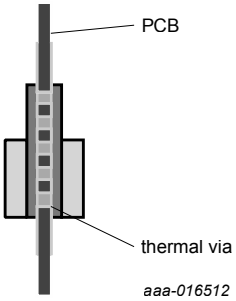
Note: This arrangement does not promote equal current sharing, but promotes better die temperature matching. The temperatures of all the MOSFETs in the group can rise more before the temperature of the hottest MOSFET reaches 175 °C. Hence the power dissipation capability of the group is maximized.

There are practical limits to the physical extent of the thermal ring main; ideally each MOSFET should be next to all its neighbors. This condition limits the group to two or three MOSFETs.

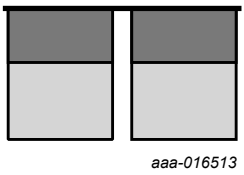


This layout suits standard packaged MOSFETs (e.g. D2PAK, LFPAK and TO-220). The dark shaded area corresponds to the drain tab of the device.

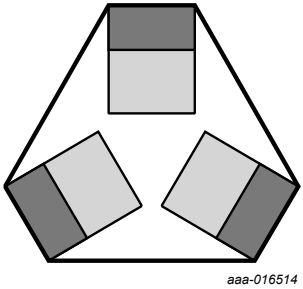
Fig 3. A layout for six paralleled MOSFETs to promote good power sharing



a. Two paralleled MOSFETs where both devices are located directly opposite each other on the two faces of a PCB



b. Two paralleled MOSFETs where the devices are located next to each other on the same face of a PCB



c. Three paralleled MOSFETs where the devices are located in a symmetrical loop other on one face of a PCB

Fig 4. Good layout arrangements for two paralleled MOSFETs and three paralleled MOSFETs

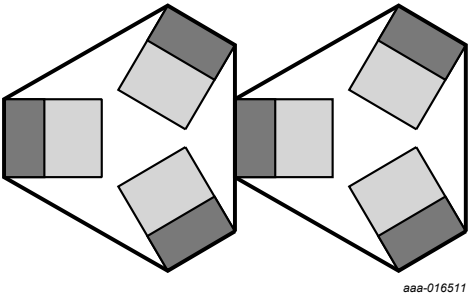
A good way to parallel a pair of MOSFETs is to locate them on opposite faces of a PCB forming a PCB 'sandwich' as in **Figure 4**a. Thermal vias between the copper 'land' areas on the PCB reduce the electrical and thermal resistances between their mounting bases.

To parallel a pair of MOSFETs on the same face of a PCB, they can be mounted next to each other as in **Figure 4**b.

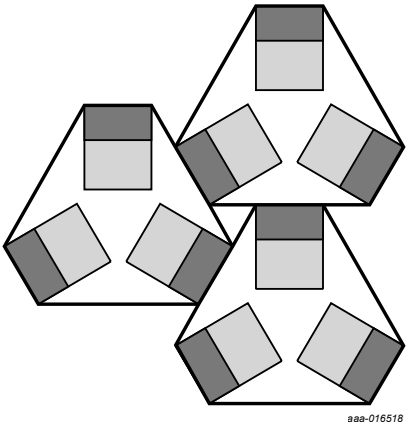
A good way to parallel three MOSFETs is in a ring as in **Figure 4**c. This arrangement allows all the MOSFET sources in the group to be connected to a 'star' point. The electrical and thermal paths between the MOSFET drains match due to their symmetrical connections to the drain loop.

Minimizing and matching the electrical impedances in the source paths is more important than matching the electrical impedance in the drain paths. This difference is because their gate drives are related to the sources. Good impedance matching in both drain and source is more important in high frequency switching circuits.

If similar electrical and thermal matching can be achieved, larger paralleled groups could be considered. Groups of more than four or five become unwieldy so grouped sub groups should be used.



a. Six paralleled MOSFETs based on two sub groups of three MOSFETs



b. Nine paralleled MOSFETs based on three sub groups of three MOSFETs

Fig 5. Layouts using sub groups of three MOSFETs

In this group of 9 (3 groups of 3), there is a natural drain star point at the center of the group. There are separate source star points at the centers of each sub group. The source star points can be connected on a layer of a multi-layer PCB.

There is a compromise between optimizing layout for power sharing and maximizing PCB usage.

Electrically and thermally optimized layouts always use more PCB area than the minimum possible, but utilization of MOSFET capability should be better. Areas of PCB that are unoccupied by MOSFETs or gate drive components are useful for thermal interfaces with heat sink or cooling air.

6.4 Power sharing in dynamic operation [pulse and Pulse Width Modulation (PWM) circuits]

Many MOSFET circuits are designed to operate in systems where they are switched repetitively (such as DC-to-DC converters). Paralleled MOSFETs can be used as the switching elements in the system, but in addition to the guidelines set out for optimal steady state power sharing. Some additional points must be considered so that the MOSFETs share current during the switching transitions.

Good circuit and layout design is important. It influences the proportion of current carried by each MOSFET in the group during and after the switching event.

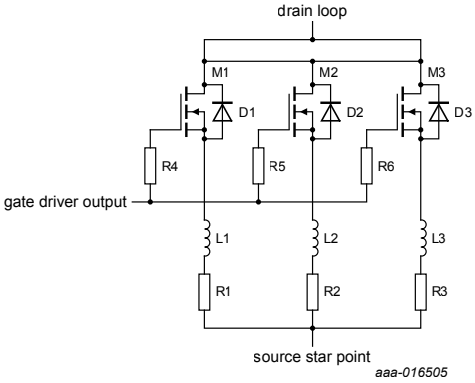
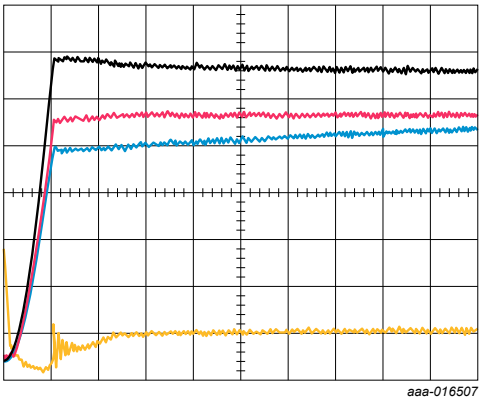
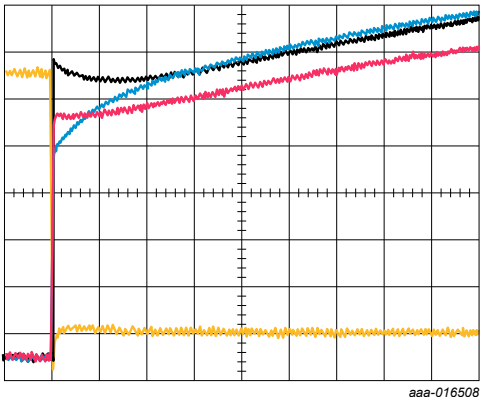


Fig 6. Schematic diagram showing the stray source inductances and source resistances



a. MOSFET drain current distribution immediately after turn on. The time base scale is 100 ns/division.



b. The same MOSFET drain current distribution as in **Figure 7**a showing the changes as time progress. The time base scale is 100 µs/division.

Fig 7. Oscilloscope plots showing the MOSFET drain currents (black, red and blue) and drain source voltage (yellow) after turn on

Figure 7a and **Figure 7**b show how the current distribution in three paralleled MOSFETs initially depends on the source inductances in the MOSFET current paths, namely L1, L2 and L3. As time progresses the resistances in the MOSFET current paths, namely $R_{DS(on)}$ + R1, $R_{DS(on)}$ + R2 and $R_{DS(on)}$ + R3 determine the current distribution.

The same principles hold about impedance matching of the current paths to the MOSFETs in the group. In this case, it is more important for the rates of change of current in the MOSFETs to match. The source inductances are the key impedance as they affect the gate-source voltages (gate drives) of the MOSFETs in the group.

This effect dominates more in high frequency and short duty cycle applications (e.g. switched-mode power supplies). It may be insignificant in lower frequency applications such as motor drives.

6.5 Partially enhanced (linear mode) power sharing

If a group of MOSFETs must operate in linear (partially enhanced) mode, great caution is needed. MOSFETs simply paralleled together as they are for fully enhanced conduction are very unlikely to share power or current well.

This behavior is due to the Negative Temperature Coefficient (NTC) of gate threshold voltage $V_{GS(th)}$. As the group of MOSFETs starts to enhance, the MOSFET with the lowest $V_{GS(th)}$ starts to conduct channel current first. It dissipates more power than the others and heat up more. Its $V_{GS(th)}$ decreases even further which causes it to enhance further.

This unbalanced heating causes the hottest MOSFETs to take a greater proportion of the power (and get even hotter). This process is unsustainable and can result in MOSFET failure if the power is not limited. Great care is needed when designing paralleled power MOSFET circuits that operate in the partially enhanced (linear mode) condition.

If all the MOSFETs in the group operate within their Safe Operating Area (SOA), they work reliably. The SOA must be adjusted for the worst case mounting base temperature that occurs in the application. Remember that the data sheet SOA graph applies only if the MOSFET mounting base temperature is 25 °C or less.

Adding external source resistors (R1 to R4 in the schematic; see **Figure 8**) provides the negative feedback needed for stable operation. The gate-source voltage applied to $V_{GS}(M1) = V_G - I_D(M1) \times R1$.

If the MOSFETs must also operate in fully enhanced mode (e.g. in ‘Hot Swap’ or ‘Soft Start’ applications), the inclusion of these resistors is an efficiency disadvantage.

As the MOSFET channel current increases, its gate drive voltage reduces.

As the MOSFETs are operating in partial enhancement (where MOSFET $R_{DS(on)}$ is not important), there is no adverse effect caused by including these resistors. If the MOSFETs must operate in both modes (as with active clamping after fully enhanced conduction), the inclusion of source resistors does have a negative impact.

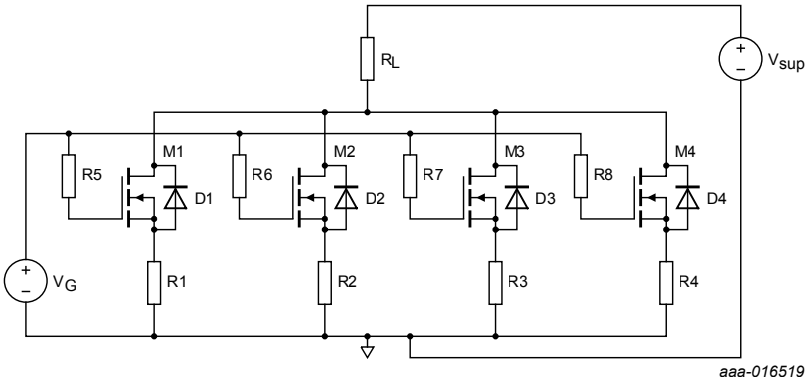


Fig 8. Schematic diagram of a group of four paralleled MOSFETs intended to operate in linear mode

MOSFETs developed specifically for linear mode operation are available from NXP. They can simplify the design of paralleled groups of MOSFETs intended for linear mode operation.

6.6 Gate drive considerations

It is preferable to fit low value gate resistors between the gate driver and the gate of each MOSFET in the group.

Their main function is to decouple the MOSFET gates from each other so they all receive similar gate drive signals. Without these resistors, at turn on the Miller plateau of the MOSFET with the lowest threshold voltage would act to clamp the gate-source voltages of the other MOSFETs in the group. This clamping effect tends to inhibit and delay the turning on of the other MOSFETs in the group. At turn off a similar process occurs.

Without these resistors, the MOSFET with the lowest threshold voltage would switch on first and switch off last. The consequences of this effect may be insignificant in low frequency high duty cycle applications. In higher frequency PWM applications, it could cause a significant power imbalance between the MOSFETs. Positive feedback also occurs in this case which increases the imbalance and could ultimately cause MOSFET failure.

Gate resistors also help to damp out oscillatory transients on V_{GS}. They also swamp any effects caused by variations in the internal gate resistance $R_{G(int)}$ of the MOSFETs.

6.6.1 Should individual gate drivers be used for each MOSFET in the group?

Using individual gate drivers for each MOSFET in the group is usually unnecessary. They may be necessary in applications where fast switching of a large group of large die MOSFETs is needed. Here the MOSFETs should be arranged in smaller sub groups, each sub group driven by an individual gate driver. Care should be taken to balance the circuit so the propagation delays of all the gate drivers are similar. This matching ensures that the switching of all the MOSFETs in the group is synchronized. Usually it is sufficient to drive the gate of each MOSFET in the group from the same gate driver. However, it is important to have a gate resistor between the gate driver output and the gate of each MOSFET as mentioned earlier.

6.7 MOSFET packaging considerations for paralleled groups

Conventionally packaged surface-mounted MOSFETs (DPAK and D2PAK) are the most widely available types so they are considered first for paralleled groups. However, KGD and LFPAK (power SO8) MOSFETs could offer better solutions.

6.7.1 Bare die (KGD) MOSFETs

These MOSFETs offer the densest and most flexible options for paralleled groups; they are designed to suit a specific application. The die aspect ratio and gate pad location can be designed specifically to suit the application. More source wire bonds can be fitted to the die than can be fitted in a conventionally packaged MOSFET, so overall $R_{DS(on)}$ can be reduced. Maximum drain current can be increased to achieve better performance from a paralleled group of MOSFETs. Special manufacturing facilities are required for KGD assembly.

6.7.2 LFPAK MOSFETs

The power SO8 (LFPAK) MOSFETs offer the opportunity to manufacture the paralleled MOSFET circuit conventionally. Higher component density and power capability are possible (approaching that of KGDs). The connections to the source and gate are made using copper clips which give better electrical and thermal performance than aluminum wire bonds in conventional packages.

6.8 Inductive energy dissipation in paralleled MOSFETs

6.8.1 Avalanching - low side MOSFET group driving a high side inductive load

If the group of paralleled MOSFETs is driving an inductive load, energy stored in this load must be safely dissipated when the current is switched off. A good way to manage this energy is to connect a 'freewheel diode' across the load; see **Figure 9**. Current flowing in the MOSFET channel diverts into the diode when the MOSFETs switch off and the energy is dissipated in the circuit resistances. However, it is not always possible and energy must then be dissipated safely in the MOSFETs.

If the battery polarity (V_{sup}) is reversed, the low impedance path through the freewheel diode and the body diode can carry large damaging currents. Freewheel diodes are often not used for this reason.

When the group of MOSFETs is switched off, the back e.m.f. from the inductive load may be high enough to cause the drain-source voltage across the group of MOSFETs to exceed the drain-source breakdown voltage $V_{(BR)DSS}$ of one of the MOSFETs. It likely that MOSFETs in the group have a range of $V_{(BR)DSS}$ values (even though they are the same type). The current then flows through the body diode of the MOSFET with the lowest $V_{(BR)DSS}$ in reverse (avalanche) conduction. This condition causes high-power dissipation and temperature rise in the MOSFET die ($P = I_D \times V_{(BR)DSS}$). If the maximum 175 °C junction temperature is exceeded, the thermal stress on the die could degrade or destroy the MOSFET.

In the worst case, all the current which was flowing through the group of MOSFETs could be diverted into the body diode of one MOSFET in the group. If this scenario is possible, it is vital that a single MOSFET in the group can safely handle the total avalanche current under worst case thermal conditions. $V_{(BR)DSS}$ has a positive temperature coefficient which tends to redistribute the current towards other MOSFETs with higher $V_{(BR)DSS}$ values.

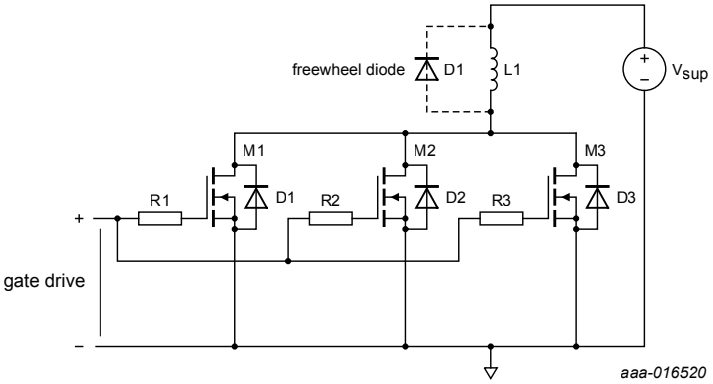


Fig 9. Low side MOSFET group driving a high side inductive load

6.8.2 Active clamping - high side MOSFET group driving a low side inductive load

This configuration (see **Figure 10**) is often used in automotive applications. This topology is useful because the vehicle chassis can be used as the negative supply return path to the battery.

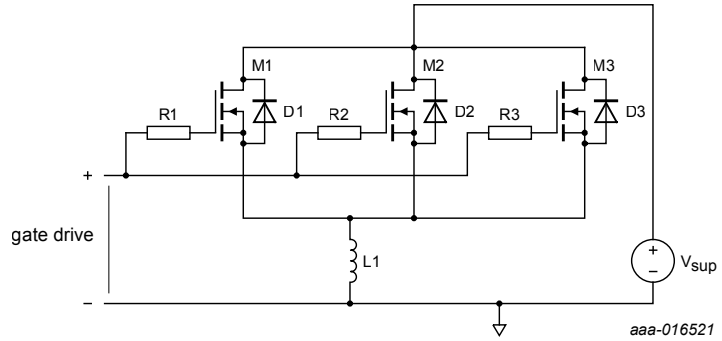


Fig 10. High side MOSFET group driving a low side inductive load

In this circuit, the difference between the threshold voltages rather than $V_{(BR)DSS}$ spread determines where the load current flows. The MOSFET with the lowest threshold voltage conducts the greatest proportion of the current. The drain-source voltage across the MOSFET group is $V_{sup} + V_{GS}$ and the power dissipation of the group is $(V_{sup} + V_{GS}) \times I_D$. As with the avalanche case, all the current (and hence all the power dissipation) could be diverted into a single MOSFET in the group.

This situation is worse than the avalanche case because MOSFET threshold voltage has a negative temperature coefficient. This characteristic tends to direct the current flow initially to the hottest MOSFET. This MOSFET then gets even hotter so that it retains the current.

6.9 Summary

1. It is better to use a single large MOSFET rather than a group of smaller MOSFETs.
2. The power capability of a group of n MOSFETs never achieves n times the power capability of a single MOSFET.
3. If it is necessary to use paralleled MOSFETs, use the lowest number possible as the basic group size (3 maximum).
4. If a larger number is needed, use a group of basic groups i.e. 4 = 2 groups of 2; 6 = 2 groups of 3.
5. The circuit layout is a very important factor determining how well a group of paralleled MOSFETs share power dissipation, particularly in higher frequency repetitive switching circuits.
6. Consider LFPAKs (for repetitive switching applications) because of their small size, good thermal performance and low package impedances.
7. Special care is needed when designing groups of MOSFETs that could operate in avalanche or active clamping mode.

Chapter 7: Designing RC snubbers

Chapter 7: Designing RC Snubbers

7.1 Introduction

This chapter describes the design of a simple “RC snubber circuit”. The snubber is used to suppress high-frequency oscillations associated with reverse recovery effects in power semiconductor applications

7.2 Test circuit

The basic circuit is a half-bridge and shown in **Figure 1**.

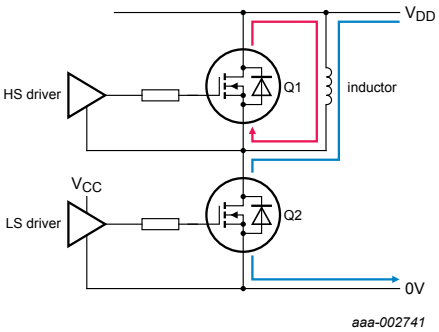


Fig 1. The half-bridge circuit

Q1 and Q2 are BUK761R6-40E devices. The inductor could also be connected to 0 V rather than V_{DD}.

Inductor current is established in the red loop; Q2 is off and current is flowing through Q1 body diode. When Q2 is turned on, current “commutates” to the blue loop and the reverse recovery effect occurs in Q1. We observe the effect of Q1 reverse recovery on the V_{DS} waveform of Q2; see **Figure 2**.

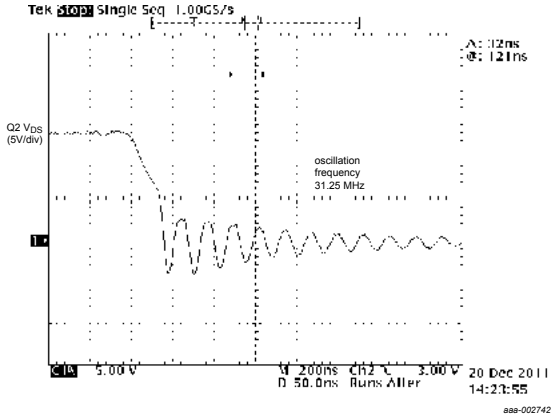


Fig 2. Reverse recovery-induced oscillation in Q2 V_{DS}

The equivalent circuit is shown in **Figure 3**.

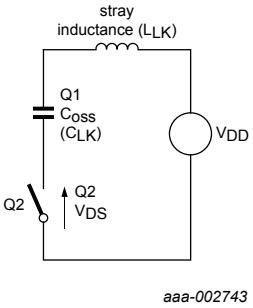


Fig 3. Equivalent circuit

We are primarily interested in the parasitic elements in the circuit:

- L_{LK} is the total stray or “leakage” inductance comprised of PCB trace inductance, device package inductance, etc.
- The parasitic capacitance C_{LK} is mainly due to C_{oss} of the upper (Q1) device.

Q2 is treated as a simple switch. The oscillation can be eliminated (snubbed) by placing an RC circuit across Q1 drain-source; see **Figure 4**.

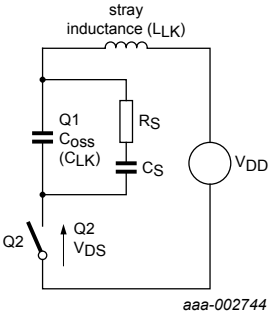


Fig 4. Equivalent circuit with snubber components R_S and C_S

7.3 Determining C_{LK} and L_{LK}

Before we can design the snubber, we must first determine C_{LK} and L_{LK}. We could attempt to measure C_{LK} and L_{LK} directly, but a more elegant method can be used. For this LC circuit, we know that:

(1) $$f_{RING0} = \frac{1}{2\pi\sqrt{L_{LK}C_{LK}}}$$

where f_{RING0} is the frequency of oscillation without a snubber in place; see **Figure 2**. If we add an extra additional capacitor across Q1 (C_{add}), the initial oscillation frequency from f_{RING0} to f_{RING1} ($f_{RING1} < f_{RING0}$) will change. It can be shown that (see **Section 7.7** "**Appendix A; determining CLK from Cadd, fRING0 and fRING1**"):

(2) $$C_{LK} = \frac{C_{add}}{x^2 - 1}$$

where:

(3) $$x = \frac{f_{RING0}}{f_{RING1}}$$

So if we measure f_{RING0} (without C_{add}), then add a known C_{add} and measure f_{RING1}, we can determine C_{LK} and L_{LK} (two equations, two unknowns).

C_{add} = 3200 pF was added in circuit, and fRING1 found to be 22.2 MHz (f_{RING0} previously found to be 31.25 MHz; see **Figure 2**).

from **Equation 3**:

$$x = \frac{31.25}{22.2} = 1.41 \quad (4)$$

and from **Equation 2**:

$$C_{LK} = \frac{3200pF}{1.41^2 - 1} = 3239pF \quad (5)$$

Rearranging **Equation 1**:

$$L_{LK} = \frac{1}{(2\pi f_{RING0})^2 C_{LK}} \quad (6)$$

So with f_{RING0} = 31.25 MHz and C_{LK} = 3239 pF:

$$L_{LK} = \frac{1}{(2 \times \pi \times 3.125 \times 10^7)^2 \times 3.239 \times 10^{-9}} = 8.01 \times 10^{-9} H = 8.0nH \quad (7)$$

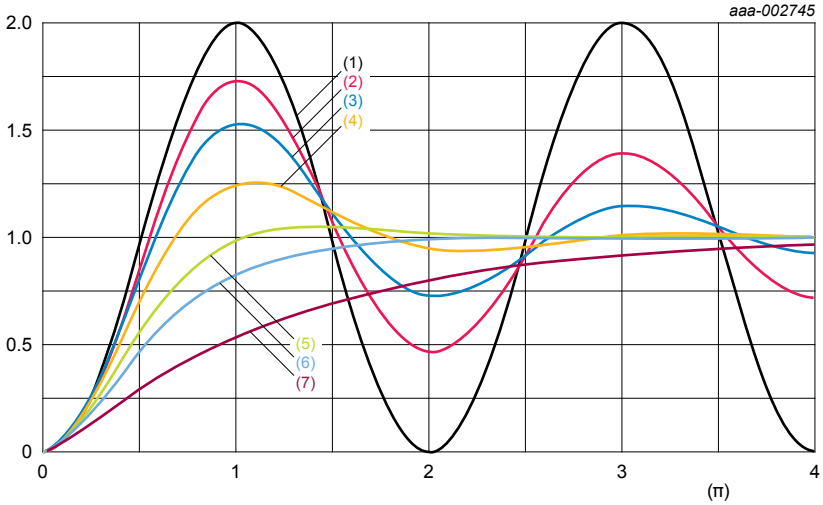
and with f_{RING1} = 22.2 MHz and (C_{LK} + C_{add}) = 3239 pF + 3200 pF = 6439 pF:

$$L_{LK} = \frac{1}{(2 \times \pi \times 2.22 \times 10^7)^2 \times 6.439 \times 10^{-9}} = 7.98 \times 10^{-9} H = 8.0nH \quad (8)$$

In other words, the calculated value of L_{LK} remains almost unchanged when we add the additional 3200 pF capacitance. This is a good sanity check of the method for determining C_{LK} and L_{LK}.

7.4 Designing the snubber - theory

If we replace C_S in **Figure 4** with a short-circuit, then we simply have the classic RLC circuit found in text books. The response of this circuit to a step change in voltage (that is Q2 turning on) depends on the degree of damping (ζ or zeta) in the circuit; see **Figure 5**.



(1) ζ = 0.

(2) ζ = 0.1.

(3) ζ = 0.2.

(4) ζ = 0.4.

(5) ζ = 0.7.

(6) ζ = 1.

(7) ζ = 2.

Fig 5. Step response of an RLC circuit for various values of zeta (ζ)

In theory the circuit oscillates indefinitely if ζ = zero, although this is a practical impossibility as there is always some resistance in a real circuit. As ζ increases towards one, the oscillation becomes more damped that is, tends to decrease over time with an exponential decay envelope. This is an "underdamped" response. The case ζ = one is known as "critically damped" and is the point at which oscillation just ceases. For values of greater than one (overdamped), the response of the circuit becomes more sluggish with the waveform taking longer to reach its final value. There is therefore more than one possible degree of damping which we could build into a snubber, and choice of damping is therefore part of the snubber design process.

For this configuration of RLC circuit, the relationship between ζ, R_S, L_{LK} and C_{LK} is:

(9) $$\varsigma = \left(\frac{1}{2R_S}\right)\sqrt{\frac{L_{LK}}{C_{LK}}}$$

The snubber capacitor C_S does not appear in **Equation 9**.

In some circuits, it is possible to damp the oscillations with R_S alone. However, in typical half-bridge circuits we cannot have a resistor mounted directly across Q1 drain source. If we did, then Q1 is permanently shorted by the resistor and the circuit as a whole would not function as required. The solution is therefore to put C_S in series with R_S, with the value of C_S chosen so as not to interfere with normal operation.

The snubber is a straightforward RC circuit whose cut-off frequency f_C is:

(10) $$F_C = \frac{1}{2\pi R_S C_S}$$

Again, we must choose which value of f_C to be used, and there is no single correct answer to this question. The cut-off frequency of the snubber must be low enough to effectively short-circuit the undamped oscillation frequency f_{RING0}, but not so low as to present a significant conduction path at the operating frequency of the circuit (for example 100 kHz or whatever). A good starting point has been found to be $f_C = f_{RING0}$.

7.5 Designing the snubber - in practice

We now have sufficient information to design a snubber for the waveform shown in **Figure 2**. To recap:

C_{LK} = 3239 pF

L_{LK} = 8.0 nH

f_{RING0} = 31.25 MHz

(11) $$\varsigma = \left(\frac{1}{2R_S}\right)\sqrt{\frac{L_{LK}}{C_{LK}}}$$

(12) $$F_C = \frac{1}{2\pi R_S C_S} = f_{RING0}$$

The first task is to choose a value of damping (**Figure 5**). We have chosen $\zeta = 1$, that is, critical damping. Rearranging **Equation 11** we have:

(13) $$R_S = \left(\frac{1}{2\zeta}\right)\sqrt{\frac{L_{LK}}{C_{LK}}} = \left(\frac{1}{2}\right)\sqrt{\frac{8.0\times10^{9}}{3.239\times10^{-9}}} = 0.78\Omega$$

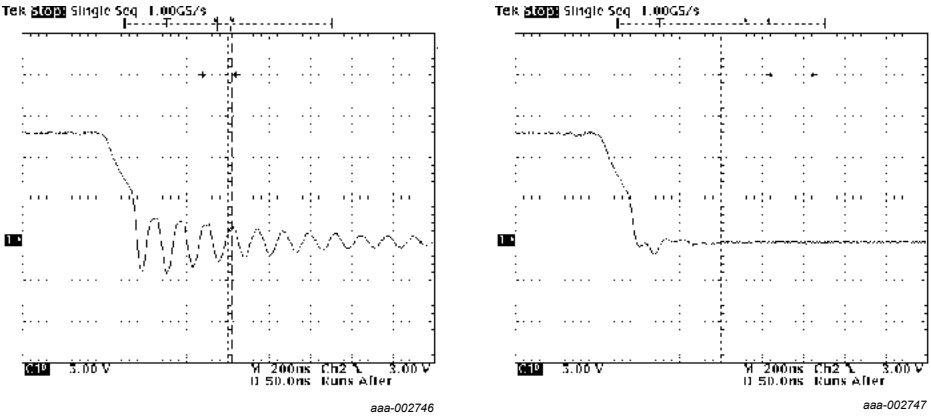
use 2 × 1.5 Ω in parallel to give 0.75 Ω.

Rearranging **Equation 12** we have:

(14) $$C_S = \frac{1}{2\pi R_S f_{RING0}} = \frac{1}{2\times\pi\times0.75\times3.125\times10^{7}} = 6.79nF$$

use 4.7 nF + 2.2 nF to give 6.9 nF.

The snubber was fitted across Q1 drain source. The resulting waveform is shown in **Figure 6** together with the original (non-snubbed) waveform from **Figure 2**



a. Without snubber

b. With snubber

Vertical scale is 2 V/div.

Fig 6. Q2 V_{DS} waveform with and without snubber

As seen in **Figure 6**, the snubber has almost eliminated the ringing in the V_{DS} waveform. This technique could also be applied to the MOSFET in the Q2 position.

7.6 Summary

- Reverse recovery effects in power devices can induce high frequency oscillations in devices connected to them.
- A common technique for suppressing the oscillations is the use of an RC snubber.
- Design of an effective snubber requires the extraction of the circuit parasitic capacitance and inductance. A method has been demonstrated for doing this.
- The snubbed circuit has been shown to be a variation on the classic RLC circuit.
- A method of determining values of snubber components has been demonstrated. The method has been shown to work well, using the example of BUK761R6-40E MOSFETs.

7.7 Appendix A; determining C_{LK} from C_{add}, f_{RING0} and f_{RING1}

We know that:

(15) $$f_{RING0} = \frac{1}{2\pi\sqrt{L_{LK}C_{LK}}}$$

where f_{RING0} is the frequency of oscillation without a snubber in place and L_{LK} and C_{LK} are the parasitic inductances and capacitances respectively.

If we add capacitor C_{add} across Q1 drain-source, f_{RING0} is reduced by an amount "x" where:

We know that:

(16) $$\frac{f_{RING0}}{x} = \frac{1}{2\pi\sqrt{L_{LK}(C_{LK}+C_{add})}}$$

therefore

(17) $$\frac{1}{2\pi\sqrt{L_{LK}C_{LK}}} = \frac{x}{2\pi\sqrt{L_{LK}(C_{LK}+C_{add})}}$$

(18) $$\frac{1}{\sqrt{L_{LK}C_{LK}}} = \frac{x}{\sqrt{L_{LK}(C_{LK}+C_{add})}}$$

(19) $$\sqrt{L_{LK}C_{LK}} = \frac{\sqrt{L_{LK}(C_{LK}+C_{add})}}{x}$$

(20) $$C_{LK} = \frac{C_{LK}+C_{add}}{X^2}$$

(21) $$C_{LK}x^2 - C_{LK} = C_{add}$$

(22) $$C_{LK}(x^2-1) = C_{add}$$

(23) $$C_{LK} = \frac{C_{add}}{x^2-1}$$

where:

(24) $$x = \frac{f_{RING0}}{f_{RING1}}$$

Chapter 8: Failure signature of electrical overstress on power MOSFETs

Chapter 8: Failure signature of electrical overstress on power MOSFETs

8.1 Introduction

Power MOSFETs are used to switch high voltages and currents, while minimizing their own internal power dissipation. Under fault conditions however, it is possible to apply voltage, current and power exceeding the MOSFET capability. Fault conditions can be either due to an electrical circuit failure or a mechanical fault with a load such as a seized motor. This leads to Electrical Overstress (EOS). Typically the consequence of EOS is the short circuiting of at least 2 of the 3 MOSFET terminals (gate, drain, source). In addition, high local power dissipation in the MOSFET leads to MOSFET damage which manifests as burn marks, die crack and in extreme cases as plastic encapsulation damage.

Examination of the size and location of the burn mark, the failure signature, provides information about the type of fault condition which caused the failure. Common fault conditions are:

- ElectroStatic Discharge (ESD)
- Unclamped Inductive Switching (UIS) - commonly called Avalanche or Ruggedness
- Linear Mode operation
- Over-current

Packaged MOSFETs have been deliberately destroyed under these conditions. Images recorded of the ensuing burn marks on the silicon surface, provide a ‘Rogue’s Gallery’ to aid the explanation of EOS failures.

Section 8.1.1 to **Section 8.1.5** gives an overview of the common failure signatures.

Appendices in **Section 8.2.1** to **Section 8.2.15** provide further images.

8.1.1 ESD - Machine Model

8.1.1.1 EOS method

ESD pulses were applied using a standard Machine Model ESD circuit; for details see *AEC - Q101-002 - REV-A - July 18, 2005*. Voltage of the applied pulse was progressively increased until device failure was observed.

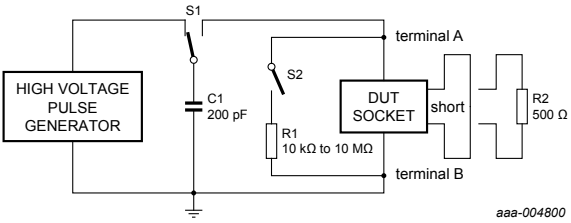


Fig 1. Typical circuit for Machine Model ESD simulation

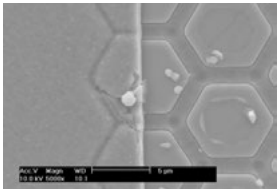
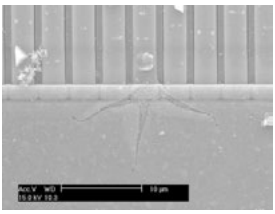
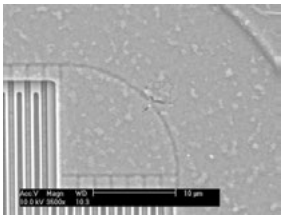
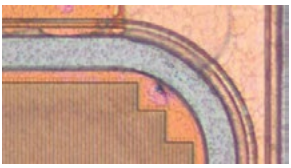
8.1.1.2 Fault condition simulated

Machine model ESD simulates situations when a voltage spike is applied to the MOSFET exceeding the maximum voltage that can be sustained by the gate oxide between either gate-source or gate-drain. The pulse is applied with minimal series resistance between the voltage origin and the MOSFET, resulting in rapid rise of the MOSFET gate voltage. Electrical test equipment or malfunctioning circuits can easily apply such voltage pulses.

8.1.1.3 Signature

An edge cell of the MOSFET structure is a failure site that is normally located close to the gate. Outer edge cells and cells near the gate are the first to be subjected to the incoming voltage pulse. As a result, these cells are the first sites where the voltage exceeds the gate-oxide capability.

Table 1. Examples of Machine Model ESD failure signature

Device name	Cell pitch (µm)	Image	Comments
BUK9508-55A	9 (hexagon)	 aaa-004801	Fail site is gate oxide of edge cell; see **Section 8.2.1 "Machine model EOS of BUK9508-55A"** for further images
BUK9Y40-55B	4 (stripe)	 aaa-004803	Fail site is gate oxide of edge cell; see **Section 8.2.2 "Machine model EOS of BUK9Y40-55B"** for further images
PSMN7R0-30YL	2 (stripe)	 aaa-004853	Fail site is gate oxide of edge cell; see **Section 8.2.3 "Machine model EOS of PSMN7R0-30YL"** for further images
PSMN011-30YL	2 (stripe)	 aaa-004854	Fail site is gate oxide of edge cell; see **Section 8.2.4 "Machine model EOS of PSMN011-30YL"** for further images

8.1.2 ESD - Human body model

8.1.2.1 EOS method

ESD pulses were applied using a standard Human-body Model ESD circuit; for details see *AEC - Q101 - REV - May 15, 1996*. Voltage of the applied pulse was progressively increased until device failure was observed.

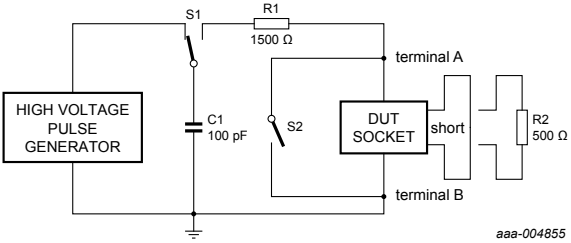


Fig 2. Typical circuit for Human body Model ESD simulation

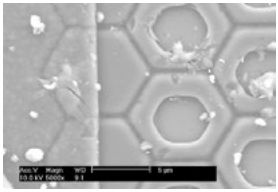
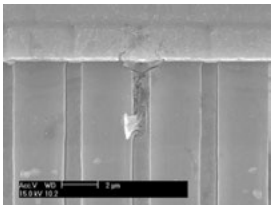
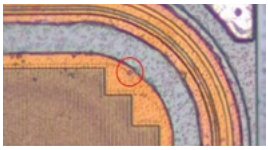
8.1.2.2 Fault condition simulated

Human body model ESD simulates situations when a voltage spike is applied to the MOSFET exceeding the maximum voltage that can be sustained by the gate oxide of either gate-source or gate-drain. The pulse is applied with 1500 Ω series resistance between the voltage origin and the MOSFET, which limits the rate of rise of the MOSFET gate voltage. Either human handling, electrical test equipment or malfunctioning circuits can easily apply such voltage pulses.

8.1.2.3 Signature

Failure site is found in an edge cell of the MOSFET structure. Outer edge cells and cells near the gate are the first to be subjected to the incoming voltage pulse and are thus the first sites where the voltage exceeds the gate-oxide capability. The signature differs from Machine Model failures in that the fail site does not show such a strong tendency to group near the gate, due to the slower rise in gate voltage.

Table 2. Examples of Human Body Model ESD failure signature

Device name	Cell pitch (µm)	Image	Comments
BUK9508-55A	9 (hexagon)	 aaa-004856	Fail site is gate oxide of edge cell; see **Section 8.2.5 "Human body model EOS of BUK9508-55A"** for further images
BUK9Y40-55B	4 (stripe)	 aaa-004857	Fail site is gate oxide of edge cell; see **Section 8.2.6 "Human body model EOS of BUK9Y40-55B"** for further images
PSMN011-30YL	2 (stripe)	 aaa-004858	Fail site is gate oxide of edge cell; see **Section 8.2.7 "Human body model EOS of PSMN011-30YL"** for further images

8.1.3 Unclamped Inductive Switching (UIS) (Avalanche or Ruggedness)

8.1.3.1 EOS method

Inductive energy pulses were applied using a standard UIS circuit; for details see *AEC - Q101-004 - REV - May 15, 1996*. A fixed inductance value is elected. Current in the inductance prior to switching the MOSFET was progressively increased until device failure was observed.

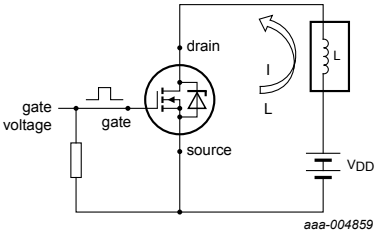


Fig 3. Circuit diagram for UIS ruggedness test

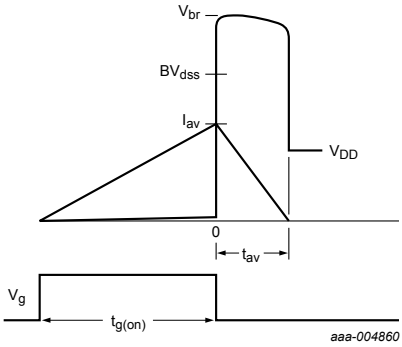


Fig 4. Waveforms obtained from UIS test

8.1.3.2 Fault condition simulated

UIS simulates situations when a MOSFET is switched off in a circuit in which there is inductance. The inductance can be deliberate (such as an injector coil in a diesel engine system), or parasitic. As the current cannot decay to zero instantaneously through the inductance, the MOSFET source-drain voltage increases to take the device into avalanche breakdown. The energy stored in the inductance is then dissipated in the MOSFET.

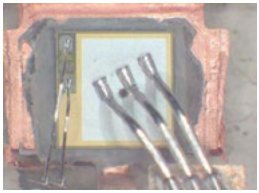
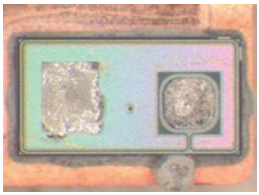
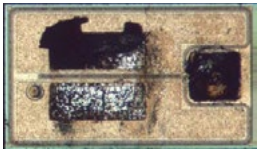
8.1.3.3 Signature

Failure site is found in an active MOSFET cell. The burn-mark is usually round in shape, indicating a central failure site and subsequent thermal damage.

If the avalanche event is long in duration (~ ms), then burn marks locate at central sites on the die, where there is maximum current flow and reduced heat dissipation. The sites are often adjacent to wire bonds/clip bonds where current density is high, but not directly under the wire bond/clip bond as it provides a local heat sink. Failure is at the hottest location of the die.

For short avalanche events (~ µs), the burn marks can take on more random locations over the die surface. The temperature rise in the chip is more uniform with negligible chance for current crowding and local heating on these time scales. For even shorter avalanche events, the burn marks can locate at die corners due to the discontinuity in cell structure at these locations.

Table 3. Examples of unclamped inductive switching failure signature

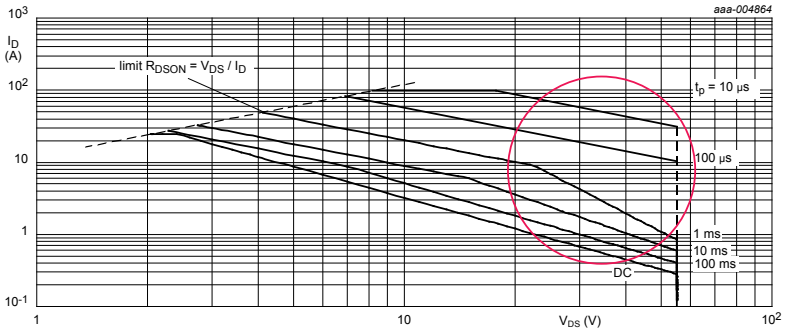
Device name	Cell pitch (µm)	Image	Comments
BUK7L06-34ARC	9 (hexagon)	 aaa-004861	round burn in active area; see **Section 8.2.8 "Unclamped inductive switching EOS of BUK7L06-34ARC"** for further images
BUK9Y40-55B	4 (stripe)	 aaa-004862	round burn in active area; see **Section 8.2.9 "Unclamped Inductive Switching EOS of BUK9Y40-55B"** for further images
PSMN7R0-30YL	2 (stripe)	 aaa-004863	round burn in active area; see **Section 8.2.10 "Unclamped inductive switching EOS of PSMN7R0-30YL"** for further images

8.1.4 Linear mode operation

8.1.4.1 EOS method

A Safe Operating Area (SOA) graph is included in all power MOSFET data sheets. Outside the defined safe region, the power dissipated in the FET cannot be removed, resulting in heating beyond the device capability and then device failure.

MOSFETs were taken and a fixed source-drain voltage applied. Current pulses of defined duration were applied and the current was increased until MOSFET failure was observed.



T_{mb} = 25 °C; I_{DM} is a single pulse.

Fig 5. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

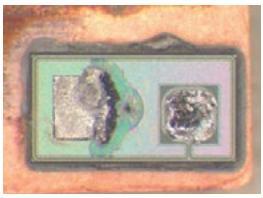
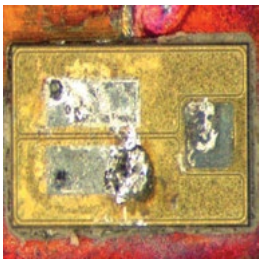
8.1.4.2 Fault condition simulated

Linear mode operation is common during device switching or clamped inductive switching and is not a fault condition unless the SOA is exceeded. Linear mode EOS simulates situations when a MOSFET is operated in Linear mode for too long. This situation can also occur if, when intending to turn the FET on, the gate signal voltage to the FET is too low. This condition can also arise when intending to hold the FET in the Off-state with high drain-source voltage. If the gate connection is lost, the gate voltage capacitively rises and the same Linear mode fault condition occurs.

8.1.4.3 Signature

The hottest location of the die is a failure site that is usually at central sites on the die. The center of the die is where there is maximum current flow and reduced heat dissipation. The sites are often adjacent to wire bonds/clip bonds where current density is high, but not directly under the wire bond/clip bond as it provides a local heat sink.

Table 4. Examples of linear mode failure signature

Device name	Cell pitch (µm)	Image	Comments
BUK7L06-34ARC	9 (hexagon)	 aaa-004865	Burns located in center of die adjacent to wire-bonds; see **Section 8.2.11 "Linear mode EOS of BUK7L06-34ARC"** for further images
BUK9Y40-55B	4 (stripe)	 aaa-004866	Burn adjacent to location of clip bond in center of die; see **Section 8.2.12 "Linear mode EOS of BUK9Y40-55B"** for further images
PSMN7R0-30YL	2 (stripe)	 aaa-004867	Burn adjacent to location of clip bond in center of die; see **Section 8.2.13 "Linear mode EOS of PSMN7R0-30YL"** for further images

8.1.5 Over-current

8.1.5.1 EOS method

The maximum current-handling capability is specified on the data sheet for Power MOSFETs. This capability is based on the current handling capability of wires or clips, before which fusing will onset, combined with the ability to dissipate heat. Exceeding this rating can result in catastrophic failure.

I_D	drain current	V_{GS} = 10 V; T_{mb} = 100 °C; see Figure 1	-	53	A
		V_{GS} = 10 V; T_{mb} = 25 °C; see Figure 1	-	76	A
I_{DM}	peak drain current	$t_p \leq 10$ µs; pulsed; T_{mb} = 25 °C; see Figure 3	-	260	A

aaa-005071

Fig 6. Example of maximum current rating from the data sheet of PSMN7R0-30YL

8.1.5.2 Fault condition simulated

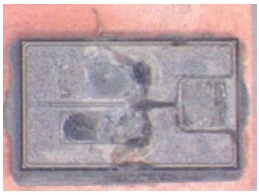
Over-current occurs if a FET is turned on with no element in the circuit to limit the current, resulting in a supply voltage being applied fully over the drain-source terminals of the FET. Typically this occurs if a load has been short-circuited. Alternatively if 2 FETs are operating in a half-bridge, over-current can ensue if both are turned on together.

8.1.5.3 Signature

Failure site is initially where the current handling connections (wires or clips) meet the die. Normally damage is extensive however in over-current conditions, and spreads over the entire die surface with evidence of melted metallization and solder joints.

For wire-bonded packages, there is often evidence of fused wires. For clip-bonded packages, die crack is commonly observed.

Table 5. Examples of over-current failure signature

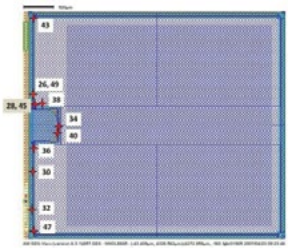
Device name	Cell pitch (µm)	Image	Comments
BUK7L06-34ARC	9 (hexagon)	 aaa-004868	Burns located in center of die adjacent to wire-bonds. Secondary damage of remelted top metal and solder die attach; see **Section 8.2.14 "Over-current EOS of BUK7L06-34ARC"** for further images
PSMN7R0-30YL	2 (stripe)	 aaa-004869	Burn adjacent to location of clip bond in center of die; see **Section 8.2.15 "Over-current EOS of PSMN7R0-30YL"** for further images

8.2 Appendices

8.2.1 Machine model EOS of BUK9508-55A

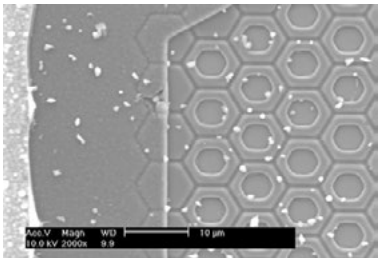
Table 6. Machine model EOS

BUK9508-55A	
Cell structure:	9 mm hexagons
Package:	TO-220
Die size:	5.5 mm x 4.5 mm
EOS condition:	1.1 kV MM pulse



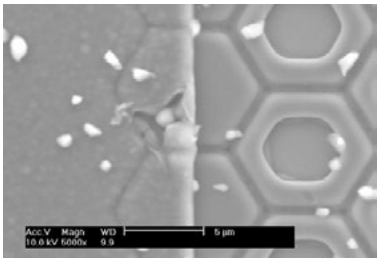
aaa-004875

Fails located in edge cells, in the vicinity of the gate contact



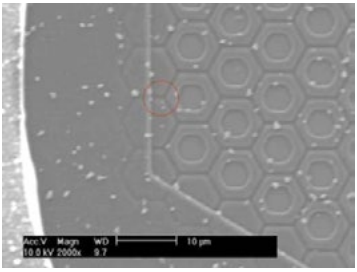
aaa-004876

Fig 7. Sample image 43; after Al removal



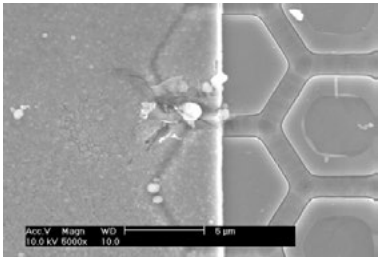
aaa-004877

Fig 8. Sample image 43; after Al removal, close-up



aaa-004878

Fig 9. Sample image 47; after Al removal, no visible damage at hot spot



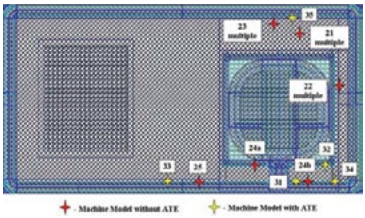
aaa-004879

Fig 10. Sample image 47; after TEOS removal, close-up

8.2.2 Machine model EOS of BUK9Y40-55B

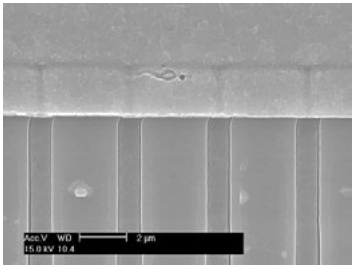
Table 7. Machine model EOS

BUK9Y40-55B	
Cell structure:	4 µm stripe
Package:	LFPAK (clip bond)
Die size:	2.5 mm x 1.35 mm
EOS condition:	200 V to 240 V MM pulse



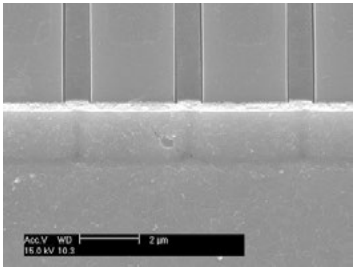
aaa-004880

Fails located mostly in edge cells, in the vicinity of the gate contact. Some fails subjected to ATE testing to create additional damage to highlight fail site



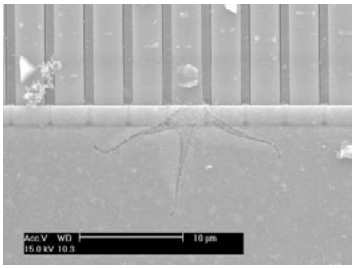
aaa-004881

Fig 11. Sample image 24; after TEOS removal



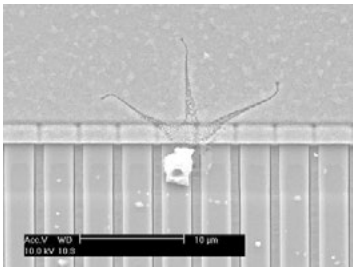
aaa-004882

Fig 12. Sample image 25; after TEOS removal



aaa-004883

Fig 13. Sample image 31; after ATE testing and after TEOS removal



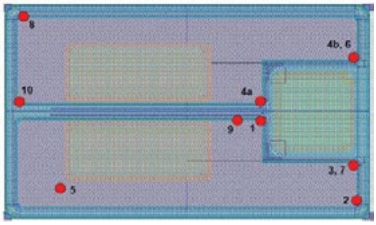
aaa-004884

Fig 14. Sample image 32; after ATE testing and after TEOS removal

8.2.3 Machine model EOS of PSMN7R0-30YL

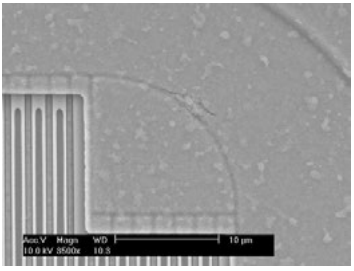
Table 8. Machine model EOS

PSMN7R0-30YL	
Cell structure:	2 µm stripe
Package:	LFPAK (clip bond)
Die size:	2.5 mm x 1.35 mm
EOS condition:	200 V to 270 V MM pulse



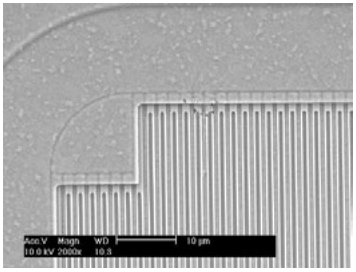
aaa-004885

Fails located mostly in edge cells, in the vicinity of the gate contact



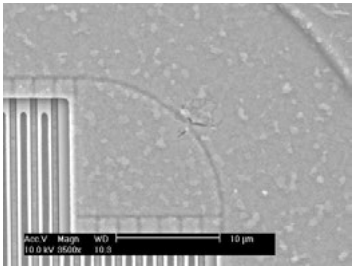
aaa-004886

Fig 15. Sample image 1; after TEOS removal



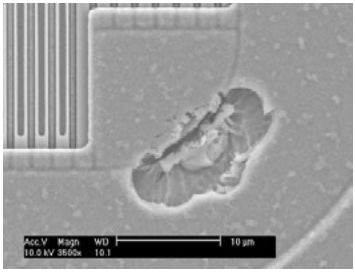
aaa-004887

Fig 16. Sample image 8; after TEOS removal



aaa-004888

Fig 17. Sample image 3; after TEOS removal



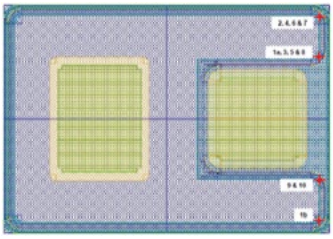
aaa-004889

Fig 18. Sample image 6; after TEOS removal

8.2.4 Machine model EOS of PSMN011-30YL

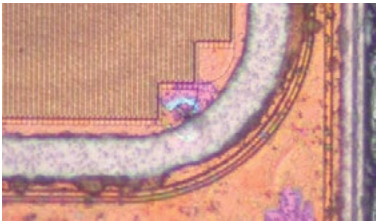
Table 9. Machine model EOS

PSMN011-30YL	
Cell structure:	2 µm stripe
Package:	LFPAK (clip bond)
Die size:	1.7 mm x 1.2 mm
EOS condition:	200 V to 210 V MM pulse



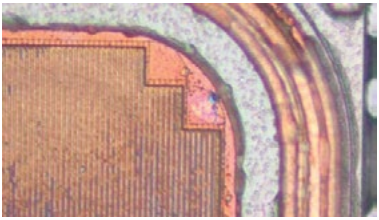
aaa-004890

Fails located mostly in corner edge cells, in the vicinity of the gate contact



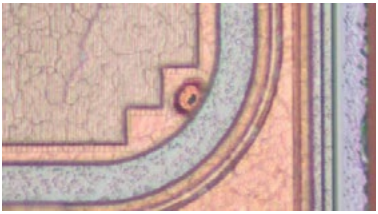
aaa-004891

Fig 19. Sample image 3; after Al removal



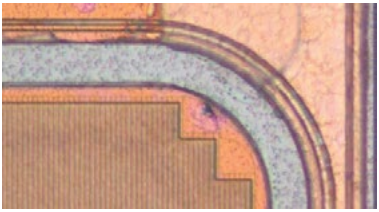
aaa-004892

Fig 20. Sample image 6; after Al removal



aaa-004893

Fig 21. Sample image 8; after Al removal



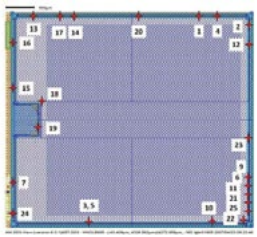
aaa-004894

Fig 22. Sample image 10; after Al removal

8.2.5 Human body model EOS of BUK9508-55A

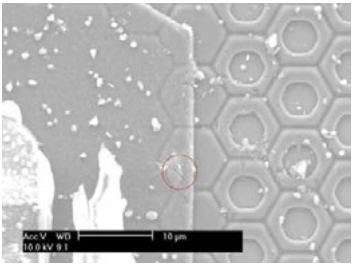
Table 10. Human body model EOS

BUK9508-55A	
Cell structure:	9 mm hexagons
Package:	TO-220
Die size:	5.5 mm x 4.5 mm
EOS condition:	5 kV HBM pulse



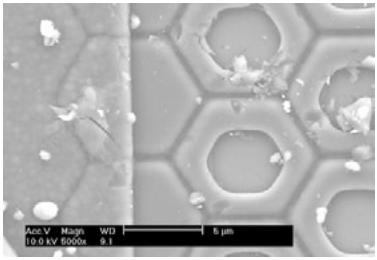
aaa-004899

Fails located in edge cells, distributed around edge of device



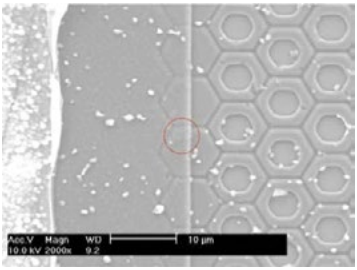
aaa-004900

Fig 23. Sample image 4; after Al removal



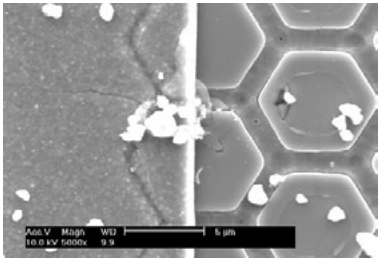
aaa-004901

Fig 24. Sample image 4; after Al removal, close-up



aaa-004902

Fig 25. Sample image 19; after Al removal



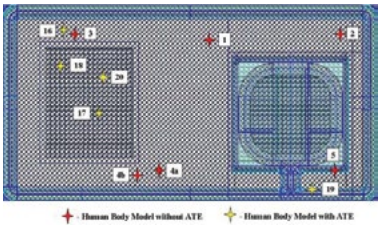
aaa-004903

Fig 26. Sample image 19; after TEOS removal, close-up

8.2.6 Human body model EOS of BUK9Y40-55B

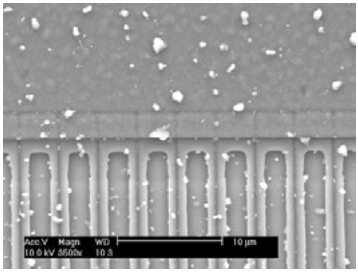
Table 11. Human body model EOS

BUK9Y40-55B	
Cell structure:	4 µm stripe
Package:	LFPAK (clip bond)
Die size:	2.5 mm x 1.35 mm
EOS condition:	450 V to 650 V HBM pulse



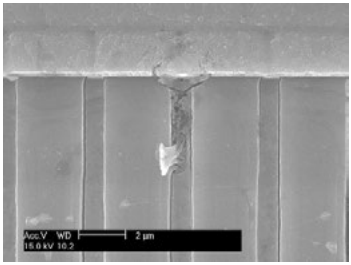
aaa-004904

Fails located randomly over die with increased grouping in edge cells. Some fails subjected to ATE testing to create additional damage to highlight fail site



aaa-004905

Fig 27. Sample image 5; after Al removal



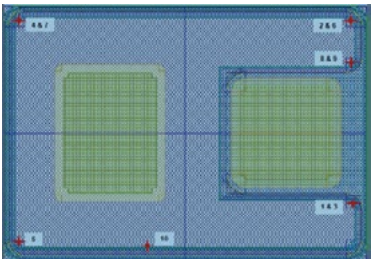
aaa-004906

Fig 28. Sample image 5; after TEOS removal, close-up

8.2.7 Human body model EOS of PSMN011-30YL

Table 12. Human body model EOS

PSMN011-30YL	
Cell structure:	2 µm stripe
Package:	LFPAK (clip bond)
Die size:	1.7 mm x 1.2 mm
EOS condition:	200 V to 210 V HBM pulse



aaa-004907

Fails located in edge cells

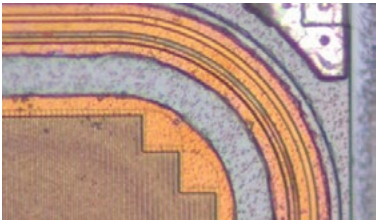


Fig 29. Sample image 2; after Al removal

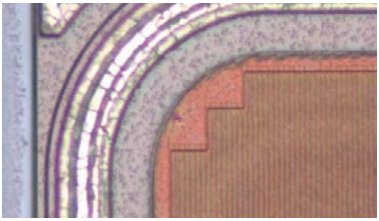


Fig 30. Sample image 4; after Al removal

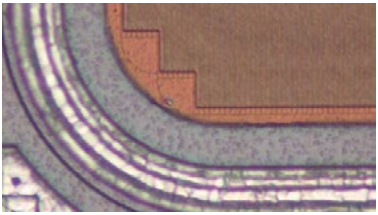


Fig 31. Sample image 5; after Al removal

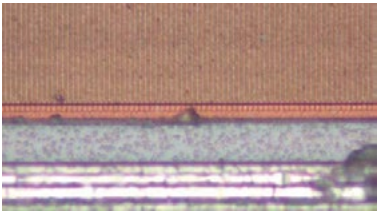
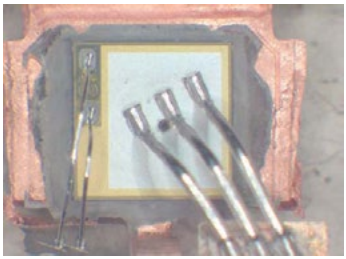


Fig 32. Sample image 10; after Al removal

8.2.8 Unclamped inductive switching EOS of BUK7L06-34ARC

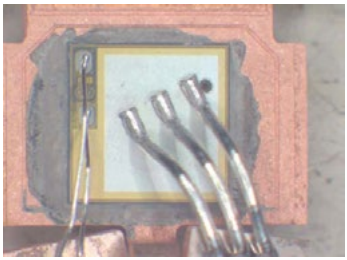
Table 13. Unclamped inductive switching EOS

BUK7L06-34ARC		
Cell structure:	9 mm hexagons	Small round burn marks, randomly distributed over active area, close to but not directly under wire-bonds
Package:	TO-220 (clip bond)	
Die size:	4.3 mm x 4.3 mm	
EOS condition:	0.2 mH; 80 A to 110 A	



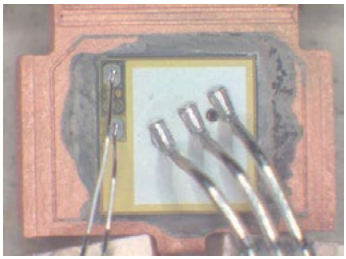
aaa-004912

Fig 33. Sample image 1



aaa-004913

Fig 34. Sample image 2



aaa-004914

Fig 35. Sample image 3

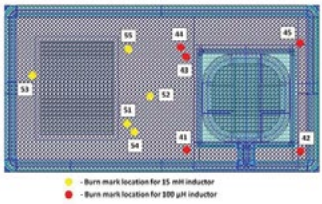
aaa-004915

Fig 36. Sample image 4

8.2.9 Unclamped Inductive Switching EOS of BUK9Y40-55B

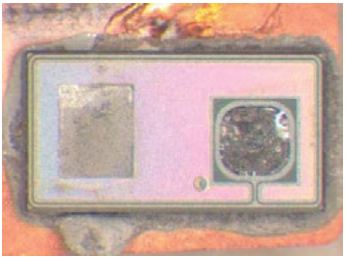
Table 14. Unclamped inductive switching EOS

BUK9Y40-55B	
Cell structure:	4 µm stripe
Package:	LFPAK (clip bond)
Die size:	2.5 mm x 1.35 mm
EOS condition:	Red dots: 0.1 mH, 76 A to 80 A Yellow dots: 15 mH, 7 A to 9 A



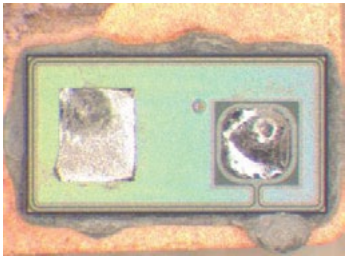
aaa-004916

Small round burn marks, randomly distributed over active area, close to but not directly under clip bond



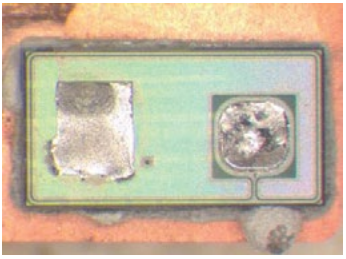
aaa-004917

Fig 37. Sample image 41; 0.1 mH



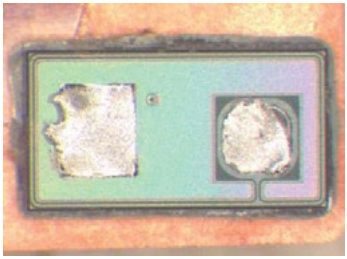
aaa-004918

Fig 38. Sample image 43; 0.1 mH



aaa-004919

Fig 39. Sample image 51; 15 mH



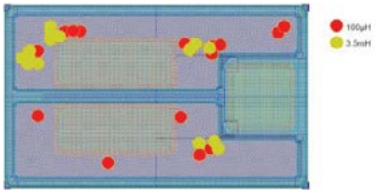
aaa-004920

Fig 40. Sample image 55; 15 mH

8.2.10 Unclamped inductive switching EOS of PSMN7R0-30YL

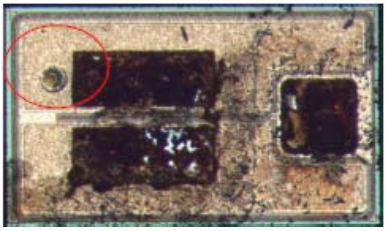
Table 15. Unclamped inductive switching EOS

PSMN7R0-30YL	
Cell structure:	2 µm stripe
Package:	LFPAK (clip bond)
Die size:	2.3 mm x 1.35 mm
EOS condition:	Red dots: 0.1 mH, 48 A to 51 A Yellow dots: 3.5 mH, 16 A to 18 A



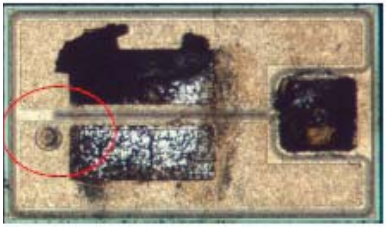
aaa-004921

Small, round, burn marks, randomly distributed over active area, close to but not directly under clip bond



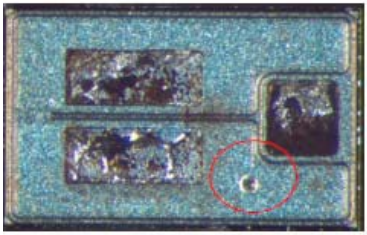
aaa-004922

Fig 41. Sample image 6; 0.1 mH



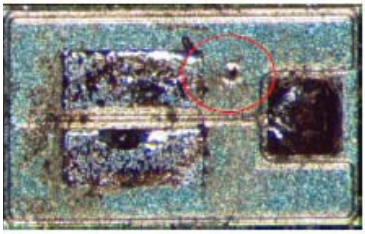
aaa-004923

Fig 42. Sample image 8; 0.1 mH



aaa-004924

Fig 43. Sample image 18; 3.5 mH



aaa-004925

Fig 44. Sample image 20; 3.5 mH

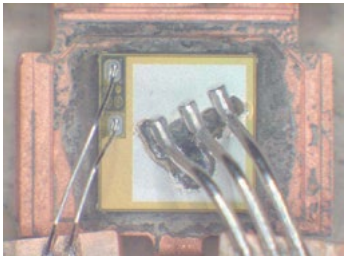
8.2.11 Linear mode EOS of BUK7L06-34ARC

Table 16. Linear mode EOS

BUK7L06-34ARC	
Cell structure:	9 mm hexagon
Package:	TO-220 (clip bond)
Die size:	4.3 mm x 4.3 mm
EOS condition:	
15 V, 3 A	Burn marks located in middle of the die adjacent to wire bonds
30 V, 1.5 A	Burn mark and location are more discrete at 20 V, 1.5 A

aaa-004926

Fig 45. Sample image 1: 15 V, 3 A

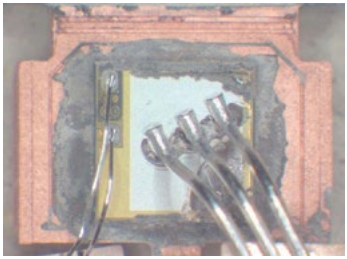


aaa-004927

Fig 46. Sample image 2: 15 V, 3 A

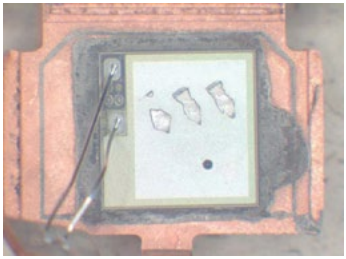
aaa-004928

Fig 47. Sample image 3: 15 V, 3 A



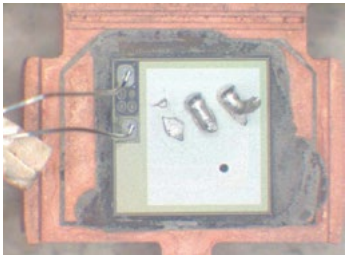
aaa-004929

Fig 48. Sample image 4: 15 V, 3 A



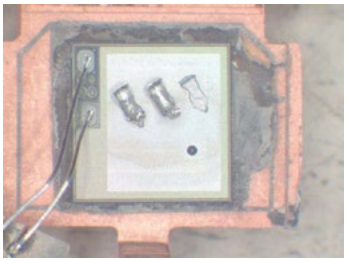
aaa-004930

Fig 49. Sample image 1: 30 V, 1.5 A



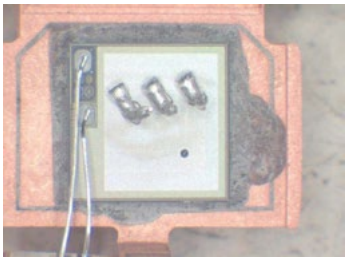
aaa-004931

Fig 50. Sample image 2: 30 V, 1.5 A



aaa-004932

Fig 51. Sample image 3: 30 V, 1.5 A



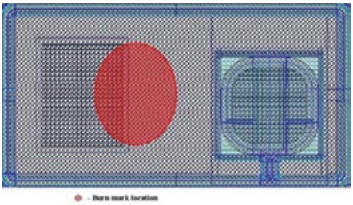
aaa-004933

Fig 52. Sample image 4: 30 V, 1.5 A

8.2.12 Linear mode EOS of BUK9Y40-55B

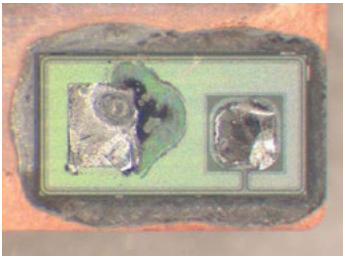
Table 17. Linear mode EOS

BUK9Y40-55B	
Cell structure:	4 µm stripe
Package:	LFPAK (clip bond)
Die size:	2.5 mm x 1.35 mm
EOS condition:	20 V, 3.5 A, 30 ms
	20 V, 3 A, 60 ms
	30 V, 1.4 A, 60 ms



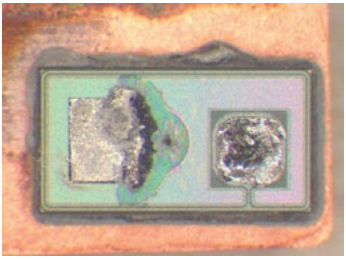
aaa-004934

Burn marks in center of die, adjacent but not directly under clip bond – can cause die cracking



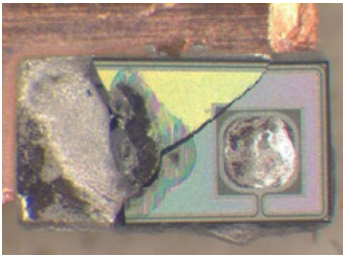
aaa-004935

Fig 53. Sample image 61; 20 V, 3.5 A, 30 ms



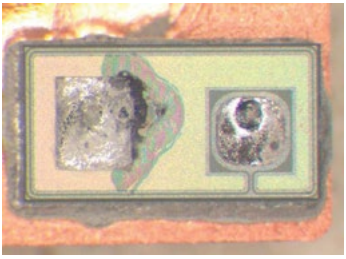
aaa-004936

Fig 54. Sample image 62; 20 V, 3.5 A, 30 ms



aaa-004937

Fig 55. Sample image 63; 20 V, 3.5 A, 30 ms

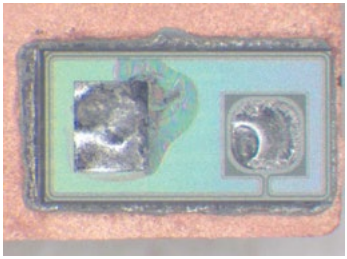


aaa-004938

Fig 56. Sample image 64; 20 V, 3.5 A, 30 ms

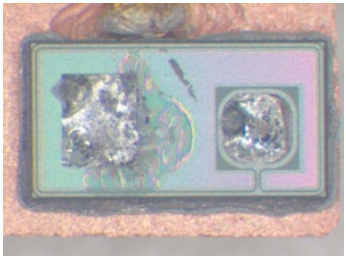
aaa-004939

Fig 57. Sample image 66; 20 V, 3 A, 60 ms



aaa-004941

Fig 58. Sample image 67; 20 V, 3 A, 60 ms

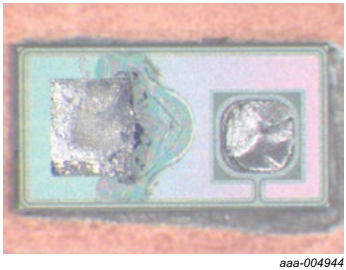


aaa-004942

Fig 59. Sample image 68; 20 V, 3 A, 60 ms

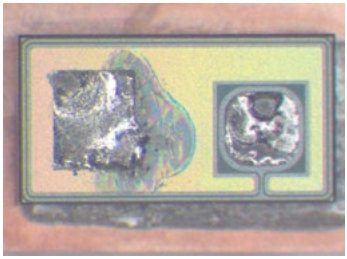
aaa-004943

Fig 60. Sample image 69; 20 V, 3 A, 60 ms



aaa-004944

Fig 61. Sample image 71; 30 V, 1.4 A, 60 ms



aaa-004946

Fig 62. Sample image 72; 30 V, 1.4 A, 60 ms

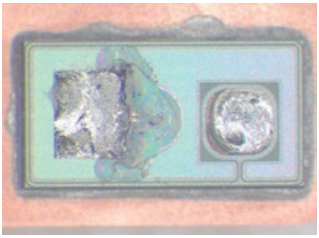


Fig 63. Sample image 73; 30 V, 1.4 A, 60 ms

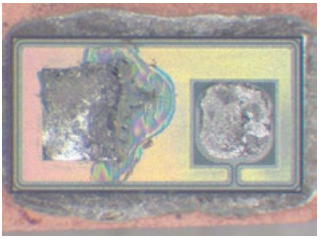


Fig 64. Sample image 74; 30 V, 1.4 A, 60 ms

8.2.13 Linear mode EOS of PSMN7R0-30YL

Table 18. Linear mode EOS

PSMN7R0-30YL	
Cell structure:	2 µm stripe
Package:	LFPAK (clip bond)
Die size:	2.3 mm x 1.35 mm
EOS condition:	Burn marks in center of die, adjacent but not directly under clip bond
	0.1 mH, 48 A to 51 A
	3.5 mH, 16 A to 18 A

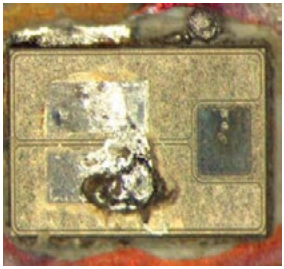

aaa-004948

Fig 65. Sample image 1; 15 V, 2.5 A, 100 ms


aaa-004951

Fig 66. Sample image 2; 15 V, 2.5 A, 100 ms

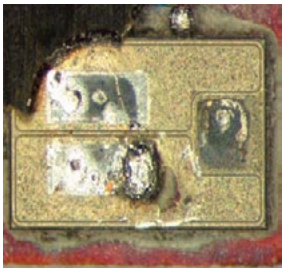

aaa-004953

Fig 67. Sample image 4; 15 V, 2.5 A, 100 ms

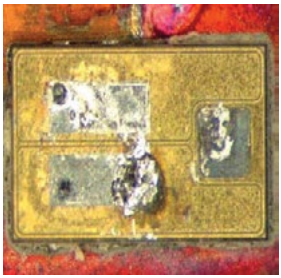

aaa-004954

Fig 68. Sample image 5; 15 V, 2.5 A, 100 ms

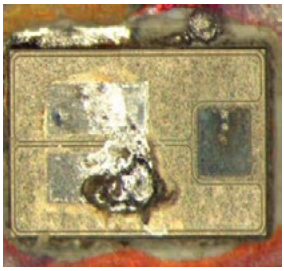

aaa-004955

Fig 69. Sample image 11; 15 V, 5 A, 1 ms


aaa-004956

Fig 70. Sample image 12; 15 V, 5 A, 1 ms

Fig 71. Sample image 13; 15 V, 5 A, 1 ms

Fig 72. Sample image 14; 15 V, 5 A, 1 ms

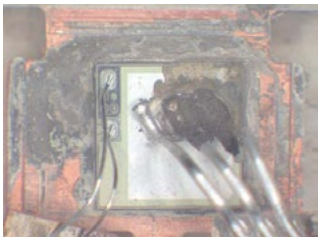
8.2.14 Over-current EOS of BUK7L06-34ARC

Table 19. Over-current EOS

BUK7L06-34ARC	
Cell structure:	9 µm hexagon
Package:	TO-220 (clip bond)
Die size:	4.3 mm x 4.3 mm
EOS condition:	120 A
	Extensive damage starting from die where wire bonds meet die. Secondary damage of reflowed solder and even fused wires are visible

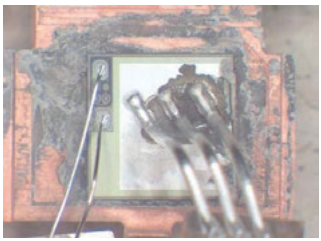
aaa-004959

Fig 73. Sample image 1



aaa-004960

Fig 74. Sample image 2



aaa-004961

Fig 75. Sample image 3

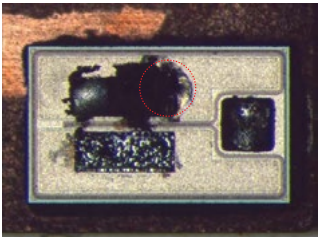
aaa-004962

Fig 76. Sample image 4: source wires fused

8.2.15 Over-current EOS of PSMN7R0-30YL

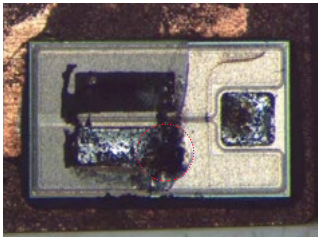
Table 20. Over-current EOS

PSMN7R0-30YL	
Cell structure:	2 µm stripe
Package:	LFPAK (clip bond)
Die size:	2.3 mm x 1.35 mm
EOS condition:	35 A, 35 ms
	Burn marks located in center of die under and adjacent to clip bond. Some evidence of die-cracking



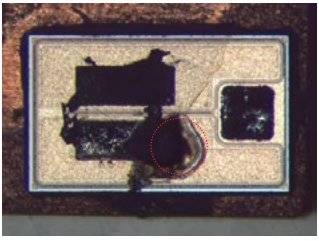
aaa-004963

Fig 77. Sample image 6



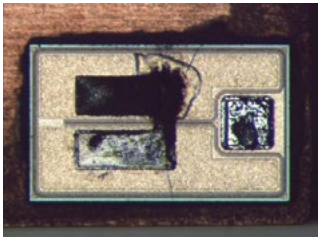
aaa-004964

Fig 78. Sample image 7



aaa-004965

Fig 79. Sample image 8; die is cracked through burn



aaa-004966

Fig 80. Sample image 10; die is cracked through burn

8.3 Tables

8.4 Figures

Chapter 9: Power MOSFET frequently asked questions

Chapter 9: Power MOSFET frequently asked questions

9.1 Introduction

This chapter provides a number of important questions regarding the use of MOSFETs and the platforms required. Although it is focused on automotive applications, the principles can apply to industrial and consumer applications. It strives to provide clear answers to these questions and the reasoning behind the answers.

This content is intended for guidance only. Any specific questions from customers should be discussed with NXP Power MOSFET application engineers.

9.2 Gate

9.2.1 Q: Logic Level Trench generation 3 types are specified with 15 V (V_{GS}). What is the technical reason for the reduction to 10 V for the Trench generation 6 logic level platform?

A: The Trench generation 3 platform is >10 years old. It was released to the best practice rules of the time. In particular, it was designed and assessed to meet the requirements of AEC-Q101. Production control and testing were established to ensure ongoing compliance to those requirements.

In the intervening years, the best practice rules have moved on. In particular, the understanding of gate oxide wear out has improved. It is now appreciated that meeting AEC-Q101 does not guarantee meeting modern reliability requirements. The market is looking for failure rates significantly lower than 1 PPM over the lifetime of >15 years.

In the Trench generation 6 data sheet, V_{gs} is rated at 175 °C and DC conditions. The gate can withstand 20 V at 25 °C for a short period (>1 hour on worst case parts). The capability is expected to be similar to competitor parts, often they state 20 V but do not specify the conditions for it.

Additional information

The Trench generation 6 platform specifies a gate voltage rating that exceeds the market reliability requirements and has production controls and tests to guarantee them.

The 10 V DC rating is conservative. Customer feedback is to set a clear, conservative but realistic limit on the data sheet. It ensures that engineers are guided to adopt good design practice and not use excessive overdrive.

For Trench generation 6 devices, use logic level parts where gate drive voltage is between 5 V and 10 V. Voltages of 15 V do not destroy any logic level part. Clearly, voltages between 10 V and 15 V are possible and have a corresponding range of lifetimes. However, the guidance is to use standard level parts where the gate voltage is >10 V for >100 Hours in the life of the vehicle.

When new designs consider using a Trench generation 3 part, or earlier NXP technology, the same guidance should be used. It is because the gate oxide thicknesses are the same in Trench generation 3 and Trench generation 6. However, it should be appreciated that the same guarantees cannot be given because the tests and controls are not the same.

9.3 Thermal impedance (Z_{th}) curves

9.3.1 Q: When comparing Z_{th} curves in some data sheets, there appear to be some contradictions.

From an R_{th} point of view, the BUK9Y38-100E (Trench generation 6) looks better (lower). However, from a Z_{th} (at less than 100 ms) point of view, the BUK9Y30-75B (Trench generation 3) looks better. The shape of the graphs indicates that a more advanced model or measurement was done on the Trench generation 6 part. Is this assumption correct?

A: The method for setting the Z_{th} curve has changed between the Trench generation 3 parts (2008) and Trench generation 6 (2012). The die size is also different which changes the Z_{th} and R_{th} characteristics.

Additional information

The earlier method used empirical models for Zth (1 µs) and R_{th}, joined by an exponential line.

The latest method uses models for the Z_{th} generated by Computational Fluid Dynamics (CFD) simulation, verified by measurement.

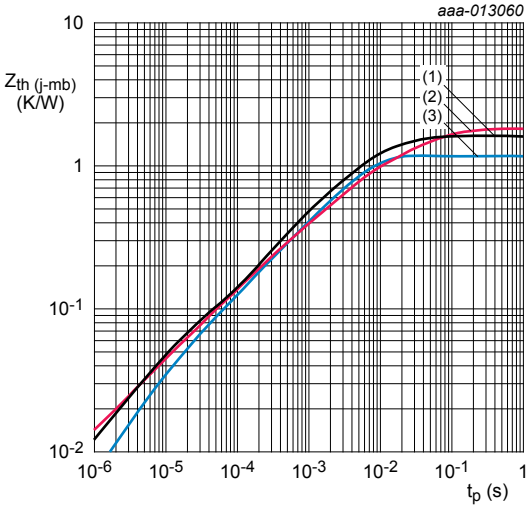
The dies in the 2 parts have different dimensions and therefore they have different Z_{th}.

The plots depicted in **Figure 1** compare the data sheet curves for the single shot Z_{th}.

There is a good match between the limit lines for both parts. The biggest difference is in the region 1 ms to 20 ms.

The conclusion from this comparison, is that if the Trench generation 3 part is designed to work within these Z_{th} limits, the Trench generation 6 part is an excellent alternative. It has a very high probability of working satisfactorily.

It is possible to assess how to rate the Trench generation 3 part using the new rules with a more accurate reflection of the true performance of it. **Figure 1** shows the new line in comparison with the two data sheet lines.



(1) = BUK9Y38-100E

(2) = BUK9Y30-75B

(3) = BUK9Y30-75B (new test method)

Fig 1. Comparison of transient thermal impedance

Although there is a difference in the R_{th}, it is probably unimportant. In practice, it is the $R_{th(j\text{-}amb)}$ that is the limiting factor for the design. The R_{th} of the PCB that is common to both parts, is dominant.

When considering the old test method with the new one for the BUK9Y30-75B, the other region of difference is below 10 µs. For pulses between 1 µs and 2 µs, the temperature rise (or $Z_{th(j\text{-}mb)}$) in the Trench generation 3 part, is only a half of what the original data sheet curve predicted. The importance of this factor depends on the application.

9.3.2 Q: It is understood that the values for thermal resistance listed in data sheets are based on controlled conditions that do not apply to typical applications. If this understanding is true, how is the proper thermal resistance/junction temperature accurately calculated?

A: This understanding is correct. To ensure reliability of the MOSFET, always limit the maximum junction temperature to 175 °C.

Additional information

- **It is understood that the typical values for thermal resistance listed in data sheets are based on controlled conditions that do not apply to typical applications.**

  Device characterization at a junction temperature of 25 °C is the accepted standard in the semiconductor industry. It is also most convenient for users to take measurements at this temperature.

- **How is the proper thermal resistance calculated?**

  Only a maximum value of thermal resistance is given on NXP MOSFET data sheets. The typical value is significantly less than the maximum. It is well understood that thermal cycling can induce an increase in $R_{th(j\text{-}mb)}$ over the lifetime of the MOSFET. A tolerance margin is included in the data sheet maximum $R_{th(j\text{-}mb)}$ value which allows for an increase of over the lifetime of the MOSFET.

  The maximum value should always be used for worst case design analysis. Maximum $R_{th(j\text{-}mb)}$ given on the data sheet is evaluated from characterization measurements.

  Its value is not dependent on temperature or other environmental conditions.

- **How is junction temperature calculated?**

  MOSFETs usually operate with a junction temperature greater than 25 °C due to temperature rise caused by the environment and/or power dissipation in the MOSFET.

If MOSFET power dissipation and mounting base temperature (T_{PCB}) are known, MOSFET junction temperature can be calculated. Use **Equation 1** to determine T_j.

(1) $$T_j = P * R_{th(j-mb)} + T_{PCB}$$

SPICE thermal models of MOSFETs provide an excellent means of estimating T_j by simulation. It is particularly useful when MOSFET power dissipation changes with time.

Worked example for a BUK7Y12-40E:

From the data sheet:

Maximum $R_{DS(on)}$ at 25 °C = 12 mΩ

Maximum $R_{DS(on)}$ at 175 °C = 23.6 mΩ

Maximum $R_{th(j-mb)}$ at 2.31 K/W

From the application data:

PWM frequency = 100 Hz

Maximum duty cycle = 50 %

V_{supply} = 14 V

R_{load} = 0.7 Ω

Maximum ambient temperature = 85 °C

Maximum PCB temp. = 100 °C

Calculation based on average power, ignoring any temperature fluctuation due to the power pulsing and also ignoring switching losses at 100 Hz:

Assume that the temperature of the MOSFET is initially 100 °C and its maximum $R_{ds(on)}$ is 18 mΩ (midway between 12 mΩ at 25 °C and 24 mΩ at 175 °C).

When conducting, the MOSFETs power dissipation $I^2R_{DS(on)}$ = 20 x 20 x 0.018 = 7.2 W.

The duty cycle is 50 %, so the average power dissipation = 7.2 x 0.5 = 3.6 W. It is assumed that the switching loss at 100 Hz can be ignored.

The rise of the MOSFET junction temperature, above the mounting base, = 2.31 x 3.6 = 8.3 K.

The maximum MOSFET die temperature in this situation is 100 + 8.3 = 108.3 °C (which is very safe).

To guarantee that the PCB temperature does not rise above 100 °C in an 85 °C ambient, the thermal resistance between PCB and ambient must be (100 - 85)/3.6 = 4.2 K/W.

9.4 MOSFET body diode

9.4.1 Q: How much current can the MOSFET body diode carry?

A: The data sheet states the I_s capability for the diode. The power constraints are the same as for the MOSFET conduction. The diode is an integral part of the MOSFET structure. They are in effect the same size and have the same thermal properties. The MOSFET can carry the same current through the channel or in reverse through the body diode. The maximum steady state current in the diode is dependent on the total allowed power loss for the device. However, the diode current may be different from the channel current because the power dissipation may be different under the 2 modes of operation.

Additional information

The objective is to keep the junction temperature below $T_{j(max)}$ so it is necessary to calculate the diode dissipation. In a DC case, it is simply I_f x V_f. It is equivalent to V_{sd} x I_s as used in the NXP MOSFET data sheet. For a worse case analysis, the max V_f of the data sheet should be used (normally 1.2 V).

Where the current is varying but in cyclic manner, the dissipation can be found using the equation:

(2) Power: $V_o \cdot I_{avg} + R_s \cdot I_{rms}^2$

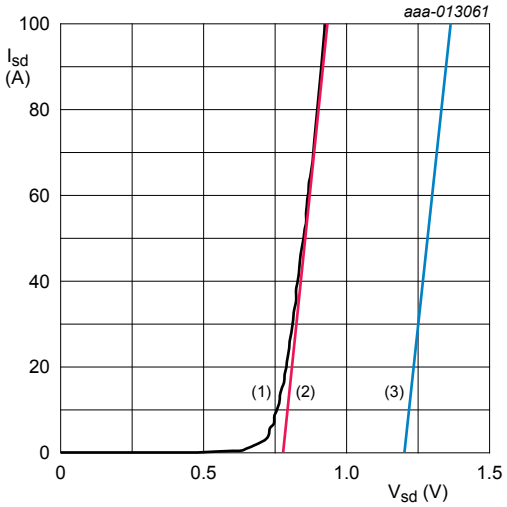
where:

I_{avg} is the average diode current

I_{rms} is the RMS diode current

R_s is the slope of the I_{sd}/V_{sd} characteristic graph given in data.

V_o is typically where the R_s line meets the axis at $I_{sd} = 0$. For a conservative worst case analysis, use 1.2 V.



(1) = characteristic at 25 °C

(2) = idealized characteristic at 25 °C

(3) = worst case idealized characteristic at 25 °C

Fig 2. Diode characteristics

For transient currents, a simulation using the spice model of the diode is useful but care is needed because the model is for a typical part.

Once the dissipation is known, standard thermal analysis methods can be used to check that T_j is acceptable. It can include SPICE simulation using RC thermal models.

9.5 Safe operating area and linear mode operation

9.5.1 Q: The current derates with temperature. Is this limit based on power dissipation?

A: The most important factor in current derating or power derating is junction temperature. T_j is a function of power dissipation. Power dissipation is a function of I_d current and on-state resistance ($P = I_d^2 \times R$) when operating in the fully enhanced mode. It is the product of I_d and V_{ds} when operating between on and off states. The R_{dson} of a MOSFET, increases with increase in temperature. Therefore, for a given maximum power dissipation, the maximum current must be derated to match the maximum power dissipation. In NXP data sheets, graphs show the continuous drain current and normalized total power dissipation (see **Figure 4**) as a function of the mounting base temperature. These graphs can be used to determine the derating.

9.5.2 Q: Is it necessary to derate any limit (current, voltage, power etc.) to achieve high reliability?

A: If current, voltage, power, junction temperature, etc. are within NXP data sheet limitations, no additional derating is needed. In the data sheet, there is a power derating curve based on junction temperature. Junction temp (T_j) is one of the most important factors for reliability. Particular care should be taken to extract enough heat from the device to maintain junction or die temperature, below rated values. The device should be operated within the SOA region. It should be derated if necessary (see **Section 9.5.3**) as recommended in the data sheet and it should be possible to obtain optimum reliability.

9.5.3 Q: How do I derate an SOA graph for temperatures other than 25 °C?

A: As an example, assume that the temperature required is 100 °C, instead of 25 °C. T_j rated is 175 °C for this automotive grade MOSFET. Derate the voltage when considering the effect of temperature on SOA performance (see **Figure 3**). To determine the new voltage (at temperature) for a fixed current, use the power derating line in **Figure 4**. For example, power at 100 °C = 50 % of power at 25 °C. Therefore, the 10 V line represents 5 V at 100 °C etc. It is explained in *Application Note AN11158* (Chapter 1 of this book). If necessary, the SOA lines for 1 ms, 10 ms etc. can be extended at the same slope to the right.

For example: with a mounting base temperature of 25 °C, the allowed temperature rise is 150 °C for a given automotive MOSFET rated at 175 °C. At 100 °C, the allowed temperature rise is reduced to a half (75 °C). As a result, the allowed power is half of that allowed at 25 °C. Because of the effects of linear-mode operation, the current is maintained but the allowed drain-source voltage is derated. The SOA graph depicted in **Figure 3**, shows the voltage derating effect for 100 °C condition. It is explained in more detail in Chapter 1.

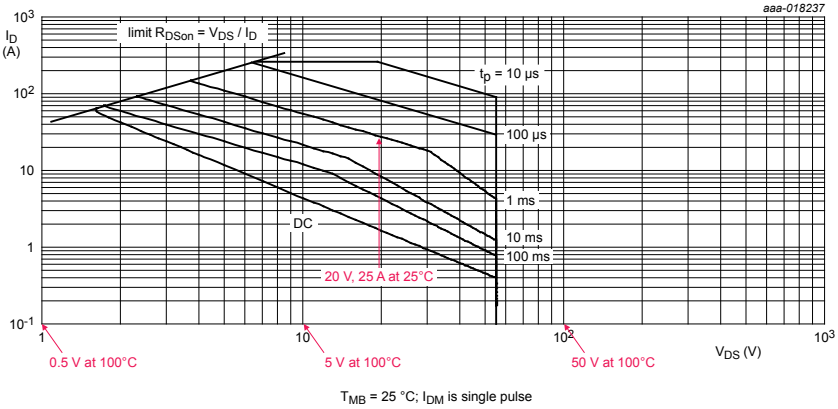


Fig 3. Example: BUK7Y12-55B SOA curve showing derating for 100 °C

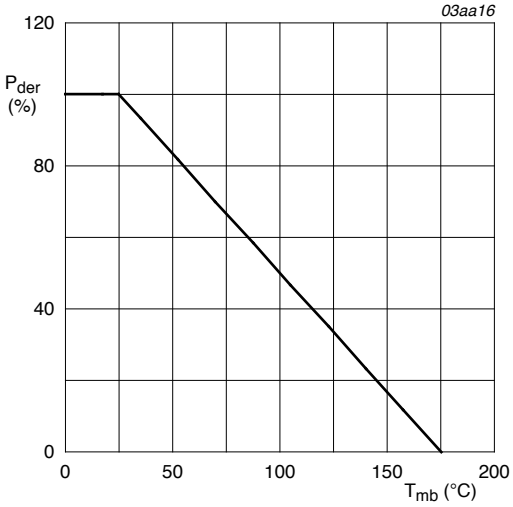


Fig 4. Normalized total power dissipation as a function of solder point temperature

(3) $$P_{der} = \frac{P_{TOT}}{P_{TOT(25°C)}} \times 100\%$$

9.5.4 Q: Is there a Spirito boundary limit line for linear mode operation?

A: The Spirito region or hot spotting issue with new higher density technologies may have more effect in the linear mode of operation. This effect is evident from the change in gradient in the limit lines for 1 ms, 10 ms and 100 ms at higher V_{ds} values (see **Figure 3**). The 1 ms, 10 ms, 100 ms and DC lines at higher V_{ds} values emphasize it. The reason is that most newer technologies pack more parallel fundamental cells to share more current in a smaller die (lower R_{dson} per unit area). It leads to an increased thermal coupling between cells. Also, to attain higher current densities, the MOSFETs are designed with higher transconductance or gain ($g_{fs} = I_d / V_{gs}$). It enables them to carry higher currents even at lower V_{gs} values. However $V_{gs(th)}$ (threshold voltage) has a negative temperature coefficient which leads to a higher zero temperature coefficient crossover value. For various reasons, the distribution of temperature in the die is never perfectly uniform.

Therefore, when the device is operated for extended periods in linear mode, hot spotting occurs. Due to the shift in threshold voltage, there is a risk of thermal runaway and device destruction where the hotspots form. Because of these reasons, special care should be taken when using trench or planar MOSFETs for linear applications. Ensure that operation remains within the data sheet SOA limits.

9.5.5 Q: Can Trench designs operate in the linear mode?

A: In order to optimize R_{dson} and switching performance, some modern Trench technology is designed with a very aggressive cell pitch. Generally, it is harmful to linear mode performance. NXP Trench technology uses a less aggressive cell pitch than competitors and achieves better linear mode performance, while maintaining very good R_{dson} and switching performance. If care is taken in the selection and use of the device, noting particularly the SOA temperature derating, these devices can be used in linear mode.

9.5.6 Q: How can a part be identified when it is designed for linear mode operation?

A: While all NXP MOSFETs can be used in linear mode operation, some NXP MOSFETs are designed specifically to be used in linear mode. The device description in the data sheet states that the device is suitable for operation in linear mode. To determine the suitability for operation in linear mode, perform a thorough analysis of the SOA graph. This analysis includes derating the SOA graph for junction temperatures above 25°C. The naming convention indicates that the MOSFET is designed for linear mode applications (refer to the part naming conventions in the selection guide).

9.5.7 Q: For parts designed for linear mode operation, are there any restrictions (such as the Spirito boundary)?

A: **Even if a MOSFET is intended for use in linear mode applications, the part must not be operated outside of its SOA.** Post 2010, all NXP MOSFETs have a measured SOA characteristic. The limit of linear mode capability on NXP parts is shown in the SOA characteristic. As a result, the boundary of what is safe is established via measurement rather than calculation. The Spirito capability limit is shown in the SOA characteristic.

9.6 Avalanche Ruggedness and Unclamped Inductive Switching (UIS)

9.6.1 Q: Are trench designs susceptible to the UIS issue (parasitic BJT turn-on)?

A: In general - Yes, but NXP Trench MOSFETs are designed to suppress this effect. The trench structure, unlike planar, can be very easily designed to suppress parasitic turn on of the BJT. For new NXP MOSFET technologies, the failure mechanism is thermal, which represents the limit of achievable UIS performance. Planar (on the left in the diagram) and Trench (on the right in the diagram) MOSFET technologies, are shown in **Figure 5**. In the Trench case, a design feature in the source contact effectively short circuits the base - emitter of the parasitic BJT. In older planar technology, the shorting of base to emitter of the parasitic bipolar is not as effective due to the longer path length in the n and p regions.

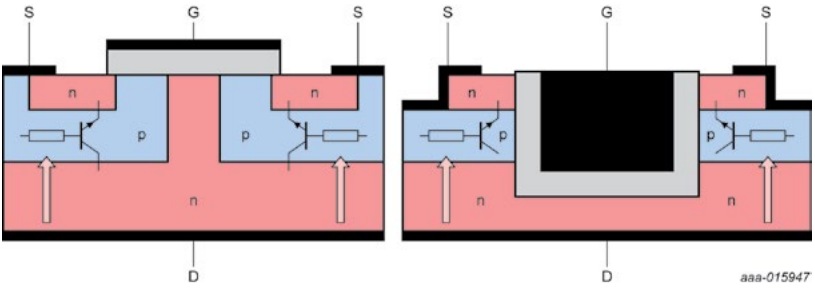


Fig 5. Simplified planar and trench technology

9.6.2 Q: Why are planar designs susceptible to failure during UIS?

A: All MOSFETs are susceptible to failure during UIS. It depends on whether the MOSFET T_j reaches the intrinsic temperature of silicon. Furthermore, if the parasitic BJT is triggered, they can fail even earlier. It is because the BJT can be switched on relatively quickly but is slow to switch off. Current can then crowd in a certain part of the device and failure results. Newer NXP trench technologies are less vulnerable to triggering of the BJT than planar designs. See **Section 9.7.1** and the additional information associated with **Section 9.6.3**.

9.6.3 Q: How are parts constructed to minimize failure during UIS?

A: The base emitter path in the silicon design is designed to minimize the risk of triggering the parasitic BJT.

Additional information

There are two strategies employed to prevent triggering of the parasitic BJT:

1. Reduce the avalanche current per cell - To reduce the avalanche current per cell, there must be a higher cell density. It is easily achieved with Trench technologies but more difficult with planar devices. If improvements in planar technologies are seen, it is likely that modern fabrication equipment achieves a high enough cell density. Increasing cell density too much, deteriorates linear mode performance (Spirito boundary occurs sooner), so cell density is a trade-off. For this reason, NXP has not been as aggressive as other Trench MOSFET manufacturers in achieving very high cell densities. The target is to ensure that the thermal limit in UIS is achieved.
2. Ensure that the current flow during avalanche does not flow through the base - emitter region of the BJT. This feature is the significant advantage of Trench over Planar. The parasitic bipolar is formed between the source of the MOSFET, the body region (i.e. channel) and the Epi region (i.e. the drain). If there is enough avalanche current through body junction, there may be enough voltage developed to bias on the BJT leading to device destruction. In NXP devices, a modified source contact is used. This contact collects any avalanche current, preventing it from biasing the BJT on.

   For planar devices, strategies include reducing the gain of the BJT by placing high doped implants close to the channel. It is similar to (2) in intention but it is not as effective.

9.6.4 Q: Is 100 % UIS testing required on MOSFETs?

A: UIS testing is a fundamental part of NXPs defect screening procedures. It is applied to all devices. The test is designed to increase the junction temperature to $T_{j(max)}$.

9.6.5 Q: I have parts not capable of parasitic BJT turn-on. Why?

A: Devices fail at the thermal limit. At the thermal limit, the silicon becomes intrinsic and blocking-junctions cease to exist. It is considered to be the only UIS-related failure mechanism in our devices.

9.6.6 Q: What is the chart accuracy for avalanche current vs. time in avalanche, or energy vs. junction temperature?

A: Avalanche current versus time graphs are based on conditions that take a device to $T_{j(max)}$ and therefore, our ruggedness screening covers them. All NXP MOSFETs are ruggedness tested during assembly and characterized during development. The graphs are accurate and provide the worst case capability of the device to ensure reliability.

9.6.7 Q: For energy versus junction temperature charts (if applicable), how is the inductance, maximum current, time in avalanche etc., determined from the chart?

A: A temperature rise model is used, which is shown in AN10273 *Power MOSFET single-shot and repetitive avalanche ruggedness rating (Chapter 2 of this book)*.

Additional information

Although energy levels for UIS are often quoted on data sheets, a single number can be misleading. Therefore a graph is provided, that outlines conditions that take junction temperature to $T_{j(max)}$. The user must determine the current/time in avalanche based on the particular conditions. Examples are provided in Chapter 2.

9.6.8 Q: Are repetitive avalanche ratings the same as for a single pulse?

A: No. The repetitive avalanche ratings are lower than the single pulse rating. Refer to the product data sheet for the device capability. An example is shown in **Figure 6**.

Additional information

Repetitive means that the avalanche event is an intended operating condition for the device.

Similarly, “Single shot” means that the MOSFET is expected to experience an avalanche event as a result of some unintended fault condition. Only 1 fault can occur at a time, the MOSFET must cool to the starting temperature and the junction temperature must not exceed 175 °C. Degradation of device characteristics is likely after a relatively low number of occurrences.

NXP shows both single shot and repetitive avalanche capability in the MOSFET data sheet. Generally, the repetitive current is 10 % of the single shot current capability for a given inductor (so the time in avalanche is shorter, see **Figure 6** and **Section 9.6.14**).

For calculating repetitive avalanche ratings, calculate the starting junction temperature for each avalanche incident independently. The calculations are based on the frequency and duty cycle of avalanche condition and summed over the entire period of expected repeated avalanche. This topic is discussed in detail in Chapter 2.

9.6.9 Q: Are there any special failure modes associated with repetitive avalanche?

A: The device can sustain small amounts of damage with each avalanche event and over time they can accumulate to cause significant parametric shifts or device failure. NXP has performed research into this area and provides the repetitive ratings in the data sheet. See also Chapter 2.

9.6.10 Q: How does the increase in cell density affect avalanche capability of MOSFETs?

A: There are two failure modes: current (parasitic BJT turn-on) and thermal. Cell density has implications for these failure modes.

Additional information

Current - If enough avalanche current flows through a cell, a voltage drop occurs in the p-region of the device as the avalanche current flows to the source contact. This volt drop occurs in the base of a parasitic bipolar device. In this mode, the resistance in the p-region/base and the avalanche current (I = V/R) are important. Once V_{be} reaches the bipolar switch-on threshold, the MOSFET is destroyed (V_{be} reduces with temperature). So at higher cell densities, for the same avalanche current, there are more cells and current per cell is reduced. Each individual cell has less current and is less likely to trigger the parasitic device. It means that the total die current, required to cause a device to fail, increases. Additionally, since the cell is smaller, the path through the p-region to the source contact is reduced. It makes it even harder to trigger the parasitic device and again increases the current required to destroy the device.

Thermal - If the avalanche current is such that the parasitic BJT is not triggered, the device heats up. If the avalanche energy is sufficient, the silicon die reaches temperatures at which the device starts to become intrinsic. The blocking-junction no longer exists, resulting in the destruction of the device. It is what is meant when a reference is made regarding failure due to reaching the thermal limit of a device. If the failure mode is thermal, changes in technology cannot improve things significantly. New technologies are generally more robust in avalanche conditions. Note, if a thermal limit is reached, the only solution is to improve the thermal impedance at the device level. Moving to a smaller die can be detrimental.

Summary - New technologies improve the high current avalanche capability of a device due to increased cell density and reduced parasitic NPN base resistance. Lower current, higher energy (i.e. longer duration) avalanche capability is unchanged.

9.6.11 Q: How many times can a device sustain single avalanche events?

Example - A device has an avalanche event once in two months so how many cycles of such an avalanche frequency can the device sustain? This question relates more to quality and reliability but it is important nonetheless.

A: Refer to **Section 9.6.8** of this chapter. For the answer to this question, refer to **Section 1.2.4.3** of Chapter 1 and all of Chapter 2.

Additional information

Keep each avalanche event within the safe limits for repetitive operation specified on the data sheet and T_j below 175 °C. There should be no degradation of the MOSFET characteristics and no impact on MOSFET quality or reliability. There are some applications where MOSFETs are repetitively avalanched (e.g. some engine controllers) and the reliability is good. Although this condition takes V_{DS} beyond the data sheet maximum, the data sheet also specifies a maximum avalanche energy.

Extensive avalanche testing is performed on NXP MOSFETs. All the indications are that they are very robust. It is understood that most MOSFETs in automotive applications are likely to experience avalanche conditions at some stage during their lifetime. It could be due to occasional fault conditions or as a consequence of the circuit design (e.g. ABS solenoid valve driver MOSFETs).

9.6.12 Q: Is it possible for the avalanche current on a device to exceed the package maximum current but not the die maximum current?

A: The current specified in the avalanche graph should not be exceeded. It is restricted to the DC rated current. The device factory test defines the limit which is guaranteed for the device.

9.6.13 Q: How is the avalanche rating on the body diode obtained (testing or modeling). If it is tested, how is it tested and what circuit model is used?

A: The avalanche rating is modeled first and the results are then verified by testing to destruction. The test circuit used is similar to the one defined in *JESD24-5*. For spice modeling, the reverse diode characteristics can be defined and modeled. By adding an RC thermal model of the Z_{th} characteristic, it is possible to estimate the T_j of the device.

Additional information

The body diode of the MOSFET is not a single circuit element, but a structure distributed throughout the MOSFET. There is a diode element associated with each cell. In behavior terms, it can be represented as a single (Zener) diode in parallel with the single MOSFET (representing the sum of all the cells). The design of the MOSFET determines the avalanche rating. Its representation in the model is based on parameters measured during characterization testing.

The constraints are the same as for the MOSFET conduction. Diodes are an integral part of the MOSFET structure. They are in effect the same size and have the same thermal properties. The objective is to keep the junction temperature below $T_{j(max)}$ so it is necessary to calculate the diode dissipation.

For transient currents, the simulation using the spice model of the diode is useful but care is needed because the model is for a typical part.

Once the dissipation is known, standard thermal analysis methods can be used to ensure that T_j is acceptable.

9.6.14 Q: How is the repetitive avalanche safe operating area derived in the data sheet graph? The repetitive avalanche SOA curve seems to be the same as single-shot T_j = 170 °C.

A: The repetitive line is the line for a start temperature of 170 °C. It is because it predicts a temperature rise of 5 °C which is the maximum permissible rise from any starting temperature (see Chapter 2). It also corresponds to 10 % of the single shot current using the same inductor value, see **Figure 6**.

Additional information

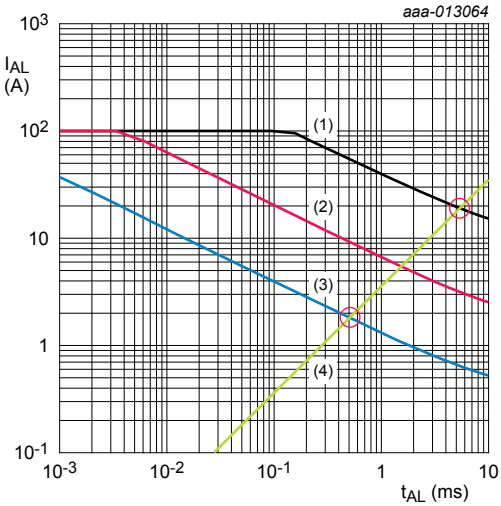
The reason it applies to any temperature is because the temperature does not strongly influence the wear-out caused by repetitive avalanche. The strongest influence is the current.

The avalanche current is composed of high energy charge carriers moving through the depletion region. As they pass through, they can collide with the Si structure. There is a chance that a high energy carrier (sometimes called a “hot carrier”) is produced that collides with the gate oxide causing it to be damaged. It is not completely destroyed but it does cause it to wear out, which is observed as parameter variation.

Higher currents mean more electrons, more collisions and more frequent damaging events leading to faster wear-out and lower reliability. The target should be a failure level <0.1 ppm over the full vehicle life. Experiments indicate that if repetitive current is limited to 10 % of single-shot current capability for $T_{j(start)}$ = 25 °C, it results in a T_j increase of 5 °C. There is no significant degradation of the device.

For example: A 15 mH inductor carrying ~19 A gives an avalanche time of ~5 ms. It has a peak temperature rise of 150 °C putting it on the limit line for a start T_j = 25 °C.

By reducing the current to 10 % = 1.9 A, t_{av} reduces to ~500 µs and the temperature rise is 5 °C.



(1) = characteristic at 25 °C

(2) = characteristic at 150 °C

(3) = repetitive characteristic at <170 °C

(4) = inductor characteristic

Fig 6. Avalanche safe operating area

9.7 Capacitive dV/dt issues

9.7.1 Q: Is there a particular capacitance or charge ratio that should be used to prevent turn-on, or is it circuit dependent?

A: The capacitive dV/dt turn-on is strongly circuit dependent.

Additional information

If the dV/dt across the MOSFETs drain to source is too high, it may charge C_{gd}, which is the capacitance between drain and gate, inducing a voltage at the gate. The gate voltage depends on the pull down resistor of the driver based on **Equation 4**:

(4) $V_{gs} = R_{driver} * C_{gd} * dV/dt$

In some bipolar drive circuits (such as emitter follower derived circuits), the problem is increased because the driver cannot pull the gate down to 0 V and has about 0.7 V offset.

It is also important that the driver is referenced to the MOSFET source and not to signal ground, which can be significantly different in voltage.

The ratio of C_{gd} to C_{gs} is a factor but a good drive circuit is the critical factor.

Even if a V_{gs} spike is present, it is safe for the MOSFET as long as the dissipation is within thermal limits and within the MOSFET SOA limits.

9.7.2 Q: How are parts constructed to minimize this effect?

A: NXP MOSFETs are designed with a high threshold at high temperatures and we check V_{gs} threshold at 25 °C is within data sheet limits. Logic level devices are designed and guaranteed to have a minimum threshold voltage >0.5 V even at 175 °C.

Additional information

Maintain a reasonable ratio between C_{gd} and C_{gs}. The gate network structure of the device is designed to have good control of all areas of the die.

9.7.3 Q: How is dV/dt characterized?

A: It is usually measured in a half-bridge test circuit. It is a measure of the device dVds/dt during body diode reverse recovery. This data is not normally published in the data sheet. This dV/dt is in practice the highest dV/dt the device experiences.

Additional information

Failure due to dV/dt is not something seen in modern low-voltage MOSFETs however, dV/dt is normally characterized for NXP MOSFETs. The failure mode is that the capacitive current resulting from dV/dt, triggers the parasitic BJT. However, as the voltages are low (dV/dt is more an issue > 600 V) a current/charge high enough to trigger the parasitic BJT cannot be generated.

9.7.4 Q: What diode or other parameters are important to assess susceptibility? For example, maximum dV/dt and maximum I_F.

A: High dV/dt can induce glitches onto the gate of the MOSFET. A snubber can help to reduce dV/dt and the magnitude of the V_{ds} spike if significant. The ratio of C_{oss} at low V_{ds} compared to C_{oss} value at high V_{ds} is an indicator of the non-linearity of C_{oss}. A very high ratio can indicate that the device can generate a high dV/dt. Gate driver circuit design can reduce the gate glitch, see **Section 9.7.1.** The ratio of Q_{gd} to Q_{gs} and the gate threshold voltage can be used to indicate the susceptibility of the device to gate glitches.

9.7.5 Q: Is trench technology sensitive to this phenomenon?

A: In theory, all MOSFETs are.

Additional information

dV/dt induced turn-on of the parasitic bipolar transistor is not known as an issue in low voltage NXP MOSFETs. If UIS parasitic turn-on is solved, then dV/dt induced turn-on is also solved. Refer to **Section 9.6.1** and **Section 9.6.3** for more information.

9.7.6 Q: Does a soft recovery body diode give lower dV/dt and if so, how is it designed and fabricated into the part?

A: Soft recovery does reduce the dV/dt. Although dV/dt is not an issue for the MOSFET, a lower dV/dt is better for EMI, voltage spikes and crosstalk. The design and manufacture is very specialized, involving proprietary information.

9.7.7 Q: How does temperature influence this sensitivity to dV/dt and why?

A: At high temperatures, it is easier to trigger a parasitic bipolar as its V_{be} reduces. But if the BJT is effectively shorted out and current diverted away from it, as discussed in **Section 9.6.1**, then it is not an issue.

9.7.8 Q: Can NXP provide R_b, C_{db}, V_{be} saturation values in the parasitic BJT model, as shown in **Figure 7**?

A: These values are required to be able to calculate **Equation 6**. The aim is to obtain a dV/dt value to check if parasitic BJT turns on, leading to device failure. It is impossible to measure the characteristics of the parasitic bipolar transistor as its terminals cannot be accessed independently of the MOSFET terminals. A parasitic bipolar transistor is always created when a MOSFET is fabricated. Referring to **Figure 7**, it can be seen that there are two current paths which could cause MOSFET problems. Current I_1 flows via C_{gd} and depending on C_{gs} and R_g it can cause the MOSFET to switch on momentarily. It is often referred to as a "gate glitch". Current I_2 flows via C_{db} and R_b which can potentially switch on the parasitic BJT

(5) $$V_{gs} = I_1 * R_g = R_g * C_{gd} * dV/dt$$

(6) $$V_{be} = I_2 * R_b = R_b * C_{db} * dV/dt$$

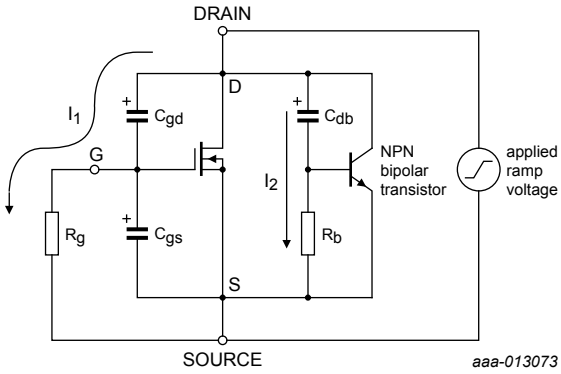


Fig 7. Power MOSFET showing two possible mechanisms for dV/dt induced turn-on

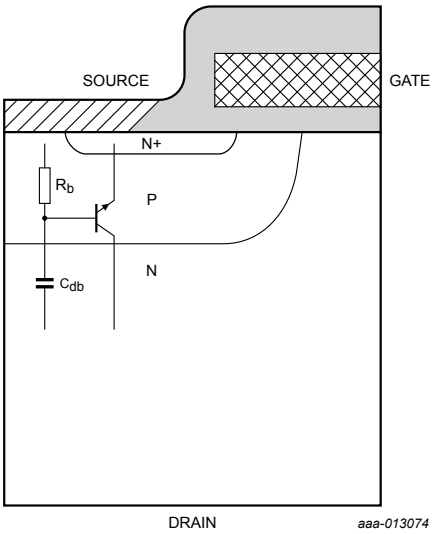


Fig 8. Physical origin of the parasitic BJT components that may cause dV/dt induced turn-on

Additional information

Early lateral MOSFETs (structure shown in **Figure 8**), were susceptible to failure caused by the turn-on of this parasitic transistor.

However, TRENCH MOSFETs, as manufactured by NXP, are much more immune to this failure mechanism.

The gate structure is located in trenches in the die surface rather than it being a horizontal layer on the die surface. This structure means that the short-circuiting of the base emitter junction of the parasitic bipolar transistor (to prevent its turn on), is much more effective.

As the generations of Trench MOSFETs have progressed, feature dimensions (trench pitch) have reduced, making the parasitic bipolar transistor even more immune to being turned on.

Figure 9 shows the structure of a Trench generation 6 device. The parasitic bipolar inhibition is particularly good in this structure due to the very short base to emitter length. The source metal short-circuits the p-n junction near the source contact, making it very hard to get a high enough V_{BE} to turn on the parasitic BJT.

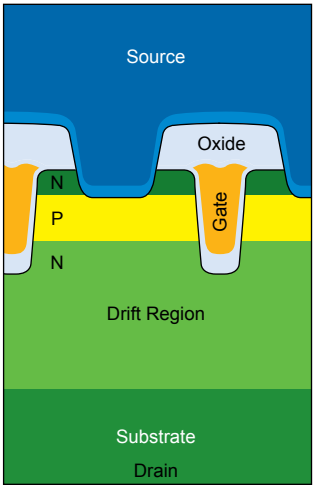


Fig 9. Trench generation 6 structure

9.8 Package and mounting

9.8.1 Q: On the drawing for the Power SO8 / LFPAK56 common footprint, there are no vias on the exposed pad. Are the addition of vias advised and, if so, which diameter?

A: If improved thermal resistance is required, vias can be added to the footprint. The effect of adding vias is discussed in **Section 4.3.5** of Chapter 4.

Additional information

NXP has used 0.8 mm successfully but it does not mean that other sizes would not work.

The vias should be pre-filled with solder and hot air leveled, to give a flat surface, before the devices are placed.

If the vias are not pre-filled, there is a chance that the solder under the part is drawn into the via, which may result in voids.

The extra process steps on the PCB and the potential problems mean that vias should not be used unless they are needed. Please consult the manufacturing process engineers regarding surface mount and soldering process issues.

9.8.2 Q: How are devices tested for HV isolation tests? An application is tested at approximately 1 kV for HV isolation testing across various terminals and a significant value is seen across the MOSFET. Are there tests that perform HV isolation analysis and, if so, what are they?

A: We do not perform any HV isolation tests on any automotive MOSFETs or specify any HV isolation parameter in our data sheets. Insulation testing is only applicable to TO220F packages (NXP SOT186A)

Additional information

HV isolation is specified for MOSFETs with insulated drain tabs or in modules with isolated bases. The test voltage applied in the NXP factory is 2.45 kV for 0.4 seconds (V_{rms} at 50 Hz).

9.8.3 Q: The efficiency of my DC-to-DC converter exceeds my requirements. Can I use smaller, higher RDS MOSFETs to save money?

Environmental conditions: 4-Layer FR4 board at 105 °C ambient.

A: Although it is possible to reduce efficiency, other factors become the constraints.

Additional information

The dominating factor is likely to be the temperature allowed at the solder joint between the MOSFET and the PCB. It is unlikely that 125 °C may be exceeded with FR4. If the dissipation is 2 W, the thermal resistance of the path from the MOSFET mounting base to ambient must be <10 K/W. (125 °C - 105 °C)/2 W = 10 K/W

Some special arrangements are required to achieve this figure. However the customer has indicated an allowed dissipation of 2 W so they may have some more information about their system indicating that it is achievable.

If dissipation is increased to 5 W, the temperature at the mounting base reaches 155 °C which is probably not allowed. The alternative would be to improve the thermal resistance to <4 K/W, which is extremely challenging.

Guidance on what can be achieved is given in Chapter 4 and Chapter 5.

The junction temperature of the MOSFET has not yet been mentioned. It is because it is only a few degrees higher than the mounting base. For example, consider an application for an LFPAK56 device, such as BUK7Y7R6-40E. The thermal resistance is 1.58 K/W. So for 2 W, the Tj would be 128.2 °C. For 5 W, it would be 133 °C (assuming T_{mb} can be held to 125 °C). Both of these values are well below the $T_{j(max)}$ of the MOSFET which is 175 °C.

So in summary, the limiting factor of what can be done with dissipation is the PCB and its thermal path to ambient, not the MOSFETs.

9.8.4 Q: What is the position of NXP on using Pb free solder for internal soldering (die attach, clip attach)?

A: NXP is a member of the DA5 working group. It is a project consortium comprising NXP, Bosch, Infineon and ST. The goal is to find new solder materials or alternative die attach methods which do not use lead. The European directive 2011/65/Eu exemption (RoHS), allows the use of lead in high melting point solders until 2016. So far, no reliable and cost effective alternative process has been developed, especially where the requirements of AEC Q101 are considered. An extension to the expiry date of this exemption was applied for in January 2015 by representatives of the electronics industry, including the DA5 working group.

The End of Life Vehicle (ELV) Directive (2000/53/EG) also applies. A similar extension to the Pb free exemption was applied for by the DA5 group in November 2013. It is expected that if approved, this directive allows the use of Pb based solders until 2018 at the earliest. It has been requested that the EU aligns the Pb free exemption between the ELV directive and the RoHS directive.

9.9 SPICE models

9.9.1 Q: Is there is a large difference between the data sheet and the SPICE model behavior and in particular, the gate charge characteristics?

A: There is quite a good similarity between the data sheet characteristics and the NXP SPICE models at 25 °C, especially for transfer curve, R_{dson}, diode characteristic and gate charge. The SPICE model also accounts for the package parasitic resistances and inductances.

Additional information

In PWM circuits, the SPICE model gives quite a good similarity to the behavior of the real device. The SPICE model can therefore be used to give a good indication of the switching losses at turn on and turn off, as well as the conduction losses.

The SPICE model is only correct at 25 °C, the R_{dson} versus temperature characteristic can be used to estimate conduction losses at higher temperatures. Switching losses are known not to change significantly with temperature.

The SPICE model also reflects a “typical device” according to the data sheet characteristics.

The method of creating models has been continuously improved over time. The latest model creation process used for Trench generation 6 devices and newer technologies results in models which closely match measured device behavior.

9.10 MOSFET silicon technology

9.10.1 Q: What is drift engineering?

A: Drift engineering is optimizing of the drift region between the bottom of the trench and the epi/substrate interface (light green area). The drift region supports most of the drain-source voltage in the off state. The purpose of drift engineering is to reduce the resistance of the drift region while maintaining the breakdown voltage BV_{dss} capability (see **Figure 10**).

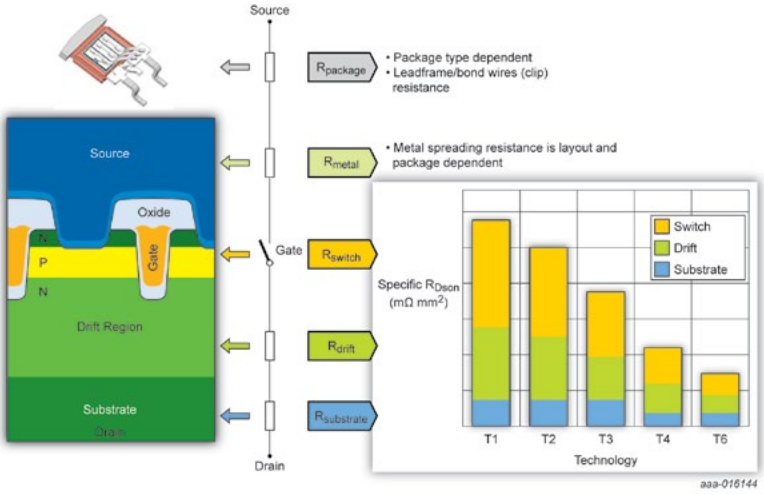


Fig 10. Resistance in power MOSFETs

9.10.2 Q: What is obtained from reduced cell pitch?

A: Reduced cell pitch generally results in lower resistance and higher capacitance. The goal of each new generation of MOSFET technology is to reduce R_{dson} without a large increase in capacitance that usually accompanies reduced cell pitch. Reduced cell pitch also reduces SOA capability (linear mode operation) but improves avalanche capability.

9.10.3 Q: What is obtained from a shorter channel?

A: Shorter channel gives a lower R_{dson} and a lower C_{gs} capacitance simultaneously. It has higher leakage current and the transfer curve (I_d versus V_{gs} characteristic) becomes more dependent on V_{ds}. It is also observed in the output characteristics.

9.10.4 Q: What is obtained from thick bottom oxide?

A: Thick bottom oxide refers to gate oxide at the bottom of the trench (see **Figure 10**). It is made thicker than the gate oxide at the side of the trench. It acts as a thicker dielectric between the gate and the drain resulting in a much lower C_{gd} value.

9.11 Supply and availability

9.11.1 Q: What statements can be made concerning the long-term availability of previous generations of TrenchMOS parts?

A: NXP continues to supply older products where the volumes of manufacture are economically viable, the sales price margin is commercially viable and there are no manufacturing reasons which prevent manufacture.

A Discontinuation of Delivery (DOD) document notifies key customers (including distributors), when a part is planned to be withdrawn. It allows customers to make arrangements to buy sufficient products for future requirements and if necessary qualify alternative products.

9.12 EMC

9.12.1 Q: If EMC issues are encountered when substituting Trench generation 6 parts for competitor parts, what advice is available? Can the application note *AN11160 Designing RC snubbers* help?

A: In this case, optimizing the RC snubber for the NXP MOSFET is necessary.

Additional information

EMC performance depends on many factors, some of which depend on layout parasitics, circuit components and the power MOSFET. For applications such as half bridges, 3 phase inverters, DC-to-DC converters etc., a snubber is often needed. It helps to reduce oscillations across the MOSFET drain and source terminals to acceptable levels. These oscillations would travel along conductors which can act as antennae. However, the snubber for the incumbent part is likely to be different from what is needed for the NXP device. It is because the MOSFETs are made from different technologies with different dynamic characteristics.

We would recommend following the process described in *AN11160* (Chapter 6 in this book) that was written specifically for these situations.

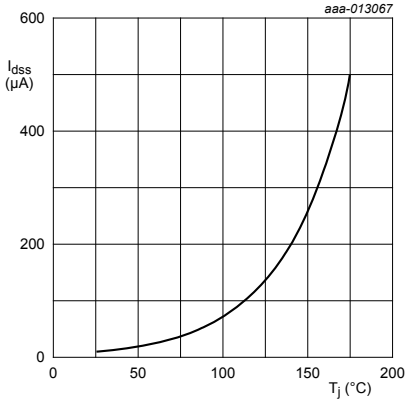
9.13 Leakage, breakdown and MOSFET characteristics

9.13.1 Q: How does quiescent current (I_{dss}) vary with respect to temperature?

A: The fundamental relationship between drain leakage current and temperature is exponential in form. The data sheet gives maximum values of I_{dss} at T_j = 25 °C and 175 °C. This example is specific to NXP Trench generation 2 technology but the same principles can be applied for other NXP technology. An exponential fit to these points provides the plot of **Figure 11**. It is also in line with some testing which is performed during the development of new MOSFET technologies.

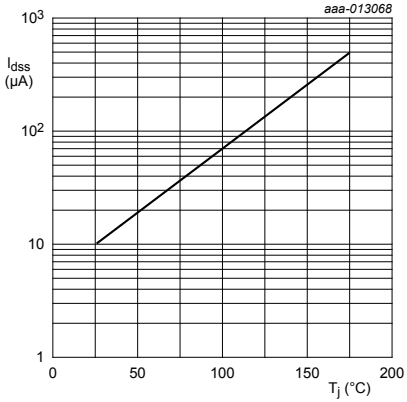
Additional information

Figure 12 is the same curve, plotted with a Log scale for I_{dss} to ease reading the value of 20 µA at 50 °C. These values are for a V_{ds} at the rated voltage. Reducing voltage reduces leakage current.



I_{dss} = 10 µA (25 °C), I_{dss} = 500 µA (175 °C),

Fig 11. I_{dss} as a function of temperature, linear axes



I_{dss} = 10 µA (25 °C), I_{dss} = 500 µA (175 °C),

Fig 12. I_{dss} as a function of temperature, log - linear axes

9.13.2 Q: What is the relationship between breakdown voltage (BV_{dss} at I_d = 250 µA) and drain leakage current (I_{dss})? Both state the same V_{dss} value but the drain current is different.

A: Although these two parameters reference the voltage rating of the part, they look at different characteristics of the product. Drain leakage current (I_{dss}) looks at the characteristic for V_{ds} at the rated voltage. The test applies a voltage, and checks that the current is below the limit.

Additional information

The breakdown voltage of a device (BV_{dss}) is the V_{ds} required to cause a drain current of 250 µA to flow. It is slightly higher than the rated voltage of the device and the actual voltage varies for the same nominal type due to manufacturing variations. The minimum stated in the data sheet is the rated voltage. Breakdown voltage looks at the characteristic of the part when it is in avalanche. The mechanisms causing leakage current and avalanche current are different.

9.13.3 Q: Is the standard level gate device BUK7Y28-75B guaranteed to work with a 7 V gate drive at -40 °C for 25 A?

A: NXP has a high degree of confidence that this scenario would be OK even in the worst case. However, it cannot be 100 % guaranteed by a production test at 25 °C.

Additional information

Referring to **Figure 13**, the typical gate threshold voltage $V_{gs(th)}$ is 3 V. It rises to approximately 3.5 V at -55 °C (i.e. a rise of approximately 0.5 V). The highest $V_{gs(th)}$ rises from approximately 4 V to 4.5 V (again, approximately 0.5 V). So in the worst case at -55 °C, the threshold voltage shifts by 1.5 V from the typical 25 °C value.

Looking at **Figure 14**, it would shift the gate drive curve from 7.0 V to 5.5 V for a worst case device (1.5 V shift).

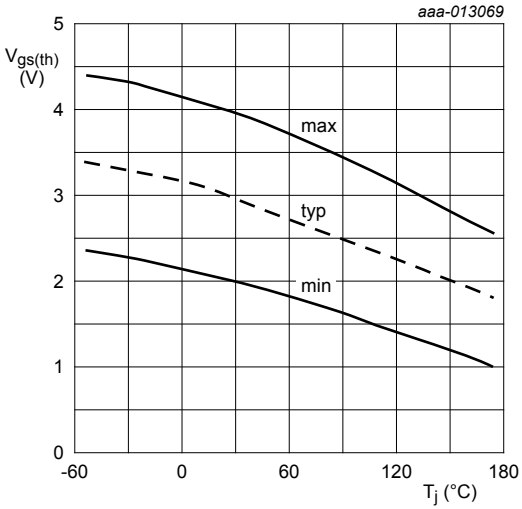
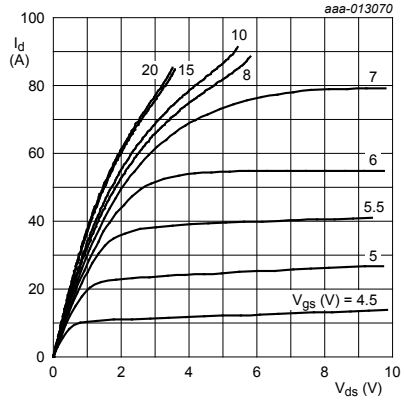
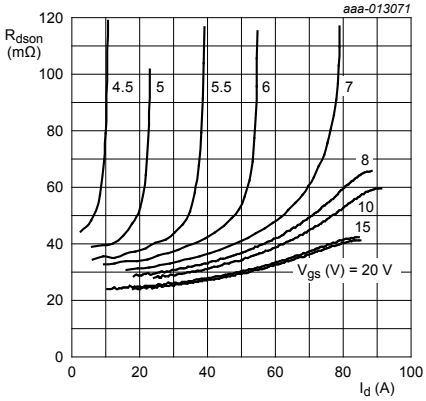


Fig 13. V_{gs} threshold as a function of temperature



$T_j = 25$ °C

Fig 14. Drain current as a function of drain-source voltage: typical values



$T_j = 25$ °C

Fig 15. Drain-source on-state resistance as a function of drain current: typical values

The 5.5 V drive curve allows more than 25 A and is still in the linear (R_{dson}) region of the output characteristic.

The R_{dson} values for the 5.5 V characteristic at 25 A in **Figure 15** is pessimistic for operation at -40 °C. It uses the 25 °C R_{dson} curves, and the mobility increases with lower temperatures making the R_{dson} better. The threshold voltage increase has already been accounted for.

It explains why a 7 V gate drive at -40 °C would be OK for this particular standard level gate device (BUK7Y28-75B). The same principles can be applied to other NXP devices. However, the customer must judge whether there is adequate margin in the design, as the result may be slightly different from what is observed.

9.13.4 Q: What is the lowest voltage (BV_{dss}) to be expected at -40 °C for a 40 V device using Trench generation 6?

A: The following principle could be applied to any NXP MOSFET technology at any breakdown voltage rating. In the data sheet, the values for minimum drain-source breakdown voltages are specified at -55 °C and 25 °C. The correlation between BV_{dss} and temperature is approximately linear over this range. Therefore, a straight line can be plotted at Temperature (-55 °C and 25 °C) versus BV_{dss} (at -55 °C and 25 °C).

For example: a 40 V Trench generation 6 part, has a BV_{dss} at -55 °C of 36 V and 40 V at 25 °C. Using linear interpolation, gives a BV_{dss} of 36.75 V at -40 °C.

9.13.5 Q: What factors affect the value of I_d current according to the transfer characteristic graph for BUK9275-55A, especially over the V_{gs} range of 2.2 V - 3.0 V?

A: The answer to this question is not simple - there are several factors which would affect the I_d value.

1. The graph depicted in **Figure 16** is typical. The BUK9275-55A MOSFET has a distribution of parameter values within the production tolerance limits. The graph is only intended to illustrate how I_d, V_{ds} and V_{gs} are related when the MOSFET is operating for a particular V_{ds} condition. $V_{gs(th)}$ has a significant influence on the characteristic of a particular device. Temperature is also a major factor. The limiting values and characteristics listed in the data sheet should be used for circuit design.
2. Junction temperature T_j strongly affects the I_d / V_{gs} characteristic. The graph in **Figure 16** is for T_j = 25 °C and T_j = 175 °C. The same graph for the same part with T_j = -55 °C, would be very different. The mode of operation preferred by the customer is with V_{gs} in the range 2.2 V to 3 V in the saturation region before full enhancement. In this mode, the MOSFET power dissipation is likely to be significant. As a result, the junction temperature may be high. **Figure 16** demonstrates how I_d changes with T_j for a given V_{gs} value.
3. A dashed vertical red line on the graph is shown at V_{gs} = 2.2 V. If T_j increases from 25 °C to 175 °C, I_d approximately doubles (from approximately 1 A to 2 A). However, at V_{gs} = 2.8 V (dashed vertical green line), the same junction temperature change has no effect on I_d. At V_{gs} > 2.8 V, an increase in T_j results in a decrease in I_d.

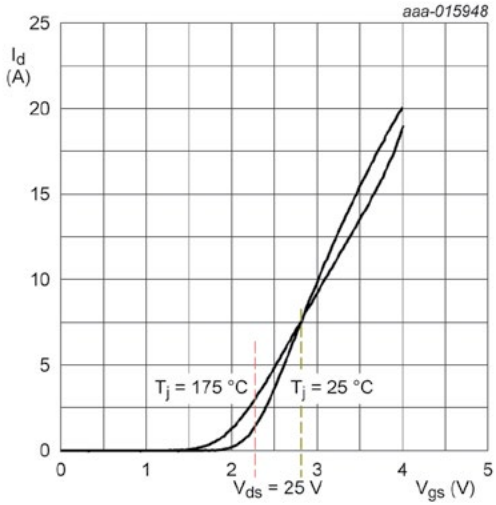


Fig 16. Transfer characteristics: drain current as a function of gate-source voltage - typical values

It is clear that the relationship between the MOSFET parameters is complex and their relationship with the thermal environment is also complex.

9.13.6 Q: Can NXP provide C_{gd}, C_{gs} and C_{ds} numerical values for T_j = -55 °C and T_j = +175 °C (at V_{gs} = 0 V, V_{ds} = 16 V)? If it is impossible to test, a theoretical one is also acceptable. A graph is provided in **Figure 17**, but it is for T_j = +25 °C.

A: Unfortunately NXP cannot supply values for these capacitances at the extremes of the MOSFET operating temperature range requested. It is due to the limitations of our parametric test equipment. However, we can comment on how these capacitances vary with temperature and the MOSFET terminal voltages.

Additional information

C_{iss} is the input capacitance formed by the parallel combination of C_{gs} and C_{gd}, and C_{gs} dominates. C_{gs} is formed across the gate oxide so it does not vary significantly with temperature or the MOSFET terminal voltages. As C_{gs} depends on gate oxide thickness and other defined die feature dimensions, it should not vary much between samples.

C_{rss} is the reverse transfer capacitance which is essentially the Miller capacitance (C_{gd}). It is formed across the MOSFET body diode depletion layer. This layer becomes thicker, as the reverse voltage (V_{ds}) across it increases. C_{rss} increases as V_{ds} decreases. C_{rss} has a greater variability than C_{iss} because it depends on the body diode depletion layer.

C_{oss} is the output capacitance. The Miller capacitance (C_{gd}) also dominates this capacitance. It varies with V_{ds} in a similar way to C_{rss} varying with V_{ds} and it has similar variability to C_{rss} for the same reasons.

These relationships are illustrated on the data sheet graph depicted by **Figure 17**. It has been observed that switching losses only slightly increase at T_j max, in the order of 10 %, since the capacitances only marginally change. Other factors can influence switching behavior, especially should the gate driver current capability change significantly with temperature. The depletion layer thickness varies in proportion to the square root of the absolute temperature in K and it affects C_{rss} and C_{oss}.

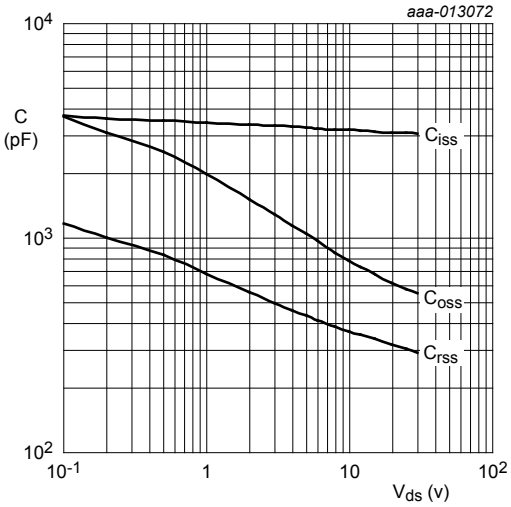


Fig 17. Input, output and reverse transfer capacitances as a function of drain-source voltage: typical values, V_{gs} = 0 V

9.13.7 Q: Can NXP provide the minimum V_{gs} threshold values for T_j from -55 °C to +175 °C? A graph is already in the data sheet. However, the numerical data of minimum values in the range of -55 °C to +175 °C are required for a standard level gate threshold.

A: Worst case values of min and max $V_{gs(th)}$ should be used for design purposes. They are given in the data sheet Characteristics (see **Table 1**).

Additional information

Table 1. Limiting values

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{gs(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{ds} = V_{gs}; T_j = 25 °C	2.4	3	4	V
		I_D = 1 mA; V_{ds} = V_{gs}; T_j = -55 °C	-	-	4.5	V
		I_D = 1 mA; V_{ds} = V_{gs}; T_j = 175 °C	1	-	-	V

These values are guaranteed worst case values. In this case, the 175 °C minimum $V_{gs(th)}$ is not less than 1 V. The -55 °C $V_{gs(th)}$ is not greater than 4.5 V.

9.13.8 Q: Can NXP provide the inherent R_g component value with T_j from -55 °C to +175 °C?

A: The measured R_g value is in the range of 1 Ω - 3 Ω and it does not vary significantly with temperature. In our general MOSFET characterization, it is presently not possible to test R_g over the temperature range.

Additional information

In a circuit such as the 3-phase motor drive circuit, switching speed is not usually critically important. The PWM frequency is usually moderate (<50 kHz). However, to mitigate emissions due to high dV/dt, the circuit designer often deliberately slows the switching of the MOSFET.

A low value (10 Ω) fixed resistor connected between the gate driver output and the MOSFET gate helps to stabilize the gate driver voltage and damp out any voltage transients or oscillations.

Often, even higher external gate driver resistor values are chosen to slow down the gate driver and reduce the EMI effects of the MOSFET switching.

9.14 MOSFET reliability

9.14.1 Q: How is the FITS-rate calculated?

A: FIT (failure in time) is commonly used to express component reliability and is defined as the number of failures occurring in 1 x 10^9 hours (1 billion hours).

At any elapsed time (t), the reliability (R) of a group of operating semiconductors is:

$R(t) = (n_o - n_f)/n_o$

Where:

n_o is the original sample size and nf is the number of failures after time t.

Over the standard time of 10^9 hours, it approximates to $F = (1/n_o)*(n_f/t)*10^9$.

Accelerated testing

A major factor in determining the reliability of a semiconductor is the total stress applied by the application. Operating temperature, resulting from ambient temperature and the heat due to power dissipation, is the most important applied operating stress where a product is otherwise generally operated within its ratings.

The Arrhenius equation is used to model the effect of temperature on component failure rate:

(7) $$\text{Acceleration factor} = e^{(EA/k)*(1/T1 - 1/T2)}$$

Where:

EA = activation energy (eV)

k = Boltzmann constant (8.60 - 10^{-5} eV / K)

T1 = operating temperature (°C)

T2 = reliability test temperature (K referenced to absolute zero)

Accelerated testing makes components perform at high levels of (thermal) stress. The results are then extrapolated to convert short life under severe conditions into the expected life under normal conditions.

Under accelerated life test conditions:

(8) $$F = (n_f / n_o * A * t) * 10^9 \text{ FITs}$$

Time t now becomes A*t, where A is the acceleration factor.

Based on the life-test results for an example part, the FITs data provided in **Table 2** has been calculated. Note that an adjustment is made to the number of failures based on Poisson's probability distribution, to indicate the number of failures expected in a larger sample depending on the confidence level. It is described in *JEDEC JEP122F section 5.18.1.4* and in numerous other references

Table 2. Calculated FITs data

Test name	High Temperature Reverse Bias (HTRB) + High Temperature Gate Bias (HTGB) + High Temperature Storage Bias (HTSL)				
Test temperature	175	°C			
Number of device hours	35,051,000				
Number of observed failures	0				
Confidence level	90	%			
Activation energy	0.7	eV			
Failure rate at	125	°C	at 90 % confidence =	6.725	FITs
Failure rate at	85	°C	at 90 % confidence =	0.688	FITs
Failure rate at	55	°C	at 90 % confidence =	0.086	FITs
Failure rate at	25	°C	at 90 % confidence =	0.0007	FITs
Mean time before failure at	125	°C	at 90 % confidence =	1.49×10^{8}	hours
Mean time before failure at	85	°C	at 90 % confidence =	1.49×10^{9}	hours
Mean time before failure at	55	°C	at 90 % confidence =	1.49×10^{10}	hours
Mean time before failure at	25	°C	at 90 % confidence =	1.49×10^{11}	hours

Abbreviations

Symbol	Description
C_i	constituent thermal capacitance element
$E_{DS(AL)S}$	single-shot avalanche energy
EMC	ElectroMagnetic Compatibility
EOS	Electrical Overstress
ESD	ElectroStatic Discharge
$I_{DS(AL)R}$	repetitive avalanche current
$I_{DS(AL)S}$	single-shot avalanche current
I_{AL}	avalanche current
I_D	MOSFET drain current
I_d	MOSFET drain current
KGD	Known Good Die
L	inductance
LFPAK	Loss-Free Package
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NTC	Negative Temperature Coefficient
$P_{(t)}$	power as a function of time
PCB	Printed-Circuit Board
$P_{DS(AL)M}$	peak drain-source avalanche power
$P_{DS(AL)R}$	repetitive drain-source avalanche power
PTC	Positive Temperature Coefficient
PWM	Pulse Width Modulation
R_i	constituent thermal resistance element
R_{th}	thermal resistance
$R_{th(j-a)}$	device junction to ambient thermal resistance
$R_{th(j-mb)}$	thermal resistance from junction to mounting base

Symbol	Description
SMD	Surface-Mounted Device
SOA	Safe Operating Area
t_{AL}	avalanche period/duration
T_j	junction temperature
$T_{j(AV)}$	average junction temperature (For repetitive avalanche.)
$T_{j(init)}$	initial junction temperature (Summation of T_{mb} and ΔT_{on}.)
$T_{j(max)}$	maximum Junction temperature
T_{jrise}	junction temperature rise in the MOSFET
T_{mb}	mounting base/case temperature
UIS	Unclamped Inductive Switching
V_{BR}	breakdown voltage
$V_{(BR)DSS}$	drain-source breakdown voltage
V_{DS}	drain to source voltage of the MOSFET (also the case for V_{ds})
V_{GS}	gate to source voltage of the MOSFET (also the case for V_{gs})
V_{DD}	supply voltage
Z_{th}	device Transient thermal impedance
$Z_{th(t)}$	transient thermal impedance
$Z_{th(tAL)/2)}$	transient thermal impedance (Measured at half the avalanche period)
ΔT	change in temperature
ΔT_j	average temperature rise from average
$\Delta T_{j(max)}$	maximum junction temperature variation
ΔT_{on}	on-state temperature difference
τ	total time of heating pulse
τ_i	thermal time constant

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Page numbers in *italics* denote figures, those in **bold** denote tables.

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Legal Information

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