# HW Getting Started Guide

# MPC8568E MDS Processor Board

**Jun 2007: Rev. 0.5**

## Contents



## About This Document

This document shows how to connect the MPC8568E MDS Processor Board and verify its basic operation, in a step by step format. Settings for switches and jumpers are shown, as well as instructions for connecting peripheral devices. Instructions for connecting the MPC8568E MDS PB to an IDE, such as Freescale's *CodeWarrior*® are included, but instructions for working with the IDE are beyond the scope of this document.

## Required Reading

The *MPC8568 Reference Manual* has information on the chip, and the *MPC8568E MDS Processor Board User's Guide* has much more detailed information on the processor board. The *Kit Configuration Guide* has instructions on working with the software

## Definitions, Acronyms, and Abbreviations

| | | | |
|---|---|---|---|
| **BCSR** | Board Register | **MDS** | Modular Development System |
| **COP** | Debug port in PowerPC | **PCI** | Peripheral component interconnec |
| **DDR2** | Double data rate DRAM | **PLL** | Phase Lock Loop |
| **DIP** | Dual In-line Package | **QE** | Quick Engine, a block in the MPC83xx line of chips |
| **I2C** | Philips serial port | **SODIMM** | Type of memory device |
| **LED** | Light Emitting Diode | **Tu** | Time unit (0.95ns) |
| | | **USB** | Universal Serial Bus |

# MPC8568E MDS Processor Board

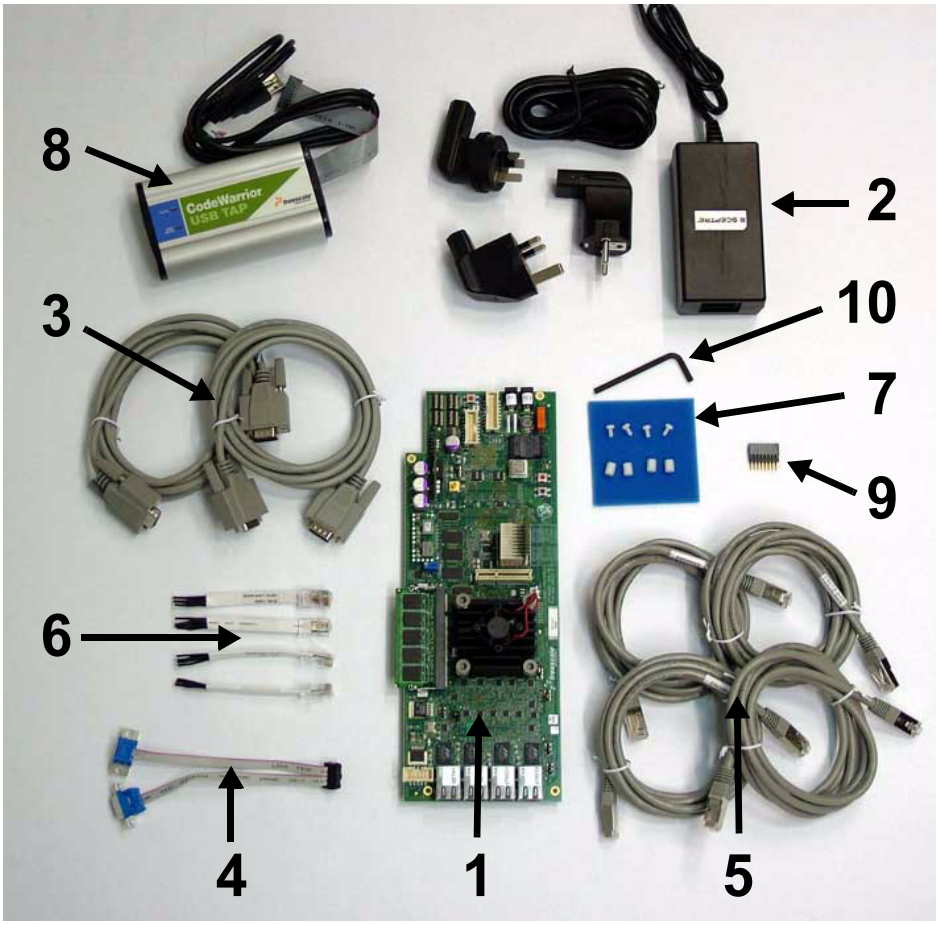
**HW Getting Started Guide**

## Step 1: Check kit contents

1. MPC8568E MDS Processor Board
2. AC/DC 5V/8A universal power supply kit
3. RS232 9-Pin cable (2)
4. Freescale adaptor cable (joined) with two RS232 connectors to single IDC 10-pin, for UART1/2
5. Giga-bit Ethernet cables (4) with RJ45-8 connectors
6. Giga-bit Ethernet loopback cables (4)
7. One set of four plastic spacers
8. CodeWarrior USB Tap
9. Interconnection header (used if programming the BCSRs via the USB Tap (For instructions on using this, see the *MPC8568E MDS User's Guide*.)
10. Allen wrench
11. MPC8568E MDS Processor Board documentation, software and tools (not shown)

*Optional (not shown):*

- PCI_PCIe adaptor card - required if using the MPC8568E MDS Processor Board as a PCI or PCIe agent. For instructions on using this, see the *MPC8568E MDS User's Guide*.
- PCI Panel - required if using the MPC8568E MDS Processor Board in a PC.

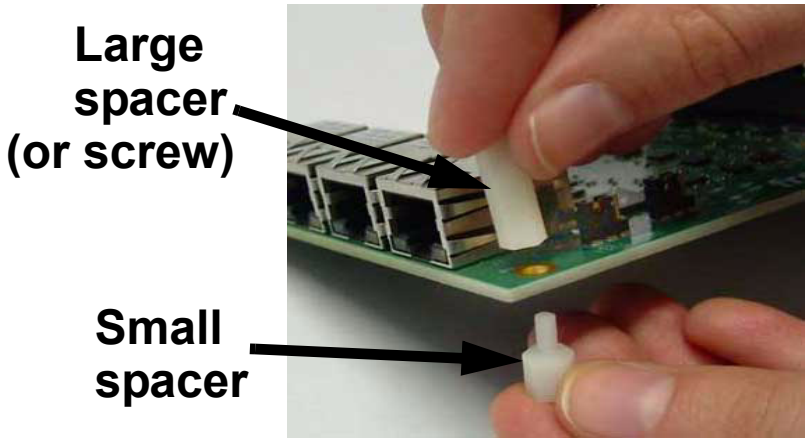


### Step 2: Connect plastic spacers

**Note: Perform this step only if you are using the processor board in a stand-alone mode.**

One set of four plastic spacers screw into holes located at (approximately) the four corners of the board.The spacers raise and stabilize the board.

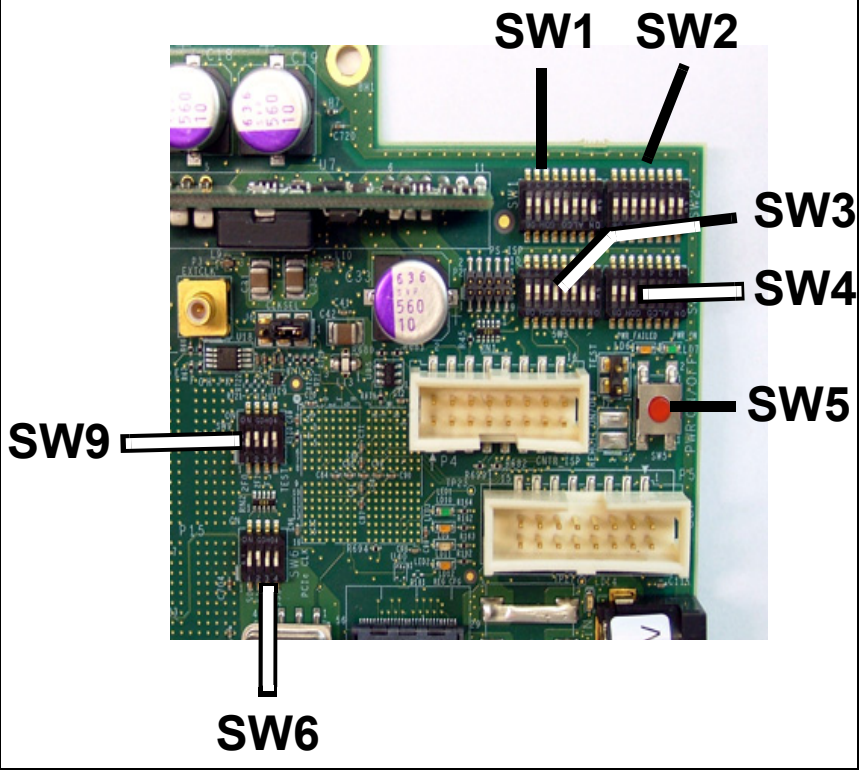
1. From the lower surface of the board, insert a smaller spacer into one of the board's four spacer holes.
2. Attach a larger spacer (or screw, if included in kit) onto the lower spacer, and screw it on.
3. Repeat for the three remaining spacers.

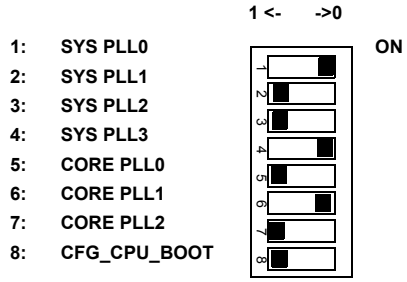
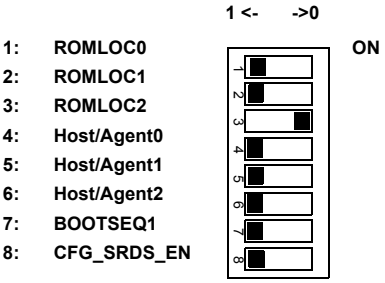
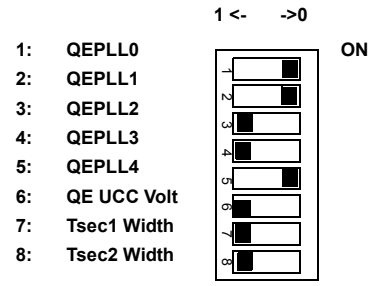


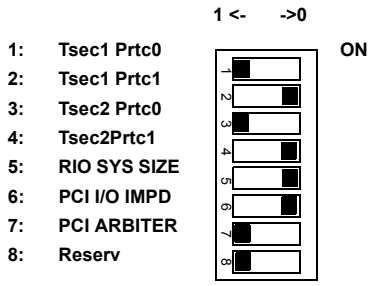
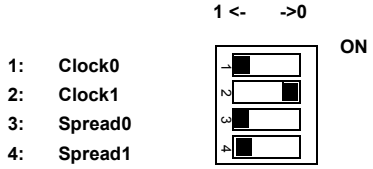
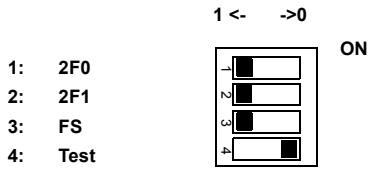
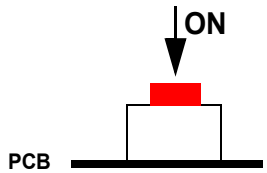

### Step 3: Check Switches

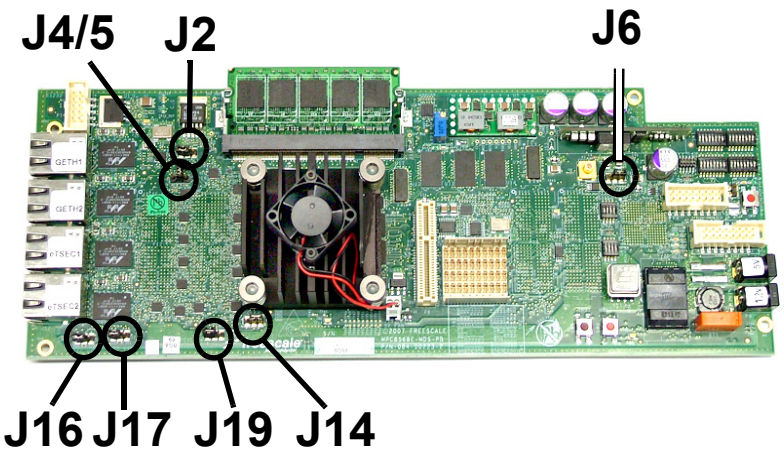
The Dual-In-Line Package (DIP) switches of the MPC8568E MDS PB are shown at right. The default DIP-switch positions set-up the MPC8568E MDS PB clock mode as shown in the table below:

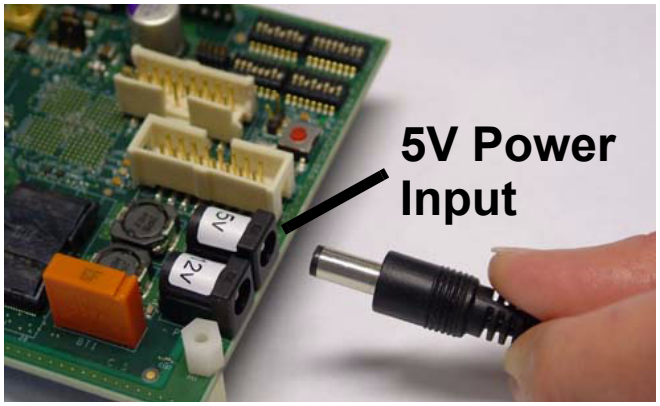
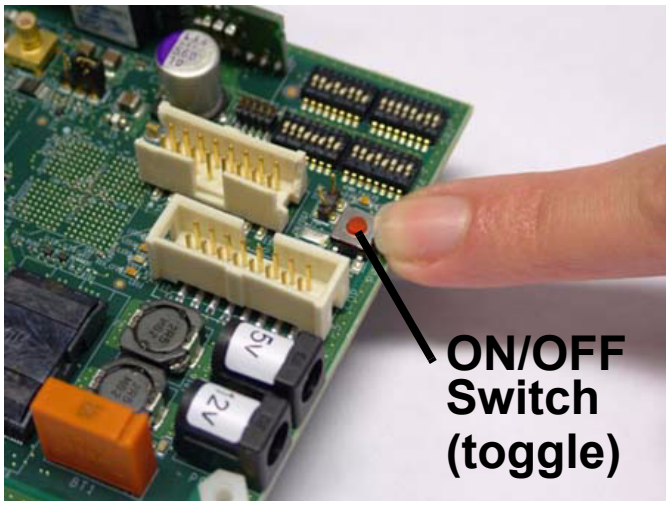
| MPC8568E MDS Processor Board Clock Mode *(default values)* | |
|---|---|
| Core Frequency | 1000 MHz |
| CCB | 400 MHz |
| DDR2 | 200 MHz |
| Local Bus<br>If LCRR = 0xXXXXXXX2 | 100 MHz |
| QE | 400 MHz |



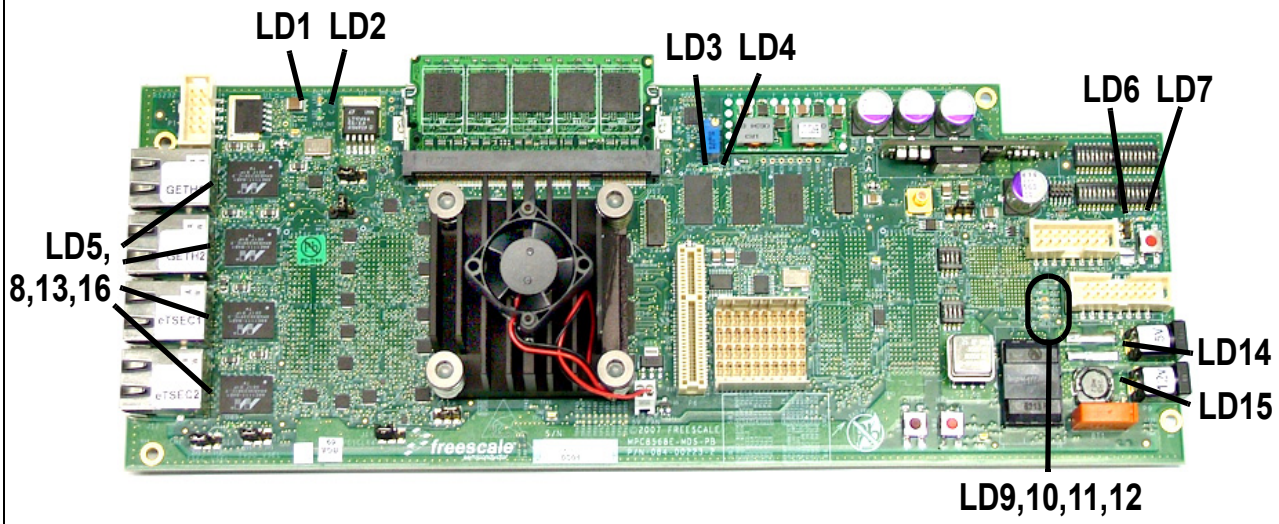
| | |
|---|---|
| **Step 3.a: SW1 Configuration**<br>  <br><br>The "On" DIP Switch position corresponds to a signal value of "zero". | **SW1.1-SW1.4: SYS PLL[0:3]**<br>Sets the platform frequency (CCB)<br>factory setting: '0110' = 400Mhz.<br>**SW1.5 - SW1.7: CORE PLL[0:2]**<br>Sets the multification factor for COR PLL = CCB * CORE PLL[0:2]<br>factory setting: '101' = 1066Mhz<br>**SW1.8 CFG_CPU_BOOT**<br>Enables/Disables the e500 core to boot without waiting for configuration by an external host<br>factory setting: '1' = enable the e500 to boot independently<br><br>Default setting: 01101011 |
| **Step 3.b: SW2 Configuration**<br>  <br> | **SW2.1-SW2.3: ROMLOC[0:2]**<br>Selects the Boot ROM location from one of the following locations: PCI, DDR2, SRIO,PCIe, Local bus<br>factory setting: '110' = Boot from Local Bus 16bit (Flash).<br>**SW2.4-SW2.6: Host Agent PCI,PCIe,SRIO selection. [0:2]**<br>factory setting: '111' = MPC8568 acts as the host processor/root complex.<br>**SW2.7 Boot Sequence1**<br>(Boot sequence[0] tied to '1') it is possible to from Extended I2C or to disable I2C Rom accessed.<br>factory setting: '1' = No I2C ROM is accessed.<br>**SW2.8: CFG_SRDS_EN**<br>Enables/Disables the SerDes interface<br>factory setting: '1' = enable the SerDes interface<br><br>Default setting: 11011111 |
| **Step 3.c: SW3 Configuration**<br>  <br> | **SW3.1-SW3.5: QE PLL setting [0:4]**<br>Sets the multiplication factor that is used to calculate QECLK from the input clock (SYSCLK) .<br>factory setting: '00110' for fcore = 400MHz.<br>**SW3.6: QE UCC Voltage**<br>Sets the voltage of UCC when it works with GETH<br>factory setting: '1' = UCC voltage = 3.3V<br>**SW3.7: Tsec1 Width**<br>Set to standard mode.<br>factory setting '1' for GMII.<br>**SW3.8: Tsec2 Width**<br>Set to standard mode.<br>factory setting '1' for GMII.<br><br>Default setting: 00110111 |

| | |
|---|---|
| **Step 3.d: SW4 Configuration**<br>  | **SW4.1: SW4.4 Tsec1,2_Prtc[0:1].**<br>Selects the eTSEC protocol: MII, GMII, or TBI<br>factory setting: '10' (GMII) for both eTSEC1 & eTSEC2.<br>**SW4.5: RIO SYS SIZE**<br>factory setting: '0' = Small system size up to 256 devices.<br>**SW4.6 PCI I/O Impedance:**<br>factory setting: '0' = 25Ohm I/O impedance.<br>**SW4.7 : PCI Arbiter.**<br>factory setting: '1' = The on chip PCI arbiter is enabled.<br>**SW4.8 : Reserved.**<br>factory setting: '1' = Reserved<br><br>Default setting: 10100011 |
| **Step 3.e: SW6 Configuration**<br>  | **SW6.1: SW6.2 PCI Express/sRIO Clock[0:1].**<br>Sets the clock value.<br>factory setting: '10' = 100MHz<br>**SW6.3: SW6.4 PCI Express/sRIO Clock Spread[0:1].**<br>Sets the spread value.<br>factory setting: '11' = No spread<br><br>Default setting: 1011 |
| **Step 3.f: SW9 Configuration**<br>  | **SW9.1: SW9.2 Skew Control [0:1].**<br>Sets the skew of the PCI clock.<br>factory setting: '11' = No skew<br>If using MPC8568E board as agent, this must be set to ‘10’ on host board<br>**SW9.3: PLL Frequency range.**<br>Sets the PLL frequency range.<br>factory setting: '1' = 48MHz - 100MHz<br>**SW9.4: Test.**<br>Disables output if skew = -4Tu (Tu = “time unit” = 0.95ns).<br>factory setting: '0' = disable output if skew = -4Tu<br><br>*This switch provides a digitally controlled delay of the PCI_CLK signal in order to provide stable operation of the board when it is a PCI agent*<br><br>Default setting: 1110 |
| **Step 3.g: SW5 Power Switch**<br>  | **SW5: power switch (toggle)**<br>• power from an external 5V power supply via the P10 power jack<br>• combined mode: powered from +5V on PIB power supply through riser connectors<br>• board plugged as a PCI add-in card: PC internal power supply will provide 5V via PCI edge connector |

| | |
|---|---|
| **Step 4: Check Jumpers**<br>Jumper locations are shown in the figure at right.<br><br>Check the default positions, as shown in the sub-steps below, and verify that the board is operational before changing any settings. |  |
| **Step 4.a: J2:**<br>3 TDMC-RXCLK<br>2 PD22 (CLK7)<br>1 UPC2-RXCLKIN | Selects input for CLK7: TDMC_RXCLK or UPC2_RXCLKIN<br><br>• For UPC2-RXCLKIN: Connect 1-2 (default)<br>• For TDMC-RXCLK: Connect 3-2 |
| **Step 4.b: J4 & J5:**<br>J5<br>3 RMII_RXCLKODD<br>PB31(CLK16) 2 GE125 J4<br>1 XUPC1_TXCLKO | Selects input for CLK16: RMII_RXCLKODD, GE125, or XUPC1_TXCLKO (J5/J4 is a 4-pin combined Jumper, configured as shown at left)<br><br>• For RMII_RXCLKODD: Connect (JP5) 2-3<br>• For XUPC1_TXCLKO: Connect (JP5) 1-2<br>• For GE125: Connect JP4 (default)<br><br>Note: GE125 is the input clock for UCC1 & UCC1 input 125Mhz clock. |
| **Step 4.c: J6:**<br>3 External clock<br>2 Input MPC8568 clock<br>1 OnBoard clock | Selects input clock for MPC8568E (onboard or external)<br><br>• For external clock: Connect 2-3<br>• For internal clock: Connect 1-2 (default) |
| **Step 4.d: J14:**<br>3 RMII_RXCLKEVEN<br>2 PD23 (CLK8)<br>1 UPC2_TXCLK | Selects input for CLK8: RMII_RXCLKEVEN or UPC2_TXCLK<br><br>• For RMII_RXCLKEVEN: Connect 2-3 (default)<br>• For UPC2_TXCLK: Connect 1 - 2. |
| **Step 4.e: J16:**<br>3 3.3V<br>2 TSEC VDD<br>1 2.5V | Selects input voltage for TSEC_VDD (3.3V or 2.5V)<br><br>• For 3.3V: Connect 2-3<br>• For 2.5V: Connect 1-2 (default) |
| **Step 4.f: J17:**<br>3 3.3V<br>2 QE UCC1&2 VDD<br>1 2.5V | Selects input power for QE UCC1&2 (MPC8568 QE GETH block) - 3.3V or 2.5V<br><br>• For 3.3V: Connect 2-3<br>• For 2.5V: Connect 1-2 (default) |

| | |
|---|---|
| **Step 4.g: J19:**<br>3 ⊗ MAC_HW-CP-G-T-SO5<br>2 ⊗ XUPC2_RXD9_PCICLK4<br>1 ⊗ XPCI_CLK4 | Enables PCI clock to be routed to the expansion board of the PIB<br>• For normal operation (no re-routing of PCI clock): Connect 1-2 (default)<br>• To route PCI clock to expansion board: Connect 2-3 |
| **Step 5: Assemble and connect the power supply kit.**<br>**Note:**<br>**Ensure the power is OFF.**<br>Assemble the AC/DC power supply kit:<br>• power cable with country-specific wall outlet plug<br>• power supply unit and cable with jack (for board connection)<br>1. Connect the AC/DC power supply cable with 5V jack on the board.<br>2. Plug the power cable into the wall outlet. |  |
| **Step 6: Perform initial board power up, and check LEDs.**<br>**Caution:**<br>**To prevent damage to the JTAG connectivity unit connect the unit only after initial board reset.**<br>1. Press the power button (SW5). LD1 briefly displays light.<br>2. Check for completion of the reset sequence-indicated by the LD2 being constantly lit, as well as LD7, indicating power on.<br>3. Shut off the power by pressing the power button (SW5) again. |  |

LED Locations:




LED Indicators meanings:

| No. | Name | Color | LED On | LED Off |
|---|---|---|---|---|
| LD1 | ASLEEP | Green | Device in PORESET or in sleep state | Device not in PORESET or sleep state |
| LD2 | TRIG_OUT | Red | Device ready after PORESET | Device not ready |
| LD3 | DDR2 | Green | Power supplied to DDR2 | No power supplied to DDR2 |
| LD4 | DDR1 | Green | Power supplied to DDR1 | No power supplied to DDR1 |
| LD5 | UCC1 | Green | GETH connected to UCC1 active | GETH not active |
| LD6 | Power Fail | Red | Power is not properly supplied to device | If board is active, power is properly supplied to device |
| LD7 | Power On | Green | Board power is ON | Board power is OFF |
| LD8 | UCC2 | Green | GETH connected to UCC2 active | GETH not active |
| LD9 | BCSR | Red | Connected to BCSR5 for debugging purposes | |
| LD10 | BCSR | Green | | |
| LD11 | BCSR | Amber | | |
| LD12 | REG-CFG | Red | Configuration from internal registers | Configuration from DIP switches |
| LD13 | eTSEC3 | Green | GETH connected to TSEC1 active | GETH not active |
| LD14 | Power 5V | Amber | 5V input active | 5V input not active |
| LD15 | Power 12V | Green | 12V input active | 12V input not active |
| LD16 | eTSEC4 | Green | GETH connected to TSEC2 active | GETH not active |

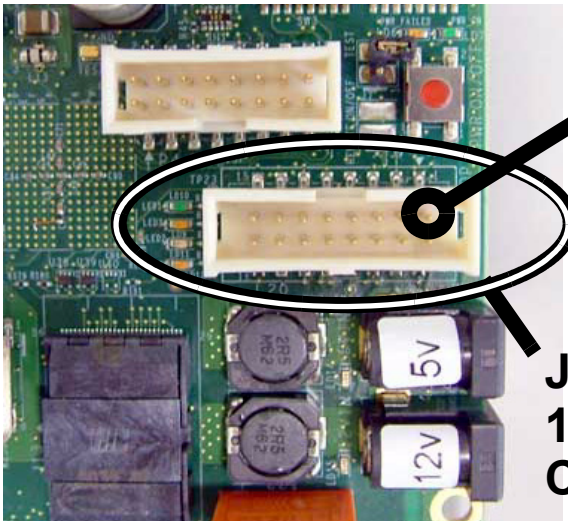
**Step 7: Connect the JTAG connectivity unit to the board.**

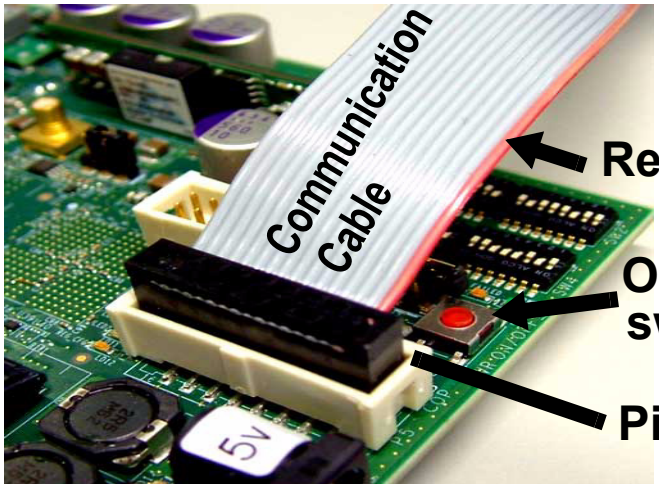
The JTAG connectivity unit ("USB Tap" ) enables the CodeWarrior software to work with the board.

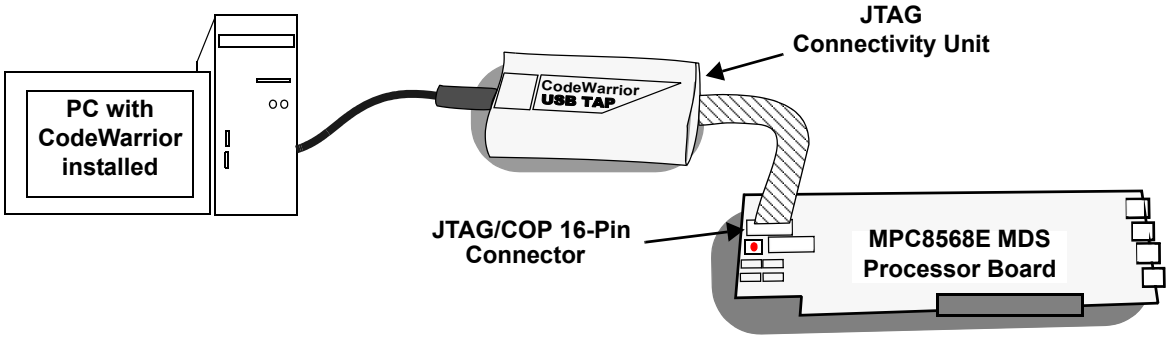
**CAUTION**

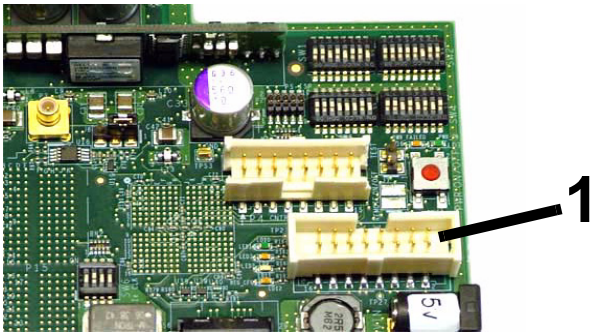
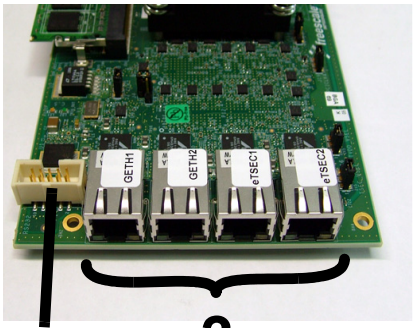
**The "USB-Tap" JTAG connectivity unit must be connected properly to the JTAG/COP 16-pin connector, as shown, otherwise sensitive devices may be damaged.**

1. Align the red stripe on the communication cable of the USB-Tap JTAG connectivity unit with Pin #1 on the JTAG/COP 16-pin connector.
2. Connect the cable to the JTAG/COP 16-pin connector.
3. Press the ON/OFF switch.
4. Check for completion of the reset sequence (see Step 6 on page 7).



| **Step 8: Attach remaining cables to the board according to your development needs.** |  <br>  |
|---|---|
| Connect the remaining cables to the board as per user development needs and planned board use:<br><br>1. JTAG/COP 16-pin connector for JTAG connectivity unit.<br>2. Port for the joined Freescale adaptor cable with two RS232 connectors<br>3. Giga-bit Ethernet ports for the four Ethernet cables with RJ45-8 pin connectors.<br>4. Continue work according to instructions in the *Kit Configuration Guide*. | |

***How to Reach Us:***

**USA/Europe/Locations Not Listed:**
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-521-6274 or 480-768-2130

**Japan:**
Freescale Semiconductor Japan Ltd.
Technical Information Center
3-20-1, Minami-Azabu, Minato-ku
Tokyo 106-8573, Japan
81-3-3440-3569

**Asia/Pacific:**
Freescale Semiconductor Hong Kong Ltd.
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
852-26668334

**Home Page:**
**www.freescale.com**