S32R294 EVB User Guide

Revision 2.0 (SCH-32157_B)

by: NXP Semiconductor

1 Introduction

This user's manual details the setup and configuration of the NXP S32R294 Evaluation Board (hereafter referred to as the EVB). The EVB is intended to provide a mechanism for easy customer evaluation of the S32R294 microprocessor, and to facilitate hardware and software development.

For the latest product information, please speak to your NXP representative.

The EVB is intended for bench / laboratory use and has been designed using normal temperature specified components (+70°C).

1.1 List of Acronyms

Table 1 provides a list and description of acronyms used throughout this document.

Table 1. List of Acronyms

Acronym	Description
ADC	Analog-to-Digital converter
RESET_B	External signal reset

Acronym	Description
EVB	Evaluation board
GND	Ground
HV	High voltage (1.8V and/or 3.3V)
LED	Light emitting diode
LV	Low voltage (0.82V)
MCU	Microcontroller
MPU	Microprocessor
OSC	Oscillator
POR_B	Power-on reset
PWR	Power
RX	Receive
SIPI	Serial Interprocessor Interface
TBD	To be defined
TX	Transmit
VSS	Ground
LCD	Liquid Crystal Display
PMIC	Power Management IC
FXOSC	Fast Crystal Oscillator

2 EVB Features

The EVB provides the following features:

- MCU (soldered or through a socket)
- Single 12V external power supply input with one NXP FS8510 PMIC providing all of the necessary EVB and MCU voltages; Power supplied to the EVB via a 2.1mm barrel style power jack; 12V operation allows in-car use if desired
- Master power switch and regulator status LEDs
- Flexible MCU clocking options allow provision of an external clock via adaptor board (MIPI-CSI0 connector) or 40MHz EVB clock oscillator circuit. Solder pads allow selection between these external clocks
- Boot mode selection via switches on board
- Standard 14-pin JTAG debug connector and 34-pin Nexus Aurora connector
- 10-pin Serial Interprocessor Interface (SIPI) connector
- Gb Ethernet Physical interface IC, with RJ45 connector
- Two MIPI-CSI2 connectors intended for use with TEF810X BEST3 RF front end board (via a separate adaptor board – X-S32R-TEF810X_ADPT)
- All MCU signals readily accessible at a port-ordered group of 0.1” pitch headers

- FlexRAY interface
- 3 CAN-FD interfaces:
    - 1x up to 8Mbps communication speed (CAN2)
    - 2x up to 5Mbps communication speed (CAN0, CAN1)
- UART to Micro USB interface
- 2 user switches and 4 user LEDs, freely connectable
- 256Mb (64MB) Serial NOR Flash memory
- 64Kb EEPROM connected to MCU via I2C
- 4*10-character LCD with DSPI interface (DSPI4)
- Liberal scattering of GND test points (surface mount loops) placed throughout the EVB
- User reset switch with reset status LED

NOTE

To alleviate confusion between jumpers and headers, all EVB 2-pin jumpers are implemented as 2mm pitch whereas 3/4/6-pin jumper and headers are 0.1inch (2.54mm). This prevents inadvertently fitting a jumper to a header.

CAUTION

Before the EVB is used or power is applied, please fully read the following sections on how to correctly configure the board. Failure to correctly configure the board may cause irreparable component, MCU or EVB damage.

3 Configuration

This section details the configuration of EVB's functional blocks.

The EVB has been designed with ease of use in mind and has been segmented into functional blocks as shown in Figure 1. Detailed silkscreen legend has been used throughout the board to identify all switches, jumpers and user connectors.

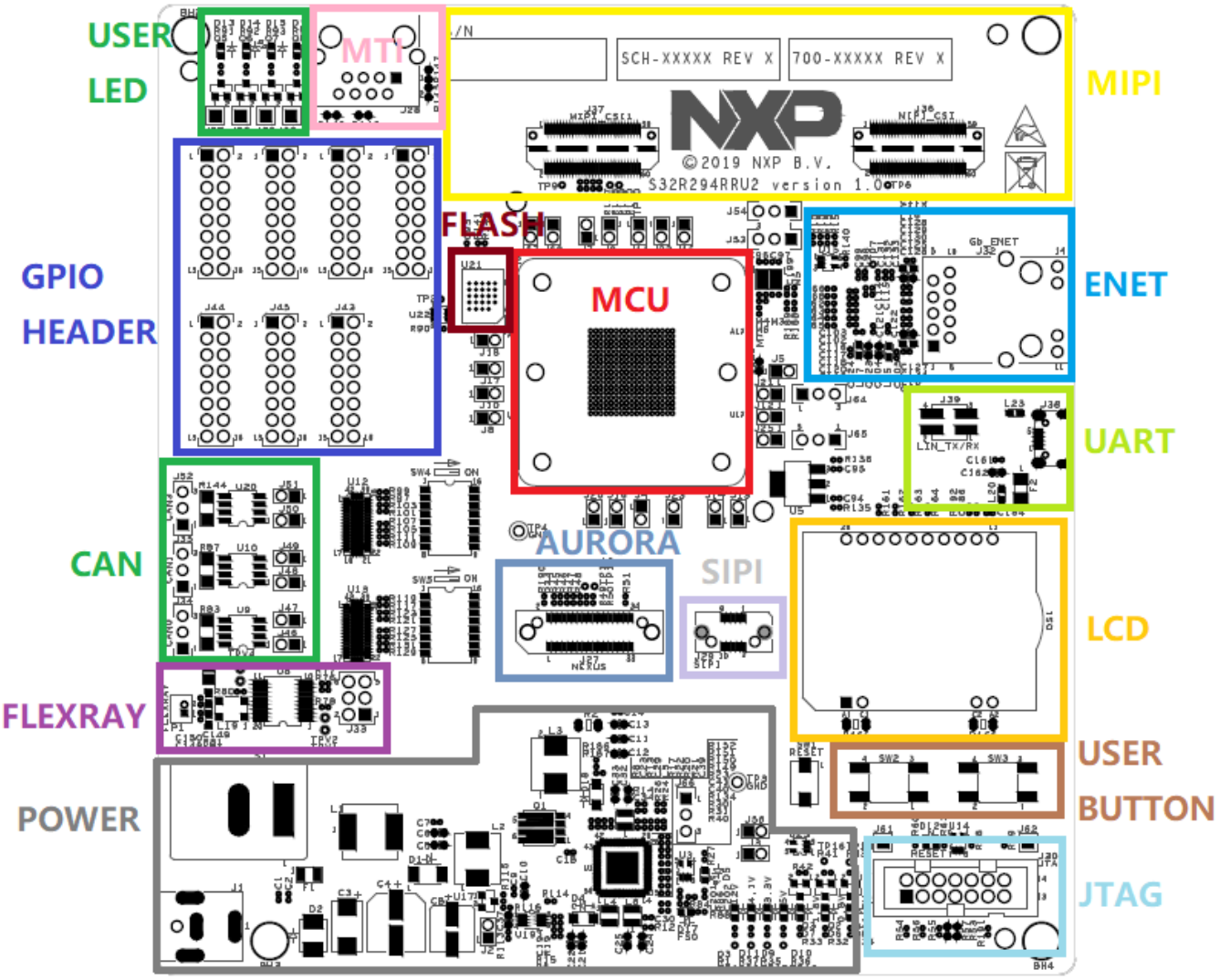

Figure 1. EVB - functional blocks

3.1 MCU Power

The EVB requires an external power supply voltage of 12V DC, minimum 1.5A. This allows the EVB to be easily used in a vehicle if required. The single input voltage is regulated on-board using the NXP FS8510 PMIC to provide the necessary EVB and MCU operating voltages of 0.82V, 1.8V, 1.2V, 3.3V and 5V, and one backup 3.3V linear regulator for ENET IO and ENET PHY.

3.1.1 Power Supply Connectors

2.1mm Barrel Connector – P26:

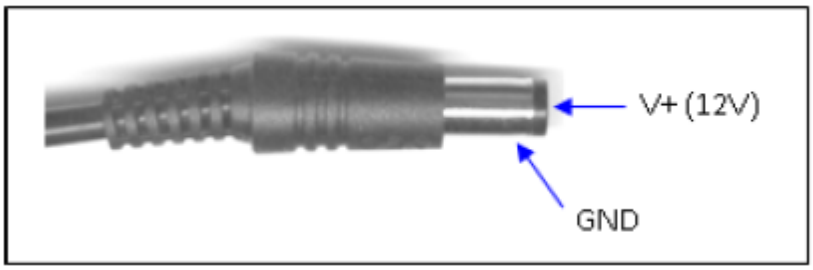

Figure 2. 2.1mm Power Connector

3.1.2 Supply Routing and Jumpers

The figure below shows how the MCU power domains are connected.

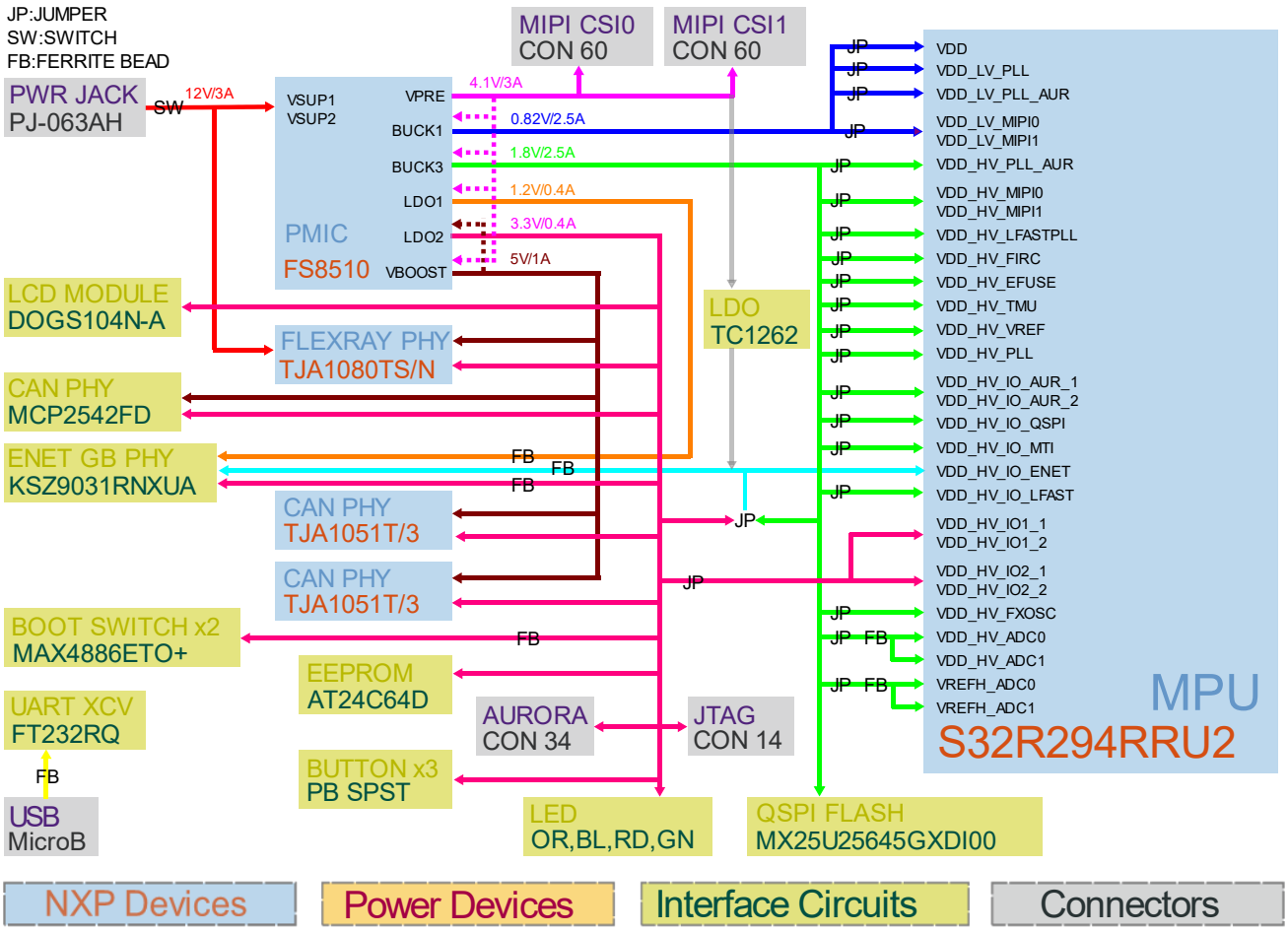

Figure 3. EVB power distribution

The connection of any power domain has to be enabled by a dedicated jumper as described in Table 2.

Table 2. MCU power selection jumpers

Jumper	Description
J4	Connects VDD Core supplies to 0.82V
J5	Connects VDD LV PLL supplies to 0.82V
J7	Connects VDD LV MIPI supplies to 0.82V
J8	Connects VDD HV PLL AUR supplies to 1.8V
J9	Connects VDD HV MIPI supplies to 1.8V
J10	Connects VDD HV LFASTPLL supplies to 1.8V
J11	Connects VDD HV FIRC supplies to 1.8V
J12	Connects VDD HV EFUSE supplies to 1.8V
J13	Connects VDD HV TMU supplies to 1.8V
J14	Connects VDD HV VREF supplies to 1.8V
J15	Connects VDD HV PLL supplies to 1.8V
J16	Connects VDD HV IO AUR supplies to 1.8V
J17	Connects VDD HV IO QSPI supplies to 1.8V
J18	Connects VDD HV IO MTI supplies to 1.8V
J20	Connects VDD HV IO LFAST supplies to 1.8V
J21	Connects VDD HV IO supplies to 3.3V
J22	Connects VDD HV FXOSC supplies to 1.8V
J23	Connects VREFH ADC supplies to 1.8V
J25	Connects VDD HV ADC supplies to 1.8V
J64	Connects VDD HV IO ENET supplies to 1.8V or 3.3V

3.1.3 FS8510 PMIC Debug Mode

As part of the safety features of the FS8510 PMIC there is an internal watchdog timer which must be refreshed within 256ms after supply power on. If this watchdog is not serviced then the FS8510 will assert the MCU RESET_B signal several times before then attempting to power cycle the MCU.

It is therfore recommended to put the FS8510 device into debug mode after power on by disabling (default) jumper J2. In debug mode, no watchdog refresh is required which allows application development without the need for watchdog servicing via the MCU.

3.1.4 Power Switch, Status LEDs and Fuse

The main power switch (switch SW1) can be used to isolate the power supply input from the EVB voltage regulators if required.

- Push S1 indicator “-” will turn the EVB on
- Push S1 indicator “O” will turn the EVB off

When power is applied to the EVB, six blue power LEDs adjacent to the FS8510 PMIC show the presence of the supply voltages as follows:

- LED D6 – Indicates that the 0.82V is enabled and working correctly
- LED D7 – Indicates that the 1.8V is enabled and working correctly
- LED D8 – Indicates that the 1.2V is enabled and working correctly
- LED D9 – Indicates that the 3.3V is enabled and working correctly
- LED D10 – Indicates that the 5.0V is enabled and working correctly
- LED D11 – Indicates that the 4.1V is enabled and working correctly

If no LED is illuminated when power is applied to the EVB and the FS8510 is correctly enabled, it is possible that either power switch S1 is in the “OFF” position or that the fuse F1 has blown. The fuse will blow if power is applied to the EVB in reverse-bias, where a protection diode ensures that the main fuse blows rather than causing damage to the EVB circuitry. If the fuse has blown, check the bias of your power supply connection then replace fuse F1 with a SMT 5A fast blow fuse.

If the LED’s illuminate and then extinguish periodically then it is likely that the FS8510 has not entered debug mode. Please power off the board and wait at least 1 second before powering back on to recover from this.

3.2 Reset Circuit

S32R294 POR_B reset is connected to FS8510 PGOOD signal as well as a reset switch SW1 via jumper J3. An orange LED D5 is illuminated after 0.82V, 1.8V, 3.3V working correctly, and the PGOOD signal is forced high simultaneously by the FS8510 PMIC.

S32R294 RESET_B reset is connected to FS8510 RST signal. Bi-direction connection is chosen by connecting J56 pin 1->2, and single-direction only from FS8510 RST to S32R294 RESET_B is chosen by connecting J56 2->3 (default). A red LED D12 is used to indicated RESET_B reset situations.

The EVB reset circuit provides the following functionality:

The reset switch SW1 can be used to reset the MCU and PMIC. FS8510 RST will be released after PGOOD going high and may assert if errors happen in FS8510 according to the configured settings. Normally, RESET_B is controlled by S32R294 and is kept high after MCU leaving the reset state. POR_B is also connected to the QSPI Flash IC (U21) reset pin. RESET_B is also connected to reset signal of several peripherals and selection signal of the analog switch IC MAX4886 via a Schmitt trigger buffer.

Table 3. Reset circuit jumper settings

Jumper	Description
J3	Connect reset switch circuit and FS8510 PGOOD pin to POR_B pin

Jumper	Description
J56 1->2	Enable bi-direction connection between FS8510 RST pin and RESET_B pin
J56 2->3	Enable single direction connection between FS8510 RST pin and RESET_B pin

3.3 MCU External Clock Circuit

In addition to the internal 48 MHz oscillator, the MCU can be clocked by different external sources. The EVB system supports two possible MCU clock sources:

1. 40MHz crystal Y1 (The MCU only has a 40MHz input)
2. External differential or single ended clock input to the EVB via MIPI-CSI0 connector J36, driving MCU EXTAL and XTAL with negative and positive clock signals respectively

The clock circuitry is shown in Figure 4. Each source is selectable via the 0-ohm links as shown, with crystal Y1 being the default factory option.

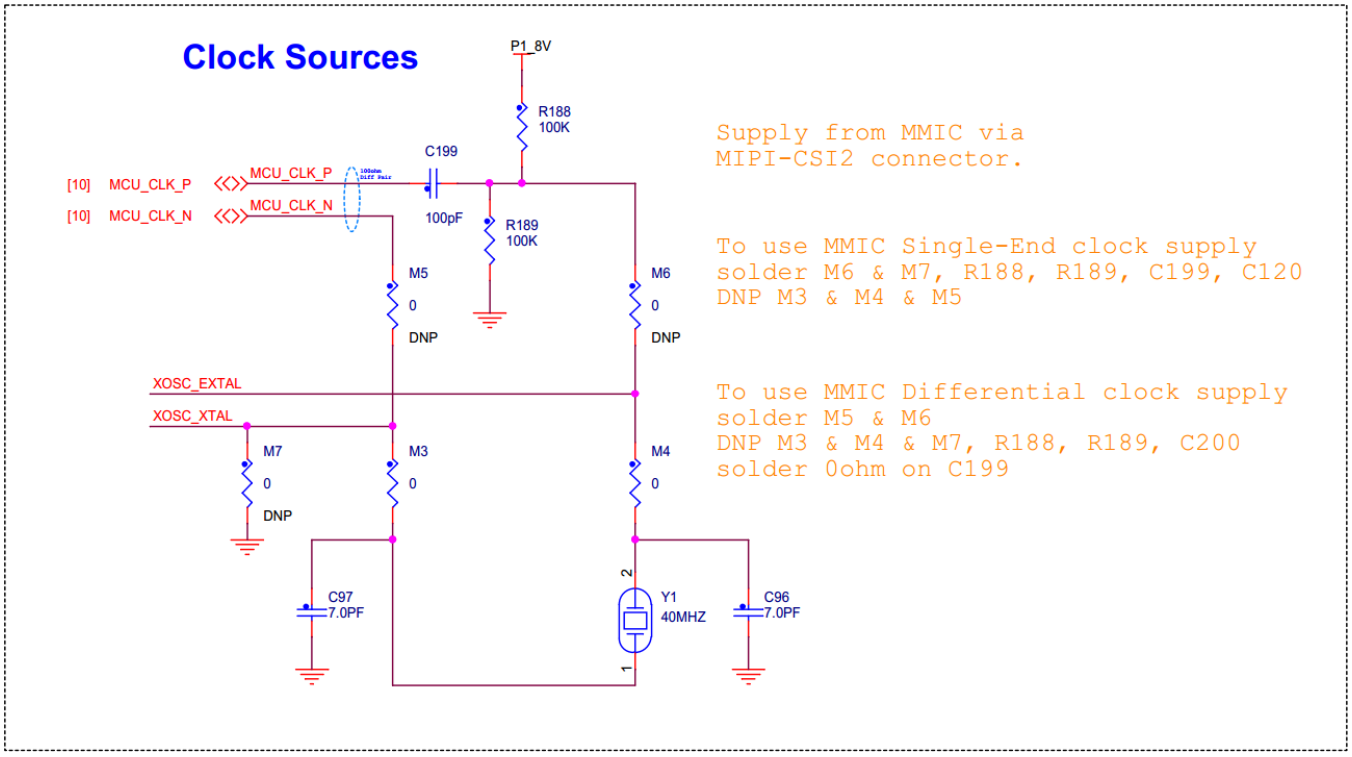

Figure 4. 40MHz crystal circuit

The main use-case for the EVB when using an external clock would be having the TEF810X RF front end BEST3 board via the S32R-TEF810-ADPT adaptor board connected to J36. In this configuration a single ended clock can be routed to the MCU by placing a zero-ohm link (or bridging the solder pads) of M5, M6 and M7, and remove M3 and M4. This gives the desired effective configuration shown in Figure 5 below.

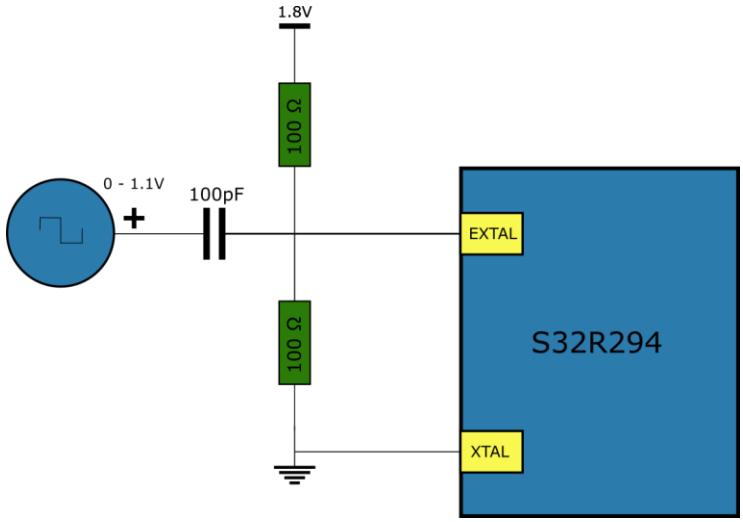

Figure 5. Effective single ended configuration

3.4 JTAG

The EVB is fitted with 14-pin JTAG debug connector. The following diagram shows the 14-pin JTAG connector pinout (0.1” keyed header).

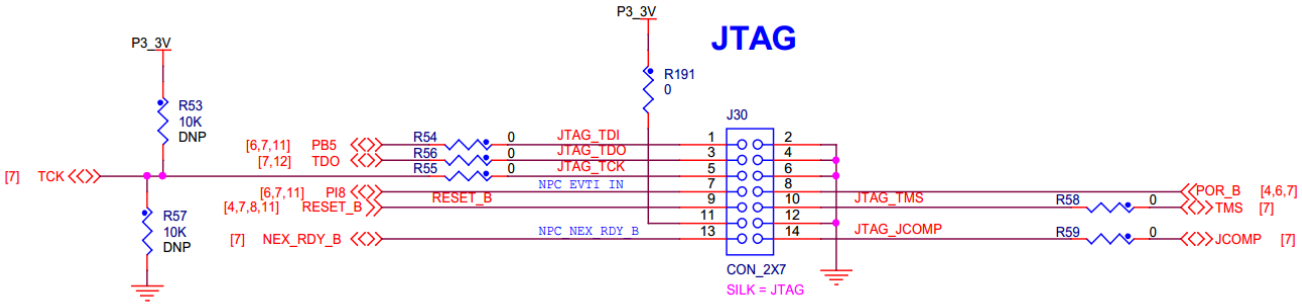

Figure 6. JTAG connector pinout

3.5 Nexus Aurora

Table 4 shows the pinout of the 34-pin Samtec connector for the S32R294 Aurora interface.

Table 4. Aurora Trace connector pinout

Pin No	Function		Pin No	Function
1	TX0+		2	VREF
3	TX0-		4	TCK/TCKC/DRCLK
5	VSS		6	TMS/TMSC/TxDataP
7	TX1+		8	TDI/TxDataN
9	TX1-		10	TDO/RxDataP
11	VSS		12	JCOMP/RxDataN
13	TX2+		14	EVTI1
15	TX2-		16	EVTI0
17	VSS		18	EVTO0
19	TX3+		20	VREG_POR_B
21	TX3-		22	RESET_B
23	VSS		24	VSS
25	TX4+[1]		26	CLK+
27	TX4+[1]		28	CLK-
29	VSS		30	VSS
31	TX5+[1]		32	EVTO1/RDY
33	TX5+[1]		34	N/C
GND	VSS		GND	VSS

1. Lane not used on the S32R294 device.

3.6 Serial Interprocessor Interface (SIPI)

A dedicated SIPI interface connector is provided on the EVB.

A 10pin Samtec connector (J17: ERF8-005-05.0-LDV-L-TR) is used for the SIPI interface. The pin-out of the connector is shown in Figure 7.

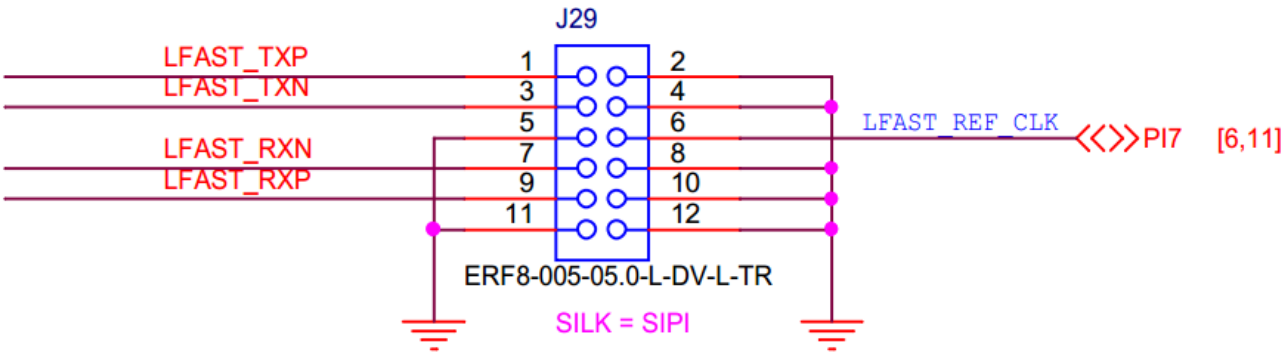

Figure 7. SIPI connector pinout

3.7 Camera Serial Interface (MIPI-CSI2)

Two dedicated MIPI-CSI2 interfaces are provided on the EVB, and are designed to provide compatibility with the TEF810X BEST3 Radar front end EVK.

Two 60 pin Samtec connectors (QTH-030-01-L-D-A-K-TR) are used for MIPI-CSI2 interfaces. The pinout is shown in Figure 8.

To use the TEF810X BEST3 Radar front end EVK an intermediate adaptor board (S32R-TEF810-ADPT) is required. Contact your local NXP representative for details on how to order this board.

For single MIPI-CSI2 front end usage connector J37 must be used since the MIPI-CSI1 instance on the S32R294 device contains the PLL. See the S32R294 device RM for more details.

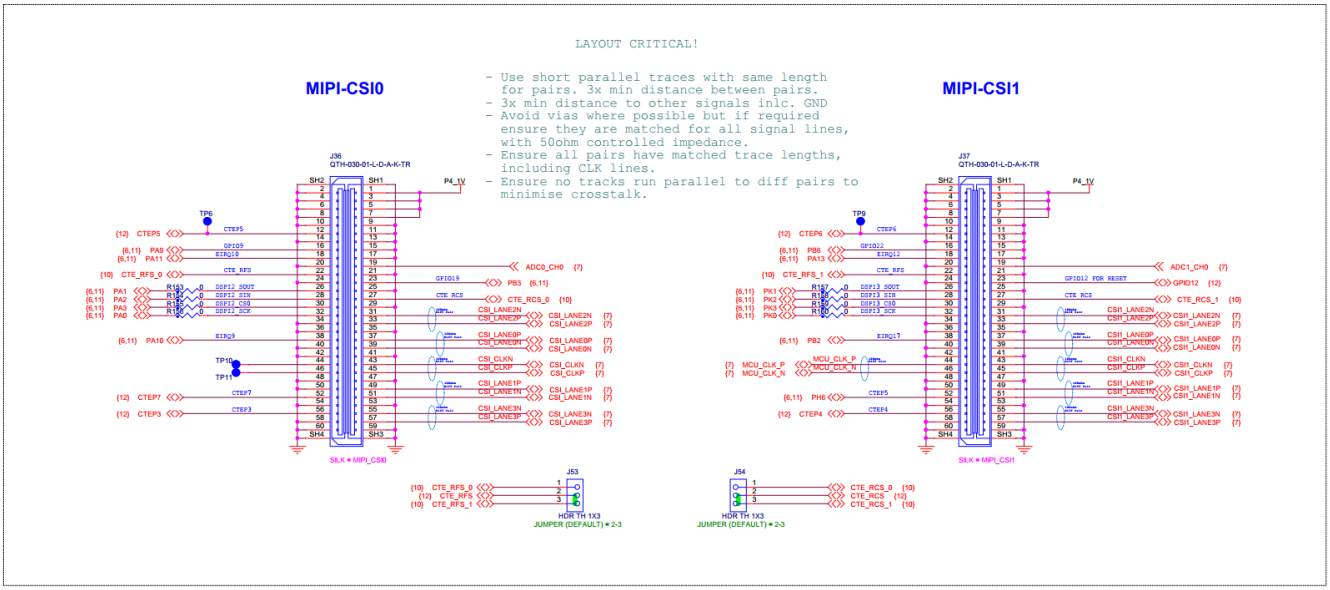

Figure 8. MIPI-CSI2 connector pinout

3.8 Gigabit Ethernet

The EVB provides support for Gb ethernet, utilising the RGMII interface present on the S32R294 device. The EVB is designed with a Micrel KSZ9031RNXUA Ethernet physical interface (U7), and associated RJ45 connector (J32- Bel Fuse V890-1AX1-A1). This is the default configuration of the RGMII signals from the S32R294 device. If for any reason the alternate functions multiplexed on the RGMII pads are required then these signals can be routed to headers by adding a 0-ohm link to the pads provided. These are not soldered by default to reduce the signal trace length and parasitics, Gb ethernet operation cannot be gauranteed if these links are in place since it adds significant length to the signal path.

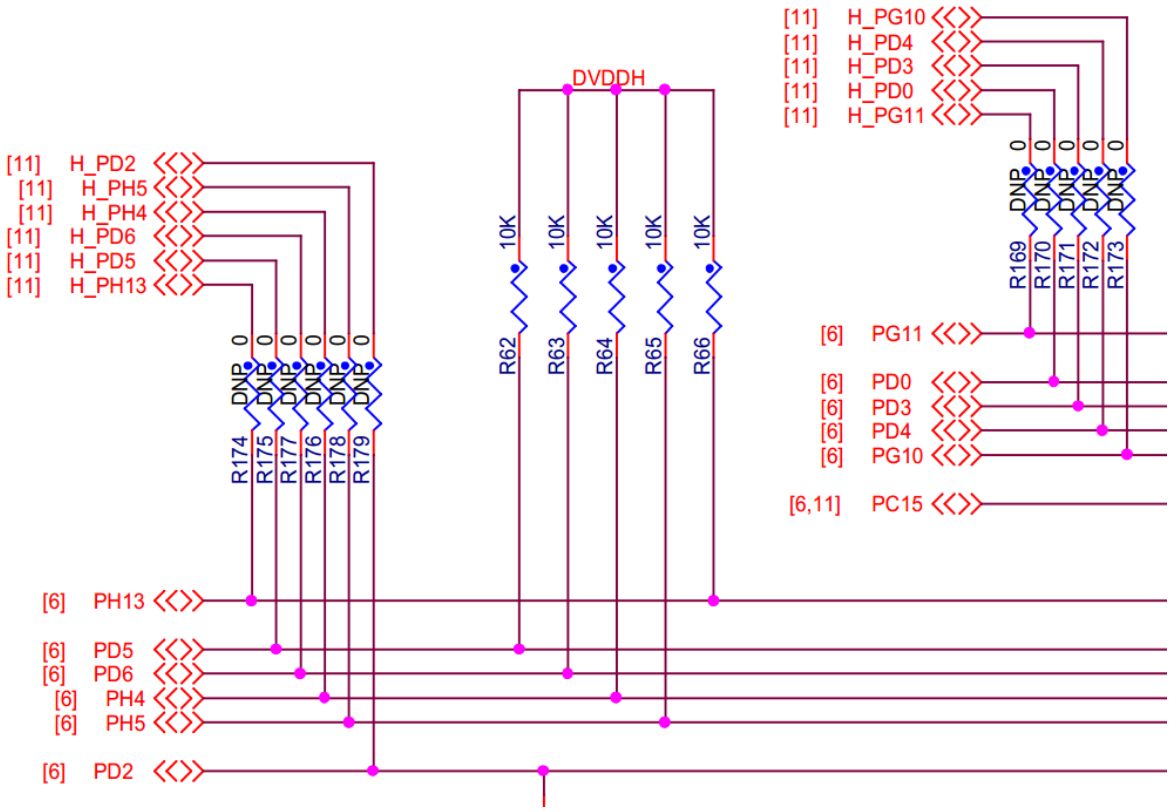

Figure 9. RGMII Signal Connections to headers

The S32R294 device supports both 3.3V and 1.8V supply and I/O levels for the ethernet interface, therefore the EVB includes support for both of these options. This can be selected by changing the connection of J64, as shown in the table below.

Table 5. Ethernet voltage selection

Jumper	Ethernet Supply Level
J64 1-2	1.8V
J64 2-3	3.3V (Default)

3.9 UART-USB

The EVB supports one UART-USB interface with a USB to serial UART Converter IC FT232RQ (U11).
Since the LIN module pads have multiplexable functions, LIN RXD signal and LIN TXD signal are routed to both IC FT232RQ U11 via J39, and to the headers on the EVB.

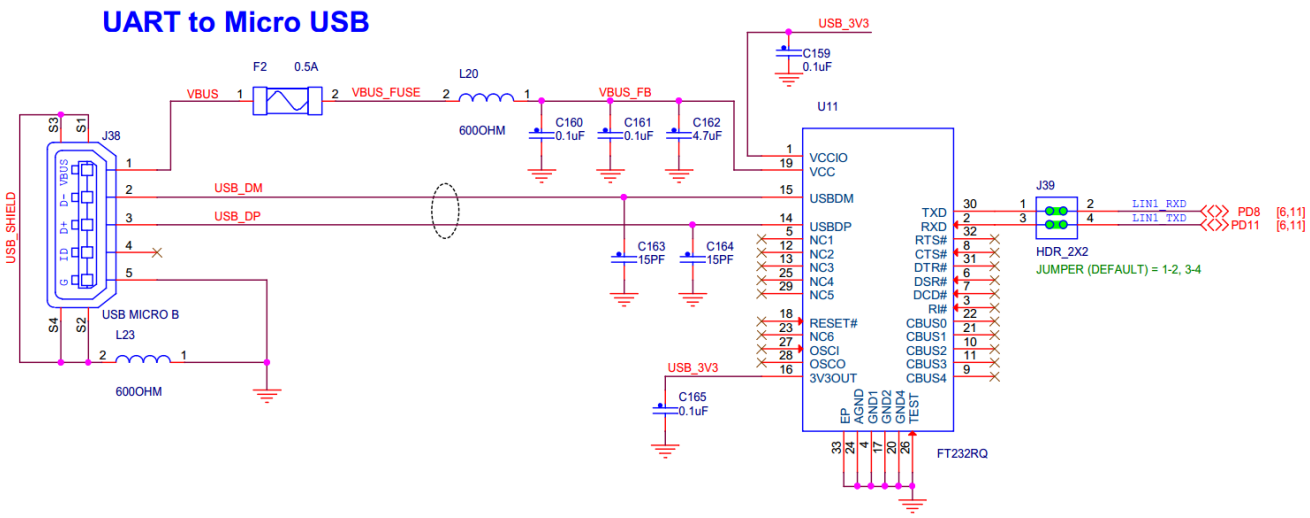

Figure 10. UART to USB interface

3.10 FlexRAY

The EVB supports one FlexRay interface with an NXP TJA1080TS/N FlexRay transceiver (U8). For flexibility, the FlexRAY transceiver is connected to a FlexRAY connector P1.

By default the FlexRAY interface is not enabled. To enable the FlexRAY interface the jumpers detailed in Table 6 need to be placed.

Table 6. FlexRAY control jumpers

Jumper	Label	Description
J33 1-2	FLEXRAY_TXD	TX to MCU
J33 3-4	FLEXRAY_TXD_EN	TXEN to MCU
J33 5-6	FLEXRAY_RXD	RX to MCU

3.11 CAN FD

The EVB supports 3x CAN-FD interfaces, CAN0 and CAN1 support up to 5Mbps communication speed utilizing NXP TJA1051T /3 CAN FD (Flexible Data) compliant physical interfaces, CAN2 can support up to 8Mbps communication speed utilizing MICROCHIP MCP2542FD CAN FD (Flexible Data) compliant physical interfaces.

Since the CAN module pads have multiplexable functions, CAN0/1/2 signals are routed to both on-board CAN-FD phy U9/U10/U20 via J46-J51, and to the headers on board.

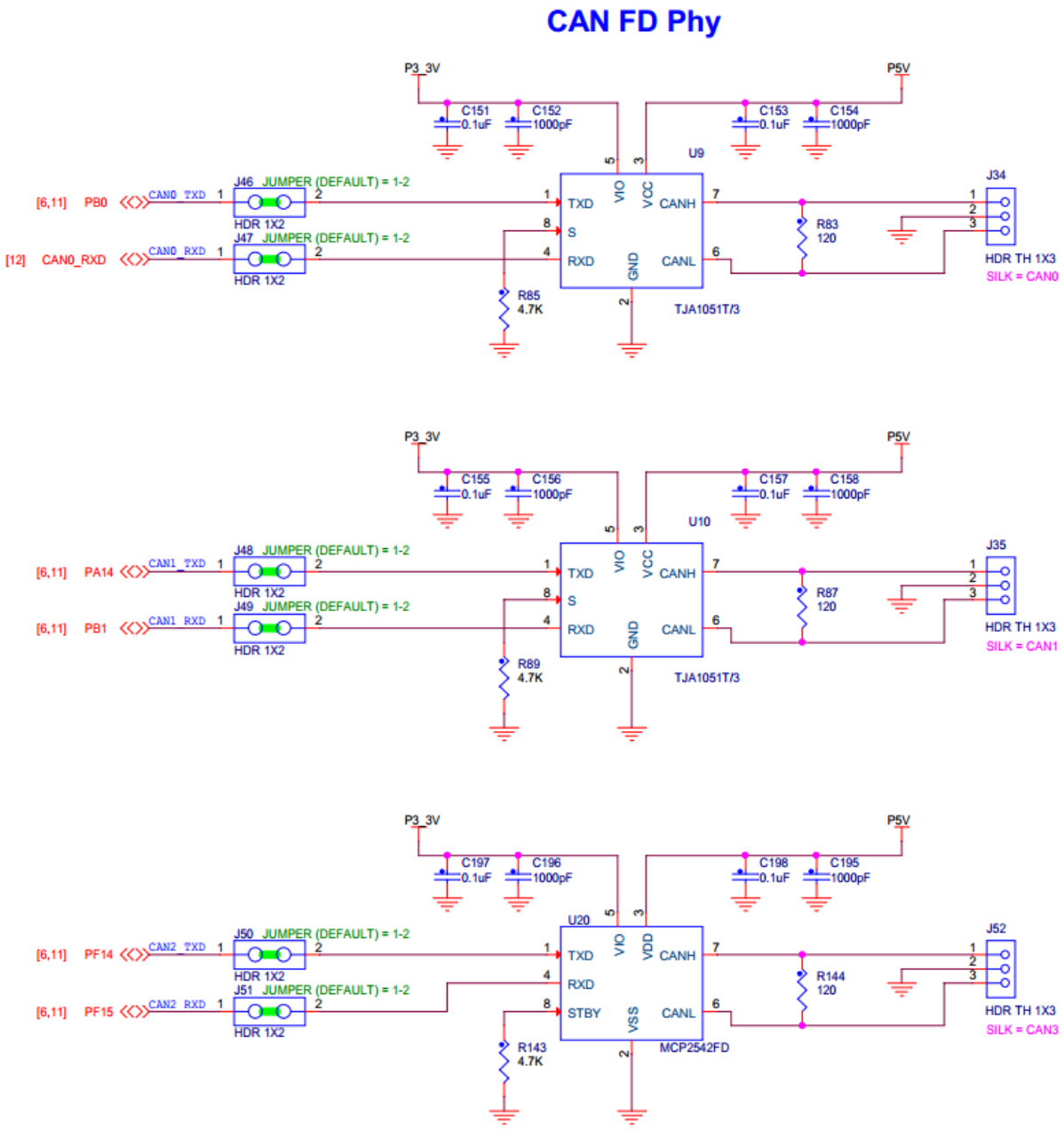

Figure 11. CAN FD Physical Interfaces

3.12 FLASH

An external 256Mbits Serial NOR Flash memory (MX25U25645G, U21) is connected to S32R294 via the QSPI interface. Since there is no internal Flash inside of the MCU, code can be stored in the external flash, then loaded into SRAM in MCU after power-on over QSPI interface. This is the default configuration of the QSPI signals from the S32R294 device. If for any reason the alternate functions multiplexed on the QSPI pads are required then these signals can be routed to headers by adding a 0-ohm link to the pads provided. These are not

soldered by default to reduce the signal trace length and parasitics, QSPI operation cannot be gauranteed if these links are in place since it adds significant length to the signal path.

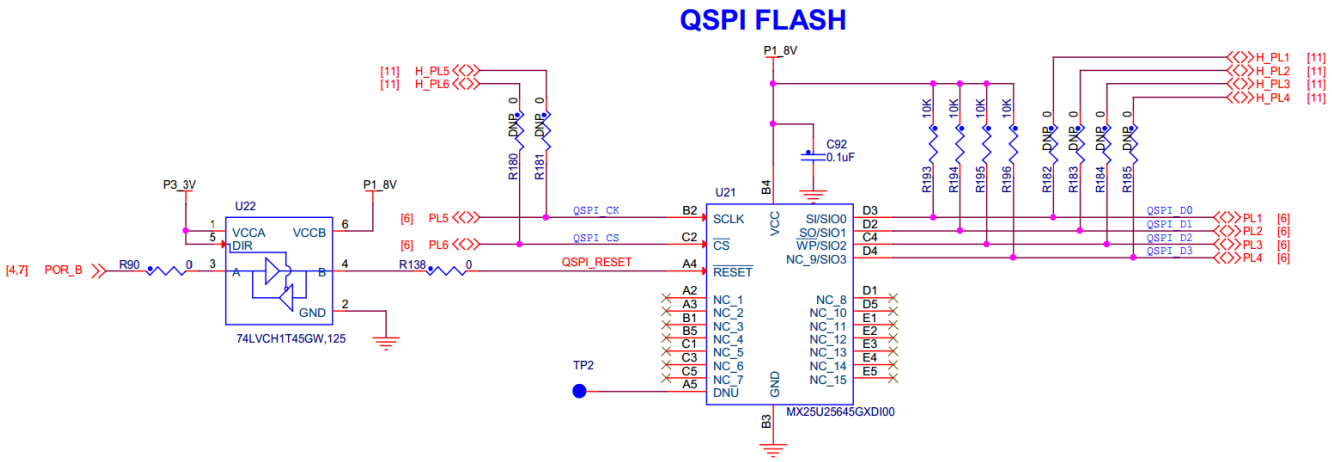

Figure 12. QSPI Flash circuit

3.13 EEPROM

An external 64Kb EEPROM (AT24C64D, U6) is connected to S32R294 via I2C interface. The I2C read address is 0xA0 and write address is 0xA1. By default the I2C interface is not enabled, which can be enabled by jumpers J67 & J68.

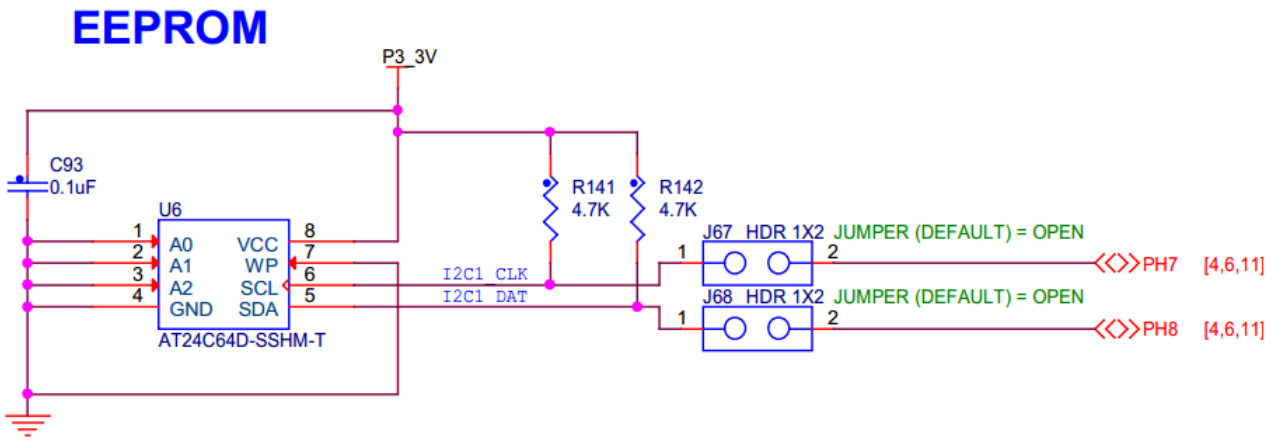

Figure 13. EEPROM circuit

3.14 BOOT Configuration

The S32R294 device can support booting from different sources by applying a logic 1 or 0 to the BOOTMODE pins of the device, which in turn latches the input level on the RCON GPIO pins of the device at reset release. The EVB supports this by providing 2 switch banks (SW4 and SW5) that can be configured to the application need, and using high speed switches these are held on the device boot pins until reset is released.

The mapping of these switches is shown in the table below. For information on the supported boot configurations of the S32R294 device please consult the device reference manual.

Table 7. Boot configuration switches

Switch Bank	Switch	RRU2 Boot Pad	Usual GPIO function after RESET_B released
SW4	1	BOOTMODE0	CTEP4
	2	BOOTMODE1	None
	3	RCON0	FS85_FS0B
	4	RCON1	DSPI1_SIN
	5	RCON2	None
	6	RCON3	CAN0_RXD
	7	RCON4	PB4 (only if J6 = 1-2)
	8	RCON5	CTEP3
SW5	1	RCON6	None
	2	RCON7	CTE_RFS
	3	RCON8	CTE_RCS
	4	RCON9	None
	5	RCON10	CTEP6
	6	RCON11	CTEP7
	7	RCON12	CTEP5
	8	RCON13	None

3.15 Test Points

EVB test points are listed and detailed in Table 8.

Table 8. Test points

Signal	TP name	Shape	Description
P12V	TP1	Surface Pad	12V supply
DNU/ECS	TP2	Surface Pad	Do Not Use/ For auto part, ECS pin from Flash.
GND	TP3	Test Loop	Ground
GND	TP4	Test Loop	Ground
P4_1V	TP5	Surface Pad	4.1V FS8510 VPRE output
CTEP5	TP6	Surface Pad	MIPI-CSI2_0 test signal
ENET_REF_CLK	TP7	Surface Pad	125MHz ENET Reference clock
GND	TP8	Test Loop	Ground
CTEP6	TP9	Surface Pad	MIPI-CSI2_1 test signal
TP10	TP10	Surface Pad	MIPI-CSI2_0 external clock output P
TP11	TP11	Surface Pad	MIPI-CSI2_0 external clock output N
GND	TP12	Test Loop	Ground
P5V	TP13	Surface Pad	5V FS8510 Boost output
AUR_NEXUS_EVTI	TP14	Surface Pad	Nexus Aurora test signal
AUR_NEXUS_EVT0	TP15	Surface Pad	Nexus Aurora test signal
P0_82V	TP16	Surface Pad	0.82V FS8510 Buck1 output
P3_3V	TP17	Surface Pad	3.3V FS8510 LDO2 output
P1_2V	TP18	Surface Pad	1.2V FS8510 LDO1 output
FRD_INH2	TPV1	Through hole Pad	FlexRAY PHY test signal
FRD_INH1	TPV2	Through hole Pad	FlexRAY PHY test signal
FRD_ERRN	TPV3	Through hole Pad	FlexRAY PHY test signal
FRD_RXEN	TPV4	Through hole Pad	FlexRAY PHY test signal

4 Default Jumper Summary Table

On delivery the EVB comes with a default jumper configuration. Table 9 lists and describes briefly the jumpers and indicates which jumpers are on/off on delivery of the board.

Table 9. Default Jumper Table

Jumper	Default Pos	PCB Legend	Description
J2	Off	-	FS8510 Debug mode select
J3	On	-	POR_B to PGOOD and switch
J4	On	-	Connect VDD core power
J5	On	-	Connect VDD_LV_PLL power
J6	2-3		Connect TDO to PB4
J7	On	-	Connect VDD_LV_MIPI power
J8	On	-	Connect VDD_HV_PLL_AUR power
J9	On	-	Connect VDD_HV_MIPI power
J10	On	-	Connect VDD_HV_LFASTPLL power
J11	On	-	Connect VDD_HV_FIRC power
J12	On	-	Connect VDD_HV_EFUSE power
J13	On	-	Connect VDD_HV_TMU power
J14	On	-	Connect VDD_HV_VREF power
J15	On	-	Connect VDD_HV_PLL power
J16	On	-	Connect VDD_HV_IO_AUR power
J17	On	-	Connect VDD_HV_IO_QSPI power
J18	On	-	Connect VDD_HV_IO_MTI power
J20	On	-	Connect VDD_HV_IO_LFAST power
J21	On	-	Connect VDD_HV_IO power
J22	On	-	Connect VDD_HV_FXOSC power
J23	On	-	Connect VREFH_ADC power
J25	On	-	Connect VDD_HV_ADC power
J33	Off	-	FlexRAY 1-2: PI6 to PHY U8 TXD 3-4: PI5 to PHY U8 TXED 5-6: PD1 to PHY U8 RXD
J39	On	-	LIN/UART 1-2: PD8 to U11 TXD 3-4: PD11 to U11 RXD
J46	On	-	CAN0 PB0 to PHY U9 TXD
J47	On	-	CAN0 CAN0_RXD to PHY U9 RXD

Jumper	Default Pos	PCB Legend	Description
J48	On	-	CAN1 PA14 to PHY U10 TXD
J49	On	-	CAN1 PB1 to PHY U10 RXD
J50	On	-	CAN2 PF14 to PHY U20 TXD
J51	On	-	CAN2 PF15 to PHY U20 RXD
J53	1-2	-	CTE_RFS signal select
J54	1-2	-	CTE_RCS signal select
J56	2-3	-	Enable/disable RESET_B and FS8510 RST bi-direction connection
J64	1-2	-	VDD_HV_IO_ENET supply select: 3.3V or 1.8V
J65	2-3	-	Enable/disable Test mode
J66	2-3	-	FS8510 VCOREMON select: BUCK1 output or S32R294 PMIC_SENSE pin
J67	Off	-	EEPROM I2C PH7 to U6 SCL
J68	Off	-	EEPROM I2C PH8 to U6 SDA

5 Known Issues

None

6 Revision History

Version	Comment
Rev A	Initial version
Rev B	Update FS85 (U1) automatic debug mode entry; Add J6 for RCON/TDO select; Re-order SW4, SW5 for RCON in order; Change J37 pin 23 connected to GPIO12 (PA12); Change R135/R136 to J24, J26; Add GND test point TP8, TP12;

	Change J56 to 3-pin jumper; Swap connection between MCU_CLK_P/N and TP10/11

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