UM10525

120 V 20 W CFL demo board using the UBA2212

Rev. 1 — 19 April 2012 **User manual**

Document information

Info	Content
Keywords	UBA2212, demo board, CFL, boost, 120 V (AC), 20 W
Abstract	This document is a user manual for the UBA2212 120 V, 20 W demo board

Revision history

Rev	Date	Description
v.1	20120419	first issue

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

1. Introduction

The UBA2212 series is a family of high voltage monolithic integrated circuits for driving Compact Fluorescent Lamps (CFL) in half-bridge configurations. It is derived from the UBA2211 IC and modified to drive a 120 V (AC) application. The UBA2212 contains a boost feature, which boosts the lamp current for a certain time after ignition. This feature results in faster CFL warm-up and more light after ignition.

Run-up time is one of the key requirements for CFL. Normally, it is measured from the time lamp was powered until 80 % of light output is reached. Run-up time is long if a high temperature amalgam burner is used or a lamp is ignited in cold environment. The UBA2212 is designed to meet the needs of these situations in both indoor and outdoor applications.

In addition to the boost feature, the UBA2212 has the following features:

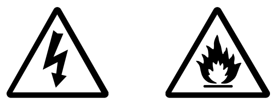
- Fixed frequency preheat with an adjustable preheat time
- RMS current control
- Saturation Current Protection (SCP)
- OverTemperature Protection (OTP)
- Capacitive Mode Protection (CMP)

This user manual is intended to describe a 120 V, 20 W application demo board using the UBA2212CT. See the *UBA2212 data sheet* for the functional description of this IC.

2. Safety Warning

WARNING

Lethal voltage and fire ignition hazard



The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire.

This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. This product shall never be operated unattended.

The demo board is powered by AC mains voltage. Avoid touching the board when power is applied. An isolated housing is obligatory when used in uncontrolled, non-laboratory environments. Always provide galvanic isolation of the mains phase using a variable transformer. The following symbols identify isolated and non-isolated devices.

a. Isolated

b. Non-isolated

Fig 1. Isolated and non-isolated symbols

3. Specifications

Table 1. Demo board specification

Parameter	State	Value	Comment
AC line input voltage	-	96 V (AC) to 144 V (AC)	board optimized for 120 V (AC), 60 Hz.
Lamp voltage (V_{lamp})	steady	100 V	measured at 120 V (AC) mains; GE T3 Spiral 20 W burner used; Table 2 on page 10
Lamp current (I_{lamp})		170 mA	
Operating frequency (f_{osc})		45 kHz	
Power Factor		>0.58	
Preheat current (I_{ph})	preheat	150 mA	constant preheat current at 96 V (AC) to 144 V (AC); Table 2 on page 10
Preheat time (t_{ph})		0.8 s	
Lamp current (I_{lamp})	boost	255 mA	measured at 120 V (AC) mains; see Figure 5 on page 8 and Table 2 on page 10
boost time (t_{bst})		40 s	
transition time from boost to burn ($t_{t(bst-burn)}$)		2 s	

Fig 2. Photographs of a 20 W CFL Application with a UBA2212

4. Schematic and functional description

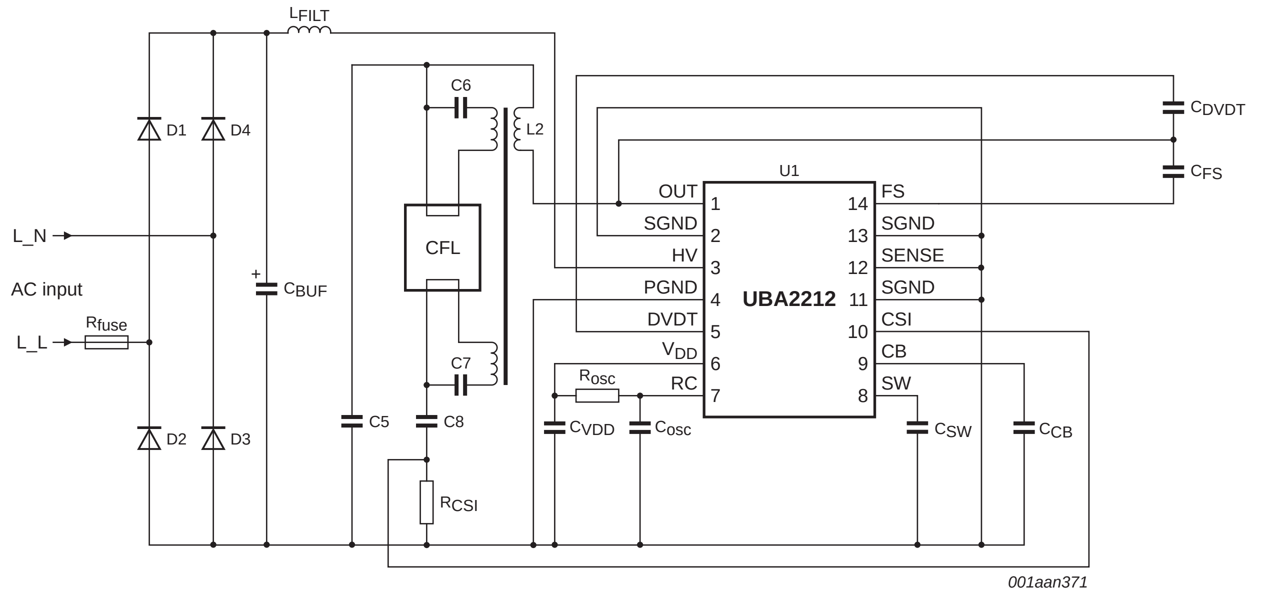


Fig 3. Typical UBA2212 Circuit for compact fluorescent lamp application

4.1 Functional description

The bridge rectifier (D1 to D4) rectifies the AC input power. The bulk storage capacitor C_{BUF} filters the rectified DC voltage. Power inductor L_{FILT} and capacitor C_{BUF} form an LC filter, which attenuates conducted differential mode EMI noise. Fusible resistor R_{fuse} provides protection against overcurrent failure.

During start-up, the internal current source connected to HV pin provides power. Once capacitor C_{DVDT} is charged, it provides the dV/dt supply for normal operation. Capacitor C_{FS} provides the high-side floating supply output and Capacitor C_{VDD} is used for VDD bypass.

C5 and inductor L2 primary winding (N1) form an LC tank translating power into the burner. The L2 secondary windings N2 and N3 preheat the burner filaments. If preheat is not required in the application, leave off secondary windings and short the filaments. C8 is DC blocking capacitor. R_{CSI} is used for burner current sensing during boost and RMS states.

R_{osc} and C_{osc} determine the nominal oscillating frequency based on the Built-in 555-timer function. The input to the SW pin generates the V_{SW} signal which determines the preheat time. Capacitor C_{CB} sets the boost time.

4.2 Timing

The UBA2212 based 20 W demo board provides all the functions needed for correct CFL operation. These functions include preheat, ignition, boost and on-state operation.

Several protection features safeguard the correct operation of the CFL and controller IC. The typical system timing is shown in Figure 4.

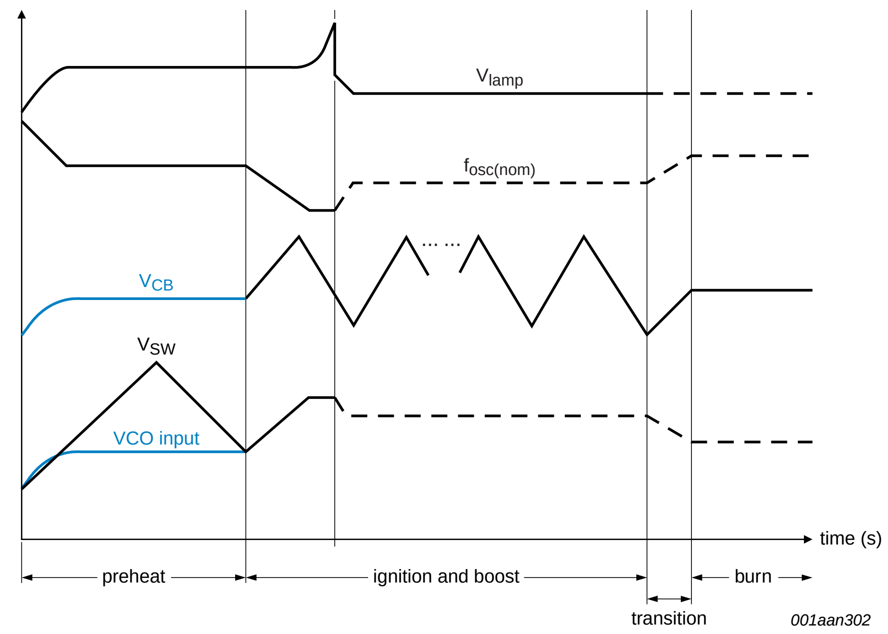


Fig 4. Timing sequence of the system

In preheat, current I_{SW} charges capacitor C_{SW} generate the preheat timing (t_{ph}).

Capacitor C_{CB} connected to pin CB is connected to the boost timer input to control the boost time. After preheat, the C_{CB} voltage sweeps up and down at the boost timing (t_{bst}). The boost ends after 25 C_{CB} sweeping cycles.

The transition from the boost state to the burn state is triggered when the boost timer indicates the end of the boost state. During the boost to burn transition, the boost transition timer is active. The timer defines transition time which is also realized using capacitor C_{CB} on CB pin.

When the RMS current control circuit leaves the system operating at the normal lamp current, it enters the burn state. In this state, a feedback loop controls the V_{SW} voltage on pin SW. This feature makes the lamp current independent mains or lamp voltage variations.

5. Measurement results

Using a typical 20 W lamp, the measurements show that the boost effect is visible to the human eye when the light is powered up. The same situation is not visible when the same lamp is used without boost feature.

Figure 4 shows the states after power-on. The preheat, ignition, boost, transition and burn states are clearly visible. The preheat and transition states are also zoomed in greater detail.

(1) I_{lamp} signal.

(2) SW signal timing for preheat.

(3) CB signal timing for boost and transition.

(4) Half-bridge voltage.

Fig 5. Time sequence for a boost state lamp

(1) I_{lamp} signal.

(2) SW signal timing for preheat.

(3) CB signal timing for boost and transition.

(4) Half-bridge voltage.

Fig 6. Time sequence for a boost lamp with a zoom function applied to the preheat state

(1) I_{lamp} signal.

(2) SW signal timing for preheat.

(3) CB signal timing for boost and transition

(4) Half-bridge voltage.

Fig 7. Time sequence for a boost lamp with a zoom function applied to the preheat to RMS transition

Table 2. Electrical parameters 12 W boost lamp (UBA2212BT N1B)

Boost ratio = 1.49; boost time = 38.5 s (25 cycles); transition time = 2 s.

State	V_{IN} (V)	P_{in} (W)	PF	V_{lamp} (V)	I_{lamp} (mA)	I_{hb} (mA)	P_{lamp} (W)	f_{osc} (kHz)	T_{ph} (s)	I_{ph} (mA)
Normal	120	21.3	0.589	107	169	366	18.1	44.3	0.76	150
Boost	-	23.1	-	80.5	252	470	20.3	39.7	-	-

The boost feature provides a fast run-up time. However when a hot lamp is powered, the lamp does not need boost or only a short boost time. The UBA2212 sets a boost overtemperature ($T_{j(end)bst}$) to allow for the reduced boost time. The IC detects its die temperature and ends the boost state when the temperature trigger point is reached. The lamp then enters the burn transition.

When a lamp burns for a long time, is switched off and then after a short delay switched on again. The end of boost is reached after only 6 s of boost. In Figure 5, SW counted only 5 cycles. Normally SW sweeps through 25 cycles when OTP is not triggered.

(1) I_{lamp} signal.

(2) SW signal timing for preheat.

(3) Half-bridge voltage.

(4) CB signal timing for boost and transition.

Fig 8. Boost with OTP triggered

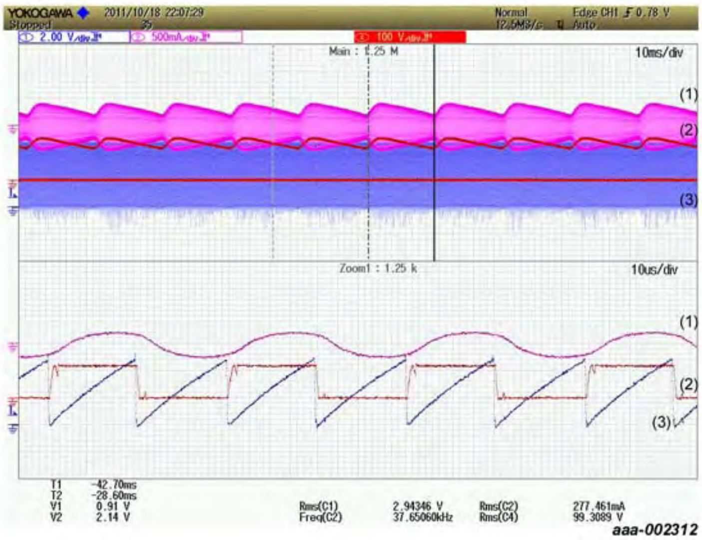
5.1 Boost lamp with high lamp voltage

During boost state, lamps consume more power. As a result, the half-bridge valley voltage value is pulled low. In addition, CM or hard switching occurs especially when a high lamp voltage with used with a low mains input.

The UBA2212 detects switched operation prevent stress on MOSFETs using the internal active Zero-Voltage Switching (ZVS) control circuit.

When capacitive mode is detected, the internal current source discharges the internal capacitor. Consequently, the SW voltage is lower and the RMS circuit controlled boost frequency increases until the system is at the zero-voltage switching border.

Figure 6 shows the Capacitive Mode (CM) protection response in the boost state.



(1) I_{lamp} signal.

(2) RC signal.

(3) Half-bridge signal.

Fig 9. CMP activated in boost state

The ratio of boost lamp current to RMS lamp current (I_{bst} : I_{RMS}) is lower because of CMP.

If a significant boost effect is needed, the system parameters need adjusted. A bigger lamp capacitor, for example, reduces the need for CM and LC tank to be adjusted to supply a larger power gain. However, the larger power gain is at the cost of a higher half-bridge current which leads to low-power efficiency and a narrow RMS operation range.

5.2 RMS control in boost and steady states

When ignition frequency is reached, the lamp ignites. V_{SW} increases to a given voltage to set the lamp current at the level defined by the internal boost reference and resistor R_{CSI}.

The calculation is shown in Equation 1:

$$Boost\ I_{lamp} = \frac{V_{ref(bst)}}{R_{CSI}} \quad (1)$$

When the RMS current control circuit leaves the system operating at the normal lamp current, it enters the steady state. In this state, the voltage on pin CB is fixed and a feedback loop controls the voltage on pin SW. This feature enables the lamp current to be independent of the mains or lamp voltage. The lamp current calculation is shown in Equation 2:

$$Burn\ I_{lamp} = \frac{V_{ref(burn)}}{R_{CSI}} \quad (2)$$

Therefore, the boost-burn ratio can be found as shown in Equation 3:

$$Boost\ to\ burn\ ratio = \frac{V_{ref(bst)}}{V_{ref(burn)}} \quad (3)$$

5.3 Overtemperature protection

OTP is active in all states except boost. When the die temperature reaches the OTP activation threshold ($T_{th(act)otp}$), the oscillator is stopped and the power switches (LSPT/HSPT) are set to the start-up state. When the oscillator is stopped, the DVDT supply no longer generates the supply current I_{DVDT}. Voltage V_{DD} gradually decreases and the start-up state is entered. OTP is reset when the temperature < $T_{th(rel)otp}$.

During boost state, the threshold of temperature is $T_{j(end)bst}$ which is lower than $T_{th(otp)}$. When the die temperature has reached $T_{j(end)bst}$, the boost state ends, the IC enters steady state and OTP is enabled.

(1) VDD signal.

(2) I_{lamp} signal.

(3) Half-bridge voltage.

(4) CB signal timing for boost and transition.

Fig 10. OTP function activated in boost state

5.4 Saturation Current protection

A critical parameter in the design of the lamp inductor is its saturation current. When the momentary inductor exceeds its saturation current, the inductance drops significantly. This drop causes the inductor current and the current flowing through the LSPT and HSPT power switches to increase rapidly. The increase can cause the current to exceed the half-bridge power transistors maximum ratings.

Saturation of the lamp inductor is likely to occur in cost-effective and miniaturized CFLs. The UBA2212 family internally monitors the power transistor current. When the current exceeds the momentary rating of the internal half-bridge power transistors, the conduction time is reduced. In addition, the frequency increases slowly by discharging C_{SW}. This function causes the system to balance at the edge of the current rating of the power switches.

Figure 11 shows the Saturation Current Protection (SCP) in real application which uses an easily saturated inductor. SCP enables the burner to ignite despite the inductor saturating effect. When the same parameters are used with an IC without SCP, the IC failed during the ignition.

(1) Half-bridge voltage.

(2) I_{lamp} signal.

(3) RC signal.

Fig 11. IC operation with saturated inductor at ignition

5.5 Capacitive mode protection

The UBA2212 detects hard switching operations to prevent stress on MOSFETs using the internal Zero-Voltage Switching (ZVS) control circuit. In preheat stage, when CMP is detected, discharge of capacitor C_{CB} occurs by a current source which is a function of the hard switching level. The frequency increases very slowly until hard switching is no longer detected. Once CMP is no longer active, the system increases to the preheating frequency as defined preheat current.

In boost and burn state, V_{SW} determines the operating frequency. Under normal conditions, the RMS current control circuit is used. During CMP, the CMP circuit controls the frequency.

The CMP circuit controls capacitor C_{SW} when capacitive mode is detected. A current source (which is also dependent on the hard switching voltage level) discharges Capacitor C_{SW}. The operating frequency f_{osc}, increases until CMP is no longer detected. See Figure 12.

Fig 12. CMP in the burn state

6. Schematic and Bill Of Materials (BOM)

The components used are illustrated in Figure 3 and Figure 13.

Table 3 describes the components required for 120 V reference board application.

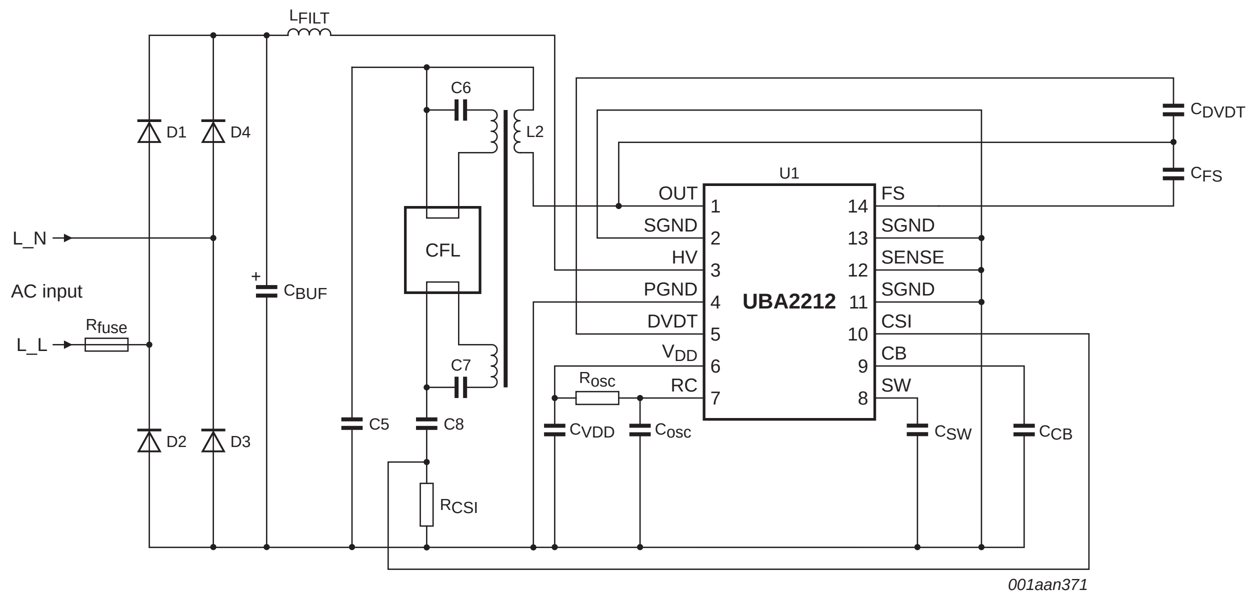


Fig 13. Application diagram

Table 3. Bill of materials

Number	Reference	Typical value	Quantity
1	R_{fuse}	10 Ω; 1 W - no value for fuse resistor	1
2	D1, D2, D3, D4	diode, 1 A; 1000 V; 1N4007	4
3	C_{BUF}	electrolytic capacitor; 33 μF; 250 V; 105 °C	1
4	L_{FILT}	inductor; 3 mH; 0.5 A	1
5	C_{DVDT}	ceramic capacitor; 330 pF; 500 V; 1206	1
6	C_{FS}	ceramic capacitor; 22 nF; 50 V; 0805	1
7	C_{CB}	ceramic capacitor; 220 nF; 50 V; 0805	1
8	C_{SW}	ceramic capacitor; 68 nF; 50 V; 0805	1
9	C_{osc}	ceramic capacitor; 220 pF; 50 V; 0805	1
10	C_{VDD}	ceramic capacitor; 100 nF; 50 V; 0805	1
11	R_{osc}	chip resistor; 100 kΩ; 5 %; 0805	1
12	C6; C7	film capacitor; 82 nF; 100 V	2
13	C5	film capacitor; 6.8 nF; 1 kV	1
14	C8	film capacitor; 8.2 nF; 400 V	1
15	R_{CSI}	chip resistor; 1.8 Ω; 1 %; 0.25 W	1

Table 3. Bill of materials *…continued*

Number	Reference	Typical value	Quantity
16	L2	PC40-EE16; 1.5 mH; 1 A; N = 180:6:6; diameter 0.23 mm	1
18	U1	UBA2212CT; SO14	1
19	Burner	burner; T3 Spiral 20 W	1

7. PCB layout

Figure 14 shows the layout of the PCB.

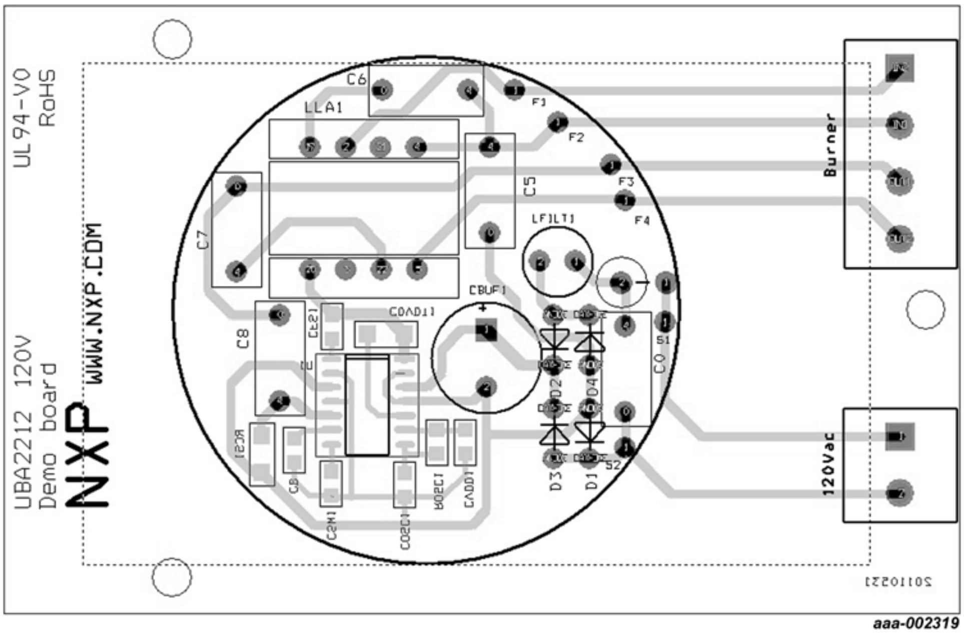


Fig 14. PCB layout

8. Alternative CFL examples

Some other lamps were measured in the lab, including 8 W, 12 W, 15 W, 20 W. Two boost lamps using UBA2212BT are listed Table 4 with their LC tank, start up-to-burn scope picture and related electrical parameters.

Table 4. Electrical parameters 12 W boost lamp (UBA2212BT N1B)
Boost ratio = 1.54.; C_{BUF} = 22 μF, 250 V; L2 = 1.7 mH, 2 Ω; C5 (res) = 6 nF, 1 kV; C6 and C7 = 100 nF, 100 V; C8 (DC) = 10 nF, 400 V; R_{CSI} = 2.2 Ω, 1 W

State	V_{IN} (V)	P_{in} (W)	PF	V_{lamp} (V)	I_{lamp} (mA)	I_{hb} (mA)	P_{lamp} (W)	f_{osc} (kHz)	t_{ph} (s)
Normal	120	11.3	0.59	75	127	248	9.5	48.3	0.8
Boost	-	16.1	-	67	196	338	13.1	40.34	-

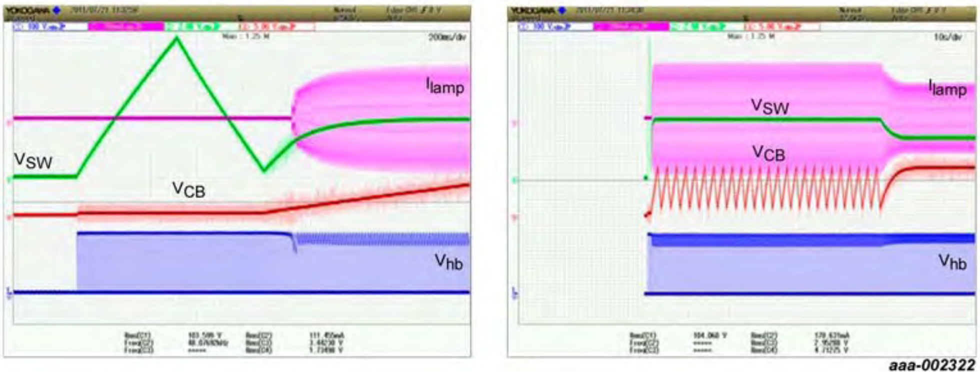


Fig 15. 12 W Baishi CFL

Table 5. Electrical parameters 12 W boost lamp (UBA2212BT N1B)

Boost ratio = 1.56.; C_{BUF} = 22 μF, 250 V; L2 = 1.75 mH, 2 Ω; C5 (res) = 7.4 nF, 1 kV; C6 and C7 = 100 nF, 100 V; C8 (DC) = 15 nF, 400 V; R_{CSI} = 2.7 Ω, 1 W

State	V_{IN} (V)	P_{in} (W)	PF	V_{lamp} (V)	I_{lamp} (mA)	I_{hb} (mA)	P_{lamp} (W)	f_{osc} (kHz)	t_{ph} (s)
Normal	120	13.7	0.6	113.3	102	302	11.6	47.38	0.8
Boost	-	17.7	-	95	159	309	15.1	39.16	-

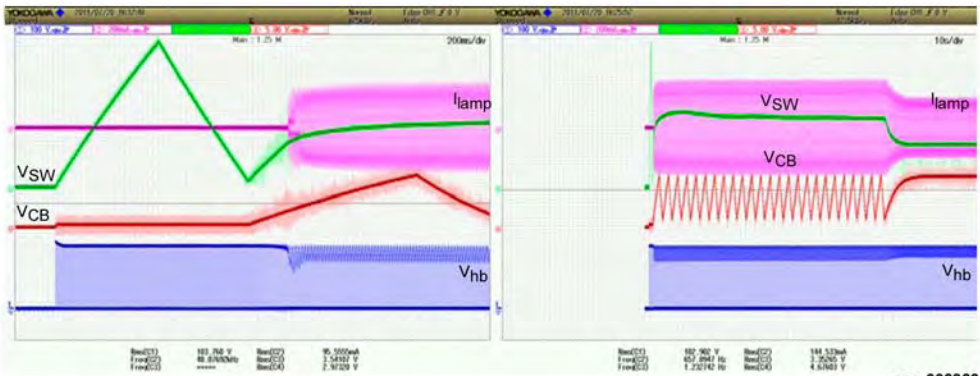


Fig 16. 15 W GE CFL

9. References

[1] **UBA2212 —** Half-bridge power IC family for CFL lamps data sheet.

10. Legal information

10.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

10.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

10.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

11. Contents

Date of release: 19 April 2012
Document identifier: UM10525