

UM12196

RDBESSK358BMU battery management unit user guide

Rev. 1.0 — 10 December 2024

User manual

Document information

Information	Content
Keywords	RDBESSK358BMU, BMU, battery management unit
Abstract	This user manual describes the RDBESSK358BMU battery management unit (BMU). The board features the S32k358 MCU, along with communication interfaces, a TPL gateway, and a secure element.



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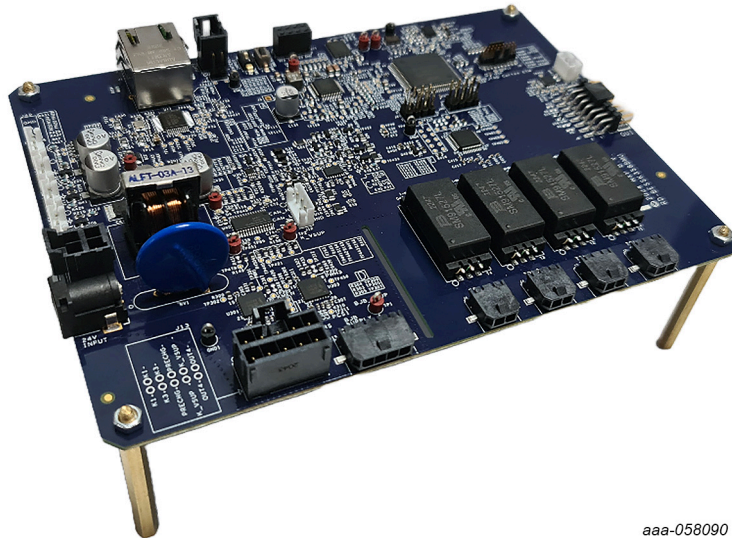
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WARNING**Lethal voltage and fire ignition hazard**

The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. This product shall never be operated unattended.

1 Introduction

The RD-BESSK358BMU is the fourth version of NXP's reference battery management unit (BMU) for evaluation and development purposes. It is suitable for faster time to market of high-voltage energy storage system (HVBESS) hardware and software. In order to achieve the HVBESS goals, the board contains: S32K358, FS2633, HB2000, TJA1463, PCA2131, MC33XS2410EL, and NCJ37B0HN devices. Together, with RDBESS774A3EVB, it allows the user to connect a lithium battery in a wide variety of cell configurations.



aaa-058090

Figure 1. RD-BESSK358BMU board

2 Finding kit resources and information on the NXP website

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <http://www.nxp.com>.

The information page for the RDBESSK358BMU evaluation board is at <http://www.nxp.com/RDBESSK358BMU>. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a Getting Started tab. The Getting Started tab provides quick-reference information applicable to using the [RDBESSK358BMU](#) evaluation board, including the downloadable assets referenced in this document.

The tool summary page for RDBESSK358BMU is [HVBESS Battery Management Unit \(BMU\)](#). The overview tab on this page provides an overview of the device, a list of device features, a description of the kit contents, links to supported devices and a Getting Started section.

The Getting Started section provides information applicable to using the RDBESS774A1EVB.

1. Go to <http://www.nxp.com/RDBESSK358BMU>.
2. On the Overview tab, locate the Jump To navigation feature on the left side of the window.
3. Select the Getting Started link.
4. Review each entry in the Getting Started section.
5. Download an entry by clicking the linked title.

After reviewing the Overview tab, visit the other related tabs for additional information:

- **Documentation:** Download current documentation.
- **Software and tools:** Download current hardware and software tools.
- **Buy/Parametrics:** Purchase the product and view the product parametrics.

After downloading files, review each file, including the user guide, which includes setup instructions.

3 Getting ready

Working with the RDBESSK358BMU requires the kit contents, additional hardware, and a Windows PC workstation with installed software.

3.1 Kit contents

The kit contents include:

Table 1. Kit contents

Item number	Description	Qty
RD-BESSK358BMU	91654 . RD-BESSK358BMU	1
700-91654	PWA, RD-BESSK358BMU	1
901-77727	BAG, ZIP CONTAINS 570-75251 M3 FASTER 280-77298(20mm F/M), 280-77405	1
280-77298	NYLON MT20MM FEMALEJMALE, STANDOFF	4/set
280-77405	NYLON, M3 NUT, HEX, FASTENER	4/set
600-10036	CABLE, NXP-BESS, Contactors Interface, 10 PINs, 300 MM, 16 AWG, 1722583110	1
600-10035	CABLE, NXP-BESS, 24V power Input to the BMIJ, 4 PINs, 300 MM, 16 AWG, 1722583104	1
600-10039	CABLE, NV-BESS, Interlock Loop, 2 PINs, 300MM, 16 AWG, 1722563102	1
600-10038	CABLE, NXP-BESS, CAN FD cable, 3 PINs, 300MM, 18 AWG, EHR-3 & DB9 Adaptor	1
600-10040	CABLE, NXP-BESS, RS485 Cable, 3 PINs, 300MM, 22 AWG, EHR-3 & 1181050	1
600-77624	CABLE, CUSTOM, TPL CABLE, 2 pin, L 500mm, 0436450200	1
400-10018 (DRQ30018331)	POWER SUPPLY, 24V 50 W ACIDC, DESKTOP ADAPTER, 72" (1.83m), SD150-24-U.P6	1
600-75423	AC CORD, POWER,3 COND.CONTINENTAL JAPAN/C13, (PSE)	1

3.2 Additional hardware

To use this kit, the following hardware is recommended:

- [RDBESS772BJBEVB](#) - BESS1500 Battery Junction Box (BJB)
- [RDBESS774A3EVB](#) - 1500 V Battery Energy Storage Reference Design
- [BATT-18EMULATOR](#) - 18-Cell Battery Pack Emulator to Supply MC33774 BCC EVBs
- [POLYBESS1500V1](#) - Polycarbonate structure for RD-BESS1500BUN evaluation board

4 Getting to know the hardware

4.1 Chipset features

The RD-K358BMU board is equipped with the latest NXP chipset. The base of the BMU board is a microcontroller unit (MCU) from the S32K3xx family and system basis chip (SBC) FS2633. These components have been designed for ASIL-D/SIL2 systems, such as a battery management system.

S32K358 MCU key features:

- 1x LS Arm[®] Cortex-M7[®] + 1x Cortex-M7 @ 240 MHz, 8 MB Flash, 1152 KB SRAM
- Fault collection and control unit, watchdog, clock/power monitor
- 8x CAN-FD, 6xLPSPi, 32ch FlexIO
- 3x 24 16-bit EMIO timer, 3x 24ch 12-bit ADC
- HSE security engine
- MAXQFP172 package reduces footprint by up to 55 %

FS2633 SBC key features:

- Configurable power management integrated circuit (PMIC), third generation of NXP safety SBCs
- Support system Low-power modes (standby and LPOFF) with long duration timer (LDT)
- 2x LDO configurable 3.3 V or 5.0 V, up to 300 mA
- 2x 125 mA trackers for external sensors supply redundancy
- Voltage reference
- Dual fail-safe outputs with delay for increased fail-safe system behavior
- Front boost converter for HEV

4.2 Board features

Interfaces

- 1x CAN-FD interface with signal improvement capability (SIC)
- 1x gigabit Ethernet interface
- 1x RS-485 interface
- 4x TPL interface (Loopback mode supported)
- 2x contactor drivers with pulse width modulation (PWM) economization and current monitoring
- 1x precharge contactor driver
- 1x short-circuit protected output reserved for future use
- Short-circuit and reverse polarity-protected output for BJB power supply

Advanced features

- PWM-based interlock pilot loop
- MCU independent real-time clock source
- Secure element and external flash to support battery passport framework

Wake-up sources

- SBC – periodic wake-up
- CAN-FD – controller unit and wake-up unit
- ETPL – wake up from CMU

4.3 Block diagram

The RD-K358BMU board is intended, but not limited, to work in a system as described below. The proposed system has three parts:

1. The BJB takes care of current measurement, high-voltage measurements, and isolation monitoring. For details about the BJB, refer to [the BJB user manual](#).
2. The cell monitoring unit (CMU) is intended to be connected directly to battery cells. It takes care of the cell-voltage measurement, temperature measurement, cell balancing, and the battery module pressure measurement. In the proposed system, 24 analog front-end (AFE) controllers are distributed across eight PCBs. AFEs are connected in two daisy-chains distributed into eight clusters in so-called half-distributed configuration. As a given example, the system can monitor 432 cells for LFP chemistry using 24 AFEs. This is just a typical example and not a system limitation. By adding more AFEs into the daisy chain, the system can monitor more cells if required. The communication protocol supports up to 62 nodes, which means more than 1000 cells. The current design is rated for 1500 V and can withstand a maximum pack voltage of 1800 V. The maximum pack current is 500 A. For more details about the CMU, refer to [the CMU user manual](#) or AN13233.
3. The battery management unit (BMU) is based on the S32K358 MCU. It is responsible for collecting all data communicated to the microcontroller unit (MCU) and makes important safety decisions. The detailed functionality of this unit is described in this document.

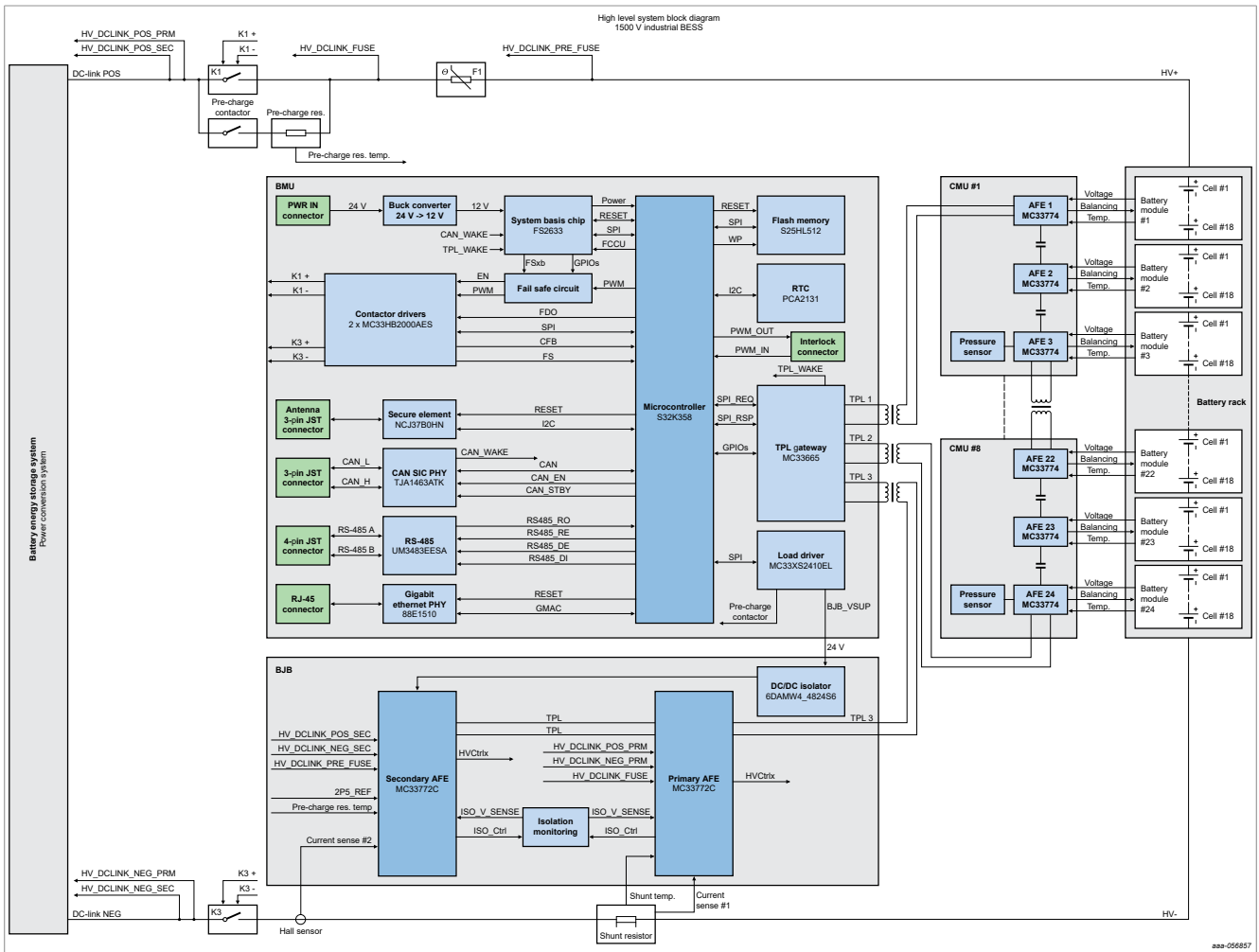


Figure 2. 1500V HVBESS system configuration example for LFP chemistry

5 Configuring the hardware

5.1 Connectors and integrated circuit location

Figure 3 shows distribution of connector and integrated circuit on the board. For detailed connector pinout, refer to [Connectors](#).

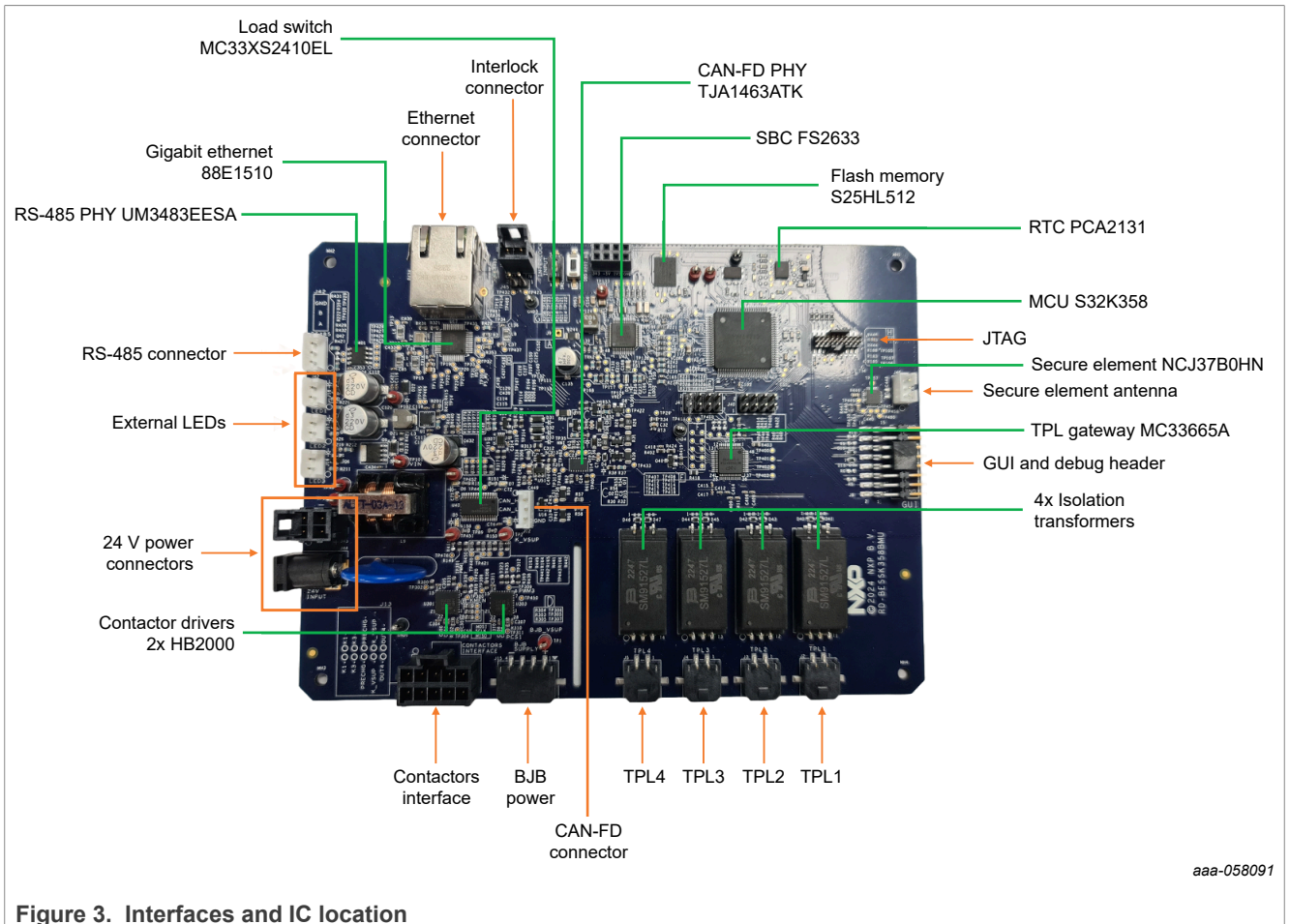


Figure 3. Interfaces and IC location

5.2 Power supply

5.2.1 BMU power supply input

The board is supplied from either connector J43 (pins 1 and 2 for GND and pins 3 and 4 for 24 V) or J44 using a 2.1 mm DC barrel jack plug. This board has built-in polarity protection and power supply input filtering. All standby functions on this board are enabled by default. To optimize current consumption in Standby mode, the user can disable functions that are not used in application. This may be done by removing zero ohm resistor (R422 – TPL, R62 – CAN FD, R8 - RTC and RS-485 PHY, R447 – secure element, R443 – flash memory).

Table 2. Board input power supply specification

Parameter	Symbol	Min	Typ	Max	UNIT
Input voltage	+24V_IN	20	24	30	V
Run current consumption	I _{RUN}		150		mA

Table 2. Board input power supply specification...continued

Parameter	Symbol	Min	Typ	Max	UNIT
Input current in LPOFF mode	I_{LPOFF}		30		μA
Standby current with minimal configuration	$I_{STBYMIN}$		46 ^{[1] [2]}		μA
Standby current adder for TPL	$I_{STBYTPL}$	-	10.5	-	μA
Standby current adder for CAN FD transceiver	$I_{STBYCAN}$	-	13	26	μA
Standby current adder for RTC + RS-485 PHY	$I_{STBYRTCRS-485}$	-	1.1	1.365	μA
Standby current with all standby functions enabled	I_{STBY}		70.6 ^{[1] [3]}		μA

[1] All values measured at 23 °C, +24V_IN = 24 V, unless stated otherwise, LPOFF and standby current measured at +24V_IN input terminals.

[2] Enabled standby functions: SBC, load drivers.

[3] Enabled standby functions: SBC, load drivers, battery gateway, CAN FD, RTC, RS-485 PHY.

Internal power supplies are managed by the FS2633 SBC. The FS26 is a family of automotive safety SBC devices with multiple power supplies designed to support entry and mid-range safety microcontrollers, such as S32K3. The SBC Switch mode power supply is also active in Standby mode. It ensures higher efficiency and lower standby current in comparison to a conventional approach with LDOs.

The FS26 features multiple Switch mode regulators and two LDO voltage regulators to supply the microcontroller, sensors, peripheral ICs, and communication interfaces. It offers a high-precision voltage reference available to the system and reference voltage for two independent voltage tracking regulators.

5.2.2 Onboard power distribution

The FS2633 onboard SBC ensures voltage regulation, overvoltage, undervoltage and overcurrent protections for low-voltage rails present on this board. Loads across power rails are distributed as shown in Figure 4 and Table 3. For more information about power supply distribution in Standby mode, see Section 5.2.3.

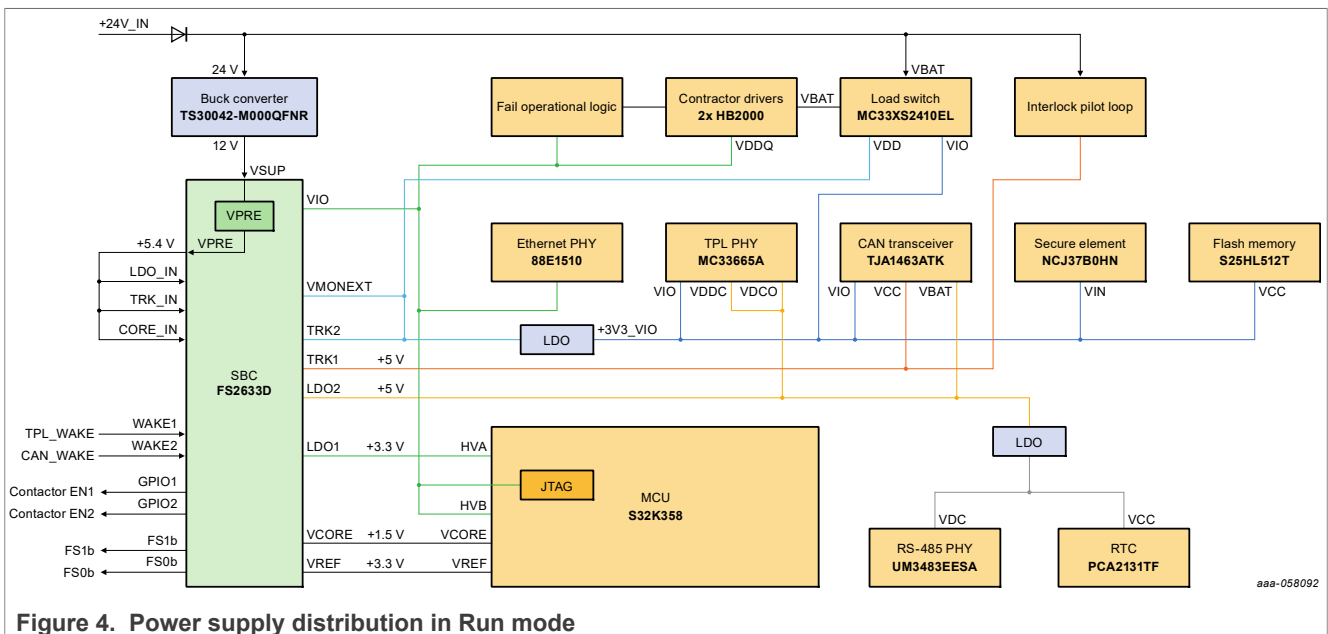


Figure 4. Power supply distribution in Run mode

Table 3. Internal power supply distribution

SBC output	Loads	Net alias	Availability	Voltage [V]	Max. out current [mA]
VPRE	LDO1, LDO2, TRK1, TRK2, VCORE	FS26_VPRE	RUN, STANDBY	5.4	1500

Table 3. Internal power supply distribution...continued

SBC output	Loads	Net alias	Availability	Voltage [V]	Max. out current [mA]
VCORE	MCU core	V15_MCU	RUN	1.5	1650
LDO1	MCU HVA, HVB, contactor drivers, Ethernet PHY, JTAG	+3V3_LDO1	RUN	3.3	400
LDO2	CAN FD, Battery gateway, RTC, RS-485 PHY ^[1]	+5V_LDO2	RUN, STANDBY	5.0	400
TRK1	CAN's Vcc, interlock loop	+5V_TRK1	RUN	5.0	150
TRK2	Load drivers, Vio ^[2]	+5V_TRK2	RUN	5.0	150
VREF	MCU ADC reference	VREF	RUN	3.3	30

[1] RTC and RS-485 PHY are connected using external LDO to regulate voltage to 3.3 V from VLDO2 voltage.

[2] CAN-FD, load drivers, battery gateway, secure element, flash memory are connected using external LDO to regulate voltage to 3.3 V from VTRK2 voltage.

5.2.3 Power modes and wake-up

5.2.3.1 BMU power modes

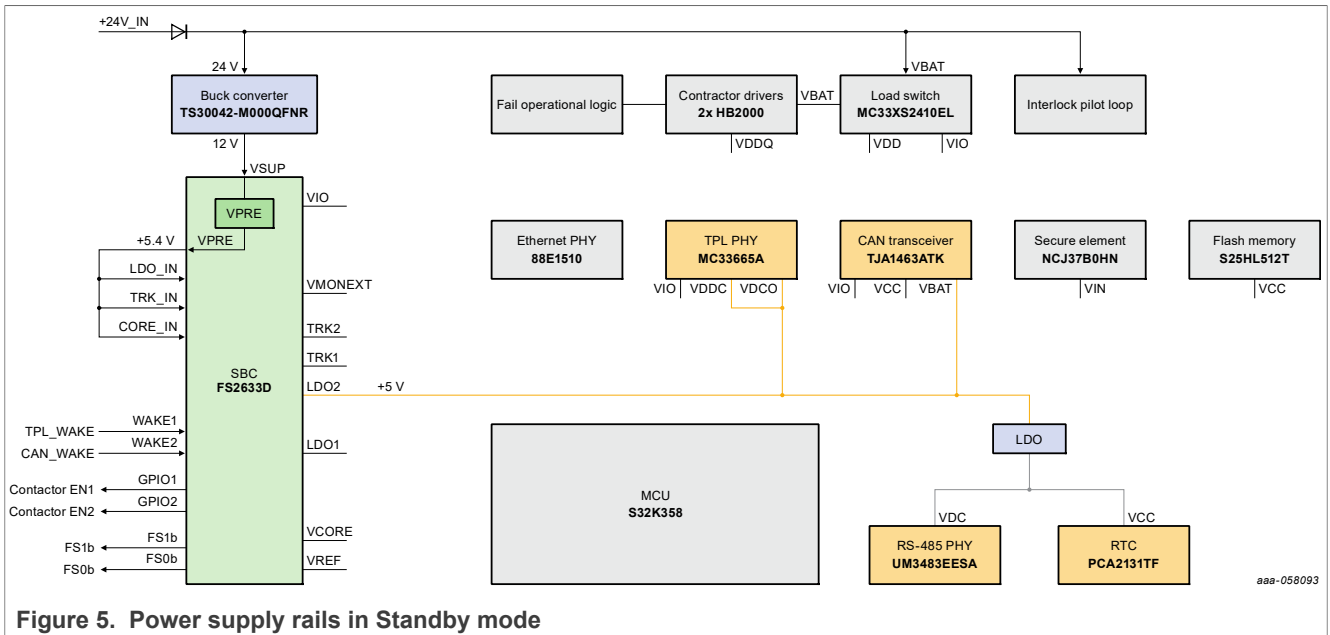
The BMU board can be operated in at least three power modes:

- Run
- Standby
- LPOFF

In Run mode, all onboard devices are supplied, and the system has access to full BMU functionality. Power supply distribution and voltage levels are shown in [Figure 5](#).

In Standby mode, board current consumption is reduced. Only necessary ICs are supplied, most SBC power rails, including the MCU power supply, are switched off. Switching from Run into Standby mode is done by a go-to-standby SPI request coming from the MCU to the SBC. If all conditions described in the SBC data sheet are met, the SBC enters Standby mode. Power supply distribution is shown in [Figure 5](#).

In LPOFF mode, the board has minimal power consumption, however most of the functionality is disabled, including most of the wake-up sources. During LPOFF, LDO2 output is disabled, which means the only possible wake-up source is the SBC (for example, SBC LDT).



5.2.3.2 BMU wake-up sources

The board has three possible wake-up sources:

- Internal SBC event (for example, long duration timer (LDT))
- MCU CAN (TJA1463ATK) available at SBC WAKE2 input
- CMU ETLF wake available at SBC WAKE1

5.2.4 SBC Debug mode

5.2.4.1 MCU firmware debugging in SBC Debug mode

To continuously check the activity of the microcontroller software and its ability to perform basic computing, a challenger watchdog is implemented through the SPI bus. The verification is performed by the FS26 while waiting for a specific response from the microcontroller during a predefined period called window.

If the watchdog is not properly refreshed, SBC safety outputs FSxB and RSTB are asserted, and the SBC tries to recover MCU functionality by resetting its power. This process is accompanied by a blinking orange LED D26.

Note: Loading firmware over JTAG in this mode is not supported.

Periodic power supply resetting, or an issue with firmware loading typically happens in the following cases:

- Missing SBC WD refresh routine
- Loading new BMU firmware via JTAG without activating Debug mode
- Using code breakpoints during debugging without activating Debug mode
- Missing or wrong BMU firmware

Warning

- An MCU firmware update in SBC Normal mode will not work. To be able to flash new firmware or do software debugging, SBC Debug mode must be activated.
- Entering SBC Debug mode is described in section [Section 5.2.4.1.1](#).

5.2.4.1.1 Entering SBC Debug mode

The debug circuit is intended for development purposes only and must be removed for production.

There are two options to enter Debug mode. It is recommended to use the first option:

1. Press and hold SW1 (or set SW2 to On position) while connecting the 24 V power supply and release SW1 after the 24 V supply is connected. Make sure that D26 is solid On afterward.
2. FS2633 debug pin is accessible at connector J11 pin 4. Applying a voltage between 2.5 V and 6 V to this pin, before the board power supply is connected, ensures Debug mode.

Make sure the 24 V power supply is in range from 20 V to 30 V while entering Debug mode. The power supply current limit must be at least 2 A to meet sufficient input voltage steepness for Debug mode entering. If there is slow input voltage ramp-up, Debug mode may not be activated. This may typically happen when a power supply with a soft-start function is used.

A blinking D26 indicates the MCU power supply is being reset, which means Debug mode was not successfully activated.

5.2.4.1.2 Leave Debug mode

For safety reasons, FSxB safety outputs' functionality is limited in Debug mode. To enable full board functionality (for example, contactor control) Debug mode must be left. The following are the options to leave Debug mode. Make sure that SW2 is in Off position.

1. To leave Debug mode, the BMU power supply must be disconnected and connected again. The actual SBC state can be checked in the FS_STATES register via SPI.
2. A request to leave Debug mode can be entered into the SBC FS_STATES register via SPI.

Warning: Avoid an immediate and unconditional leave Debug mode command in the MCU firmware. Such a command may cause dead lock, when loading of new MCU firmware through JTAG may not be possible, as the SBC is always switched to Normal mode right after startup in such a case.

5.2.5 Connectors

5.2.5.1 Power connectors

The BMU board is equipped with two power connectors: a 2.1 mm DC barrel connector (J44) and a 4-pin through-hole 3.5 mm connector (J43). Both serve the same function: provide 24 V to power the BMU. The part number and description for these connectors can be found in [Figure 6](#) and [Table 4](#).

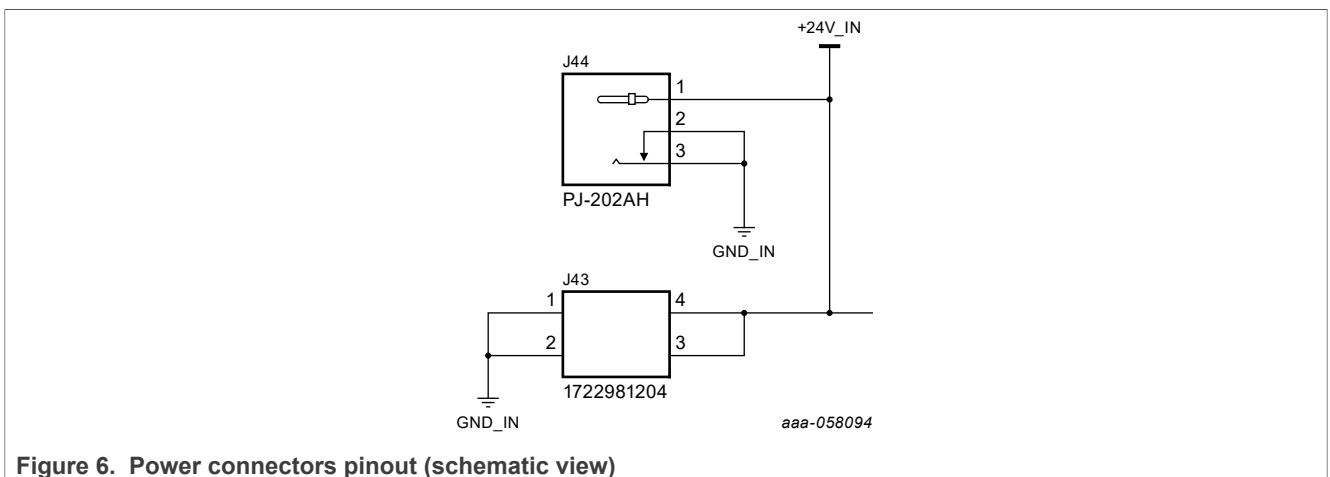


Figure 6. Power connectors pinout (schematic view)

Table 4. Power connector (J43) PN specification

Location	Description	Part number
PCB side	Connector header through hole four position 0.138" (3.50 mm)	1722981204
Wire side	Four rectangular connectors - housings receptacle black 0.138" (3.50 mm)	1722583104
	4x pre-crimped lead Ultra-Fit tangless female-to-Ultra-Fit tangless female, Tin (Sn) plating, 300.00 mm length, 16 AWG, Black	797582142

Table 5. Power connector (J44) PN specification

Location	Description	Part number
PCB side	Power barrel connector jack 2.10 mm ID (0.083"), 5.50 mm OD (0.217") through hole, right angle	PJ-202AH

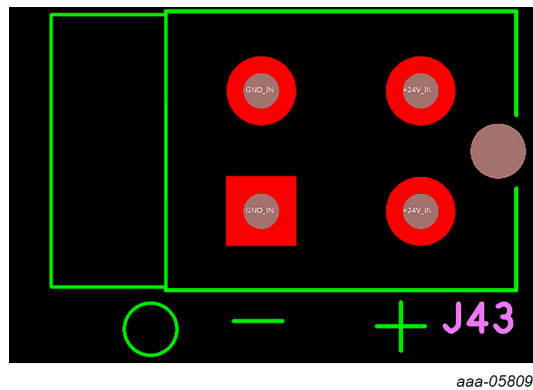


Figure 7. Power connector (J43) pinout

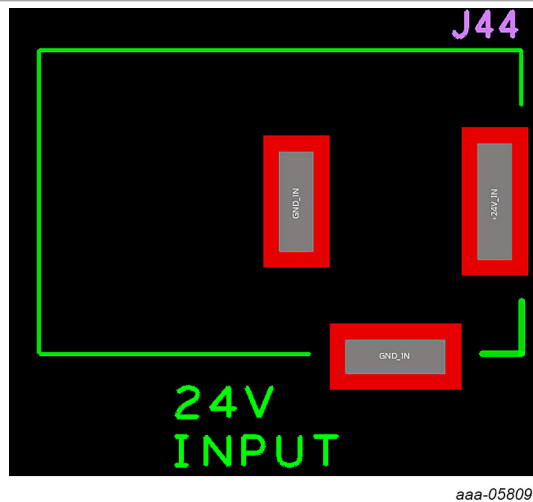


Figure 8. Power connector (J44) pinout

5.2.5.2 GUI and debug header

J8 is the debug header and provides accessibility to several MCU pins with I²C, SPI, FlexIO or UART capabilities. This is intended for HW/SW debugging only and not intended for the HW production version. A detailed pinout is shown in [Figure 9](#).

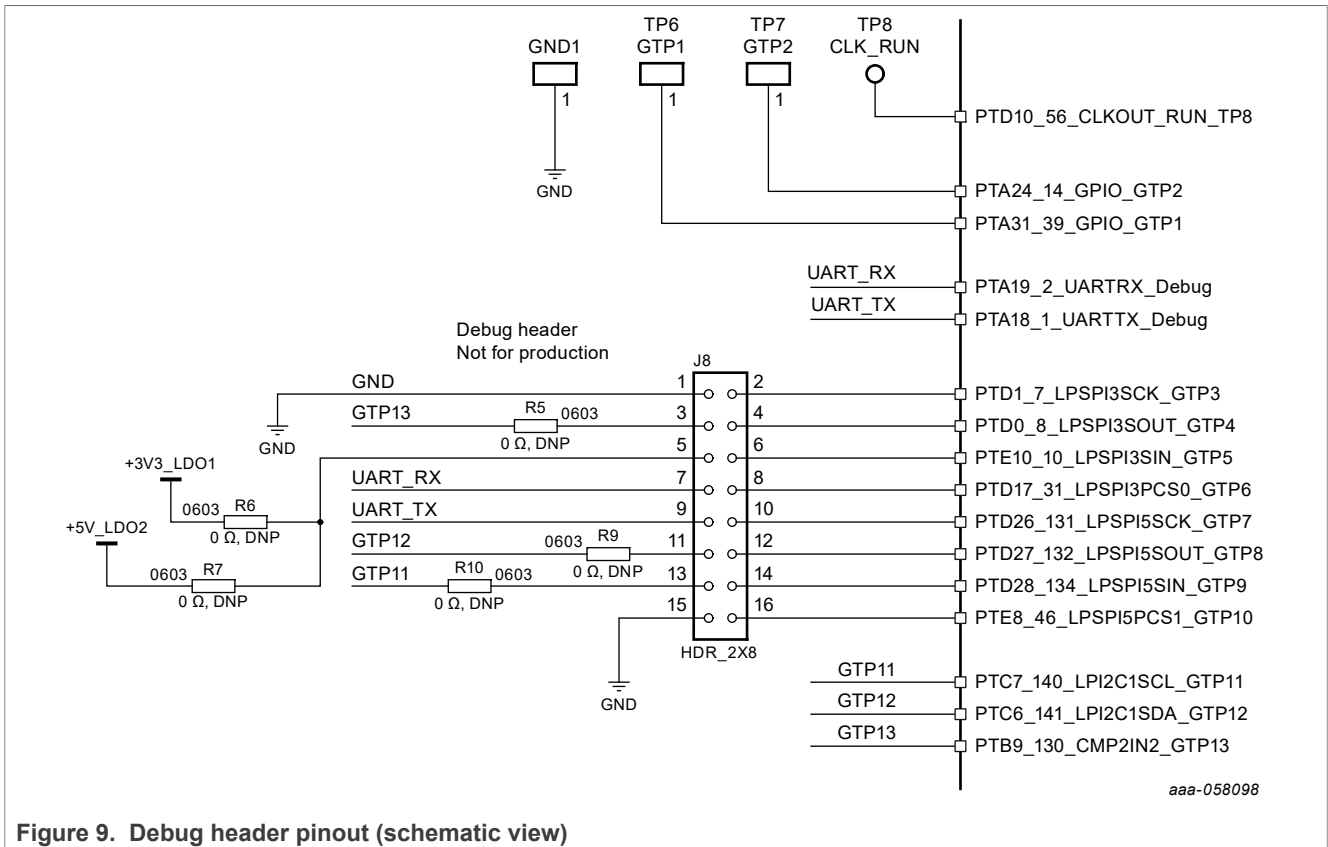


Figure 9. Debug header pinout (schematic view)

The board supports connection to a graphical user interface (GUI) over the JTAG debug probe or over the serial line. If the serial interface on the J8 header is used, it is necessary to use a 3.3 V USB to UART adapter to connect to computer, (adapter included in the board package). See [Section 5.2.6.5](#) for more information regarding the UART connection.

5.2.5.3 JTAG interface

The board is equipped with a 20-pin 1.27 MM ARM Cortex Debug + ETM connector (Samtec FTSH-110). This interface supports JTAG, SWD, and tracing for the onboard S32K358 MCU. When the Serial debug protocol is used, the TDO signal can be used for serial wire viewer output for trace capture. The connector also provides a 4-bit wide trace port for capturing traces that require a higher trace bandwidth (for example, when ETM trace is enabled).

The reference designator for this connector is J6. Pinout is shown in [Figure 10](#).

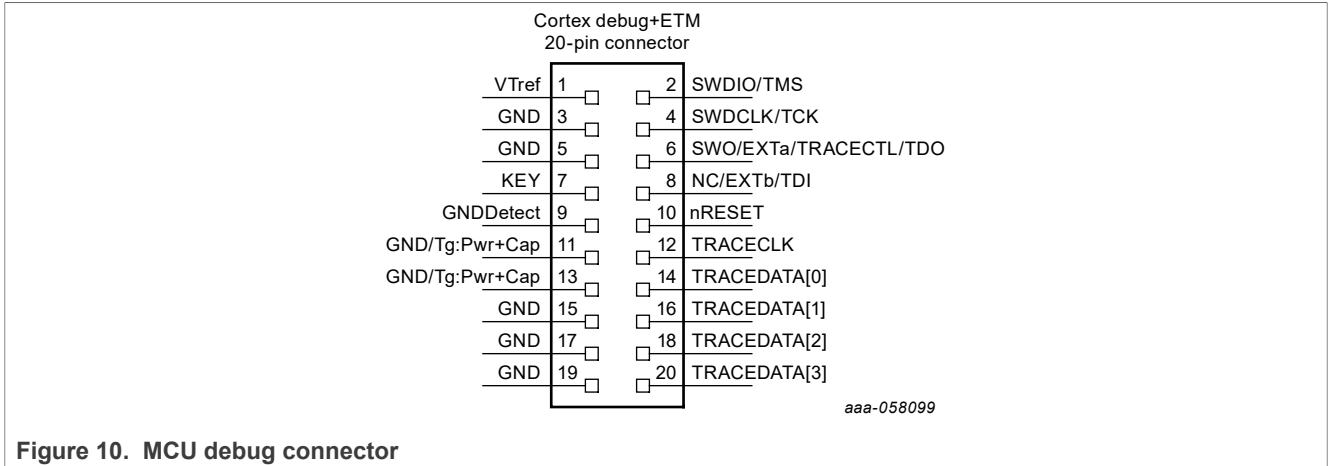


Figure 10. MCU debug connector

5.2.5.4 Ethernet interface

The board is equipped with an IEEE 802.3 compliant and UL certified single port 10/100/1G/5G Base-T RJ-45 connector (Abracon LLC ARJM11C7-502-AB-ER2-T) that is suitable for CAT5 and CAT6 UTP cabling. This interface supports Modbus protocol and enables the BMU board to communicate with the control unit and can be used to display the cell voltages, cell temperature, battery module pressure, pack voltages/current, and control the entire system via the BMS GUI.

The reference designator for this connector is J1. Detailed pinout is shown in [Figure 11](#).

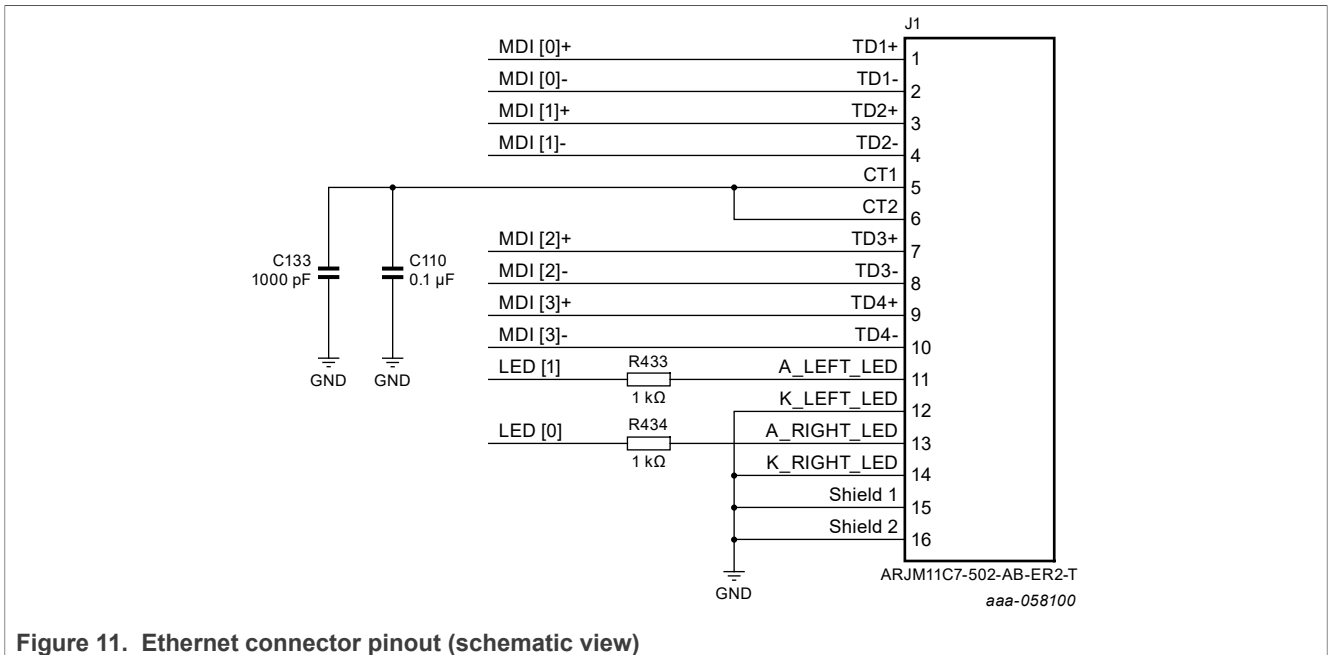


Figure 11. Ethernet connector pinout (schematic view)

5.2.5.5 RS-485 interface

For the RS-485, the board has a 3-pin, 0.098" (2.5 mm) JST connector (JST B3B-EH-A). This interface supports Modbus protocol and enables the control unit to communicate with the S32K358 MCU over the serial line (LPUART0). It can also be used to display the cell voltages, cell temperature, battery module pressure, pack voltages/current, and control the entire system via the BMS GUI.

It is necessary to use a USB to RS-485 converter to connect the BMU board to the computer (adapter included in board package). See [Section 5.2.6.3](#) for more information regarding UART connection.

The reference designator for this connector is J42. Detailed pinout is shown in [Figure 12](#).

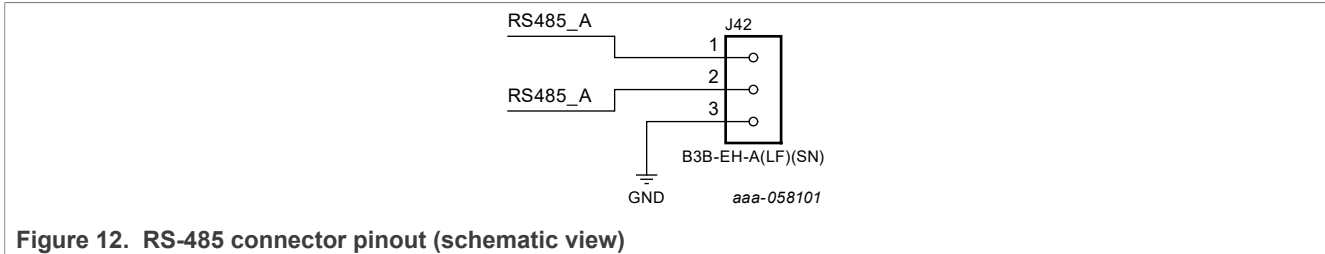


Figure 12. RS-485 connector pinout (schematic view)



Figure 13. RS-485 cable



Figure 14. USB to RS-485 adapter

Table 6. RS-485 cable pinout

Signal name	PIN #	Wire color
RS485_A	1	Red
RS485_B	2	Blue
GND	3	Black

Table 7. RS-485 cable PN specification

Location	Description	PN.
PCB side	Connector header through hole three position 0.098" (2.5 mm)	B3B-EH-A(LF)(SN)
Wire side	Three rectangular connectors - housings receptacle natural 0.098" (2.5 mm)	EHR-3
	Socket contact tin 22-30 AWG crimp	SEH-001T-P0.6

5.2.5.6 CAN-FD interface

For the CAN interface, the board has a 3-pin, through 0.098" (2.5 mm) JST connector (JST B3B-EH-A). The board package includes a JST to a female DP9 cable that can be used to connect the BMU board with the control unit or to the CAN box during the development phase.

The reference designator for this connector is J12. Detailed pinout is shown in [Figure 15](#).

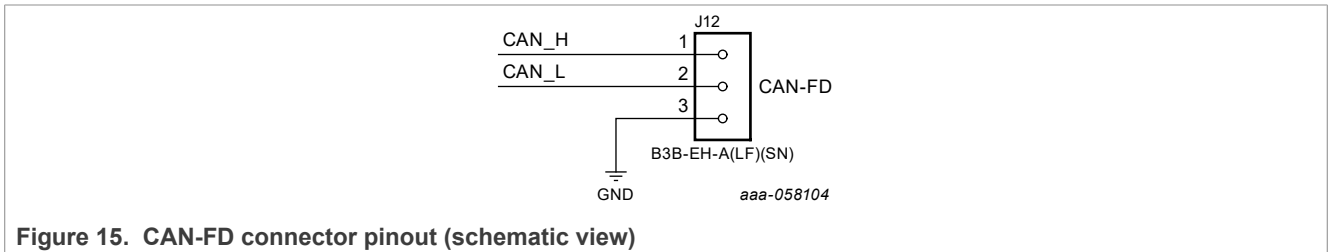


Figure 15. CAN-FD connector pinout (schematic view)

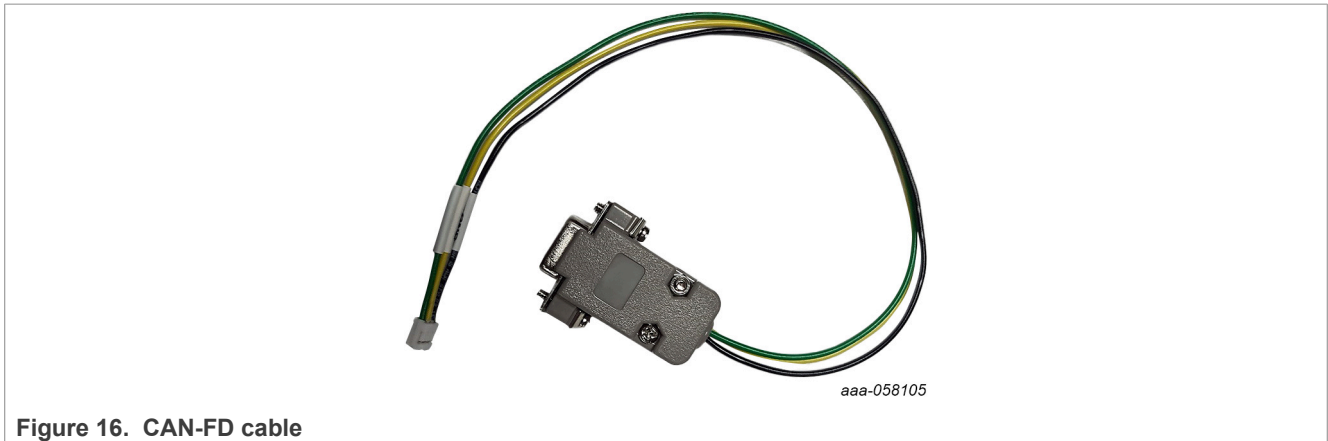


Figure 16. CAN-FD cable

Table 8. CAN-FD cable pinout (DP9 side)

Signal name	PIN #	Wire color
CAN_L	2	Yellow
CAN_H	7	Green
GND	3	Black

Table 9. CAN-FD cable PN specification

Location	Description	Part number
PCB side	Connector header through hole three position 0.098" (2.5 mm)	B3B-EH-A(LF)(SN)
Wire side	Three rectangular connectors - housings receptacle natural 0.098" (2.5 mm)	EHR-3
	Socket contact tin 22-30 AWG crimp	SEH-001T-P0.6
	Nine position D-sub receptacle, female sockets connector	61800925123

Table 9. CAN-FD cable PN specification...continued

Location	Description	Part number
	Nine position two-piece backshell connector 180° unshielded	40-9709H

5.2.5.7 Contactors connector

The board is equipped with a through hole ten positions 0.138" (3.50 mm) connector (Molex 1722981210) that can be used to connect the BMU board with the DC-link +, DC-link -, and precharge contactor. The connector can be used to connect the fourth channel of the load switch that is reserved for future use.

The reference designator for this connector is J13. A detailed pinout is shown in [Figure 17](#).

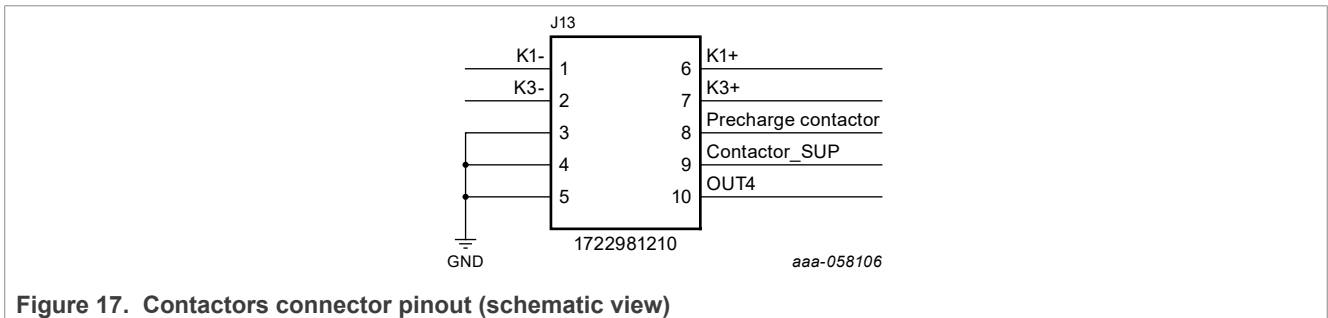


Figure 17. Contactors connector pinout (schematic view)

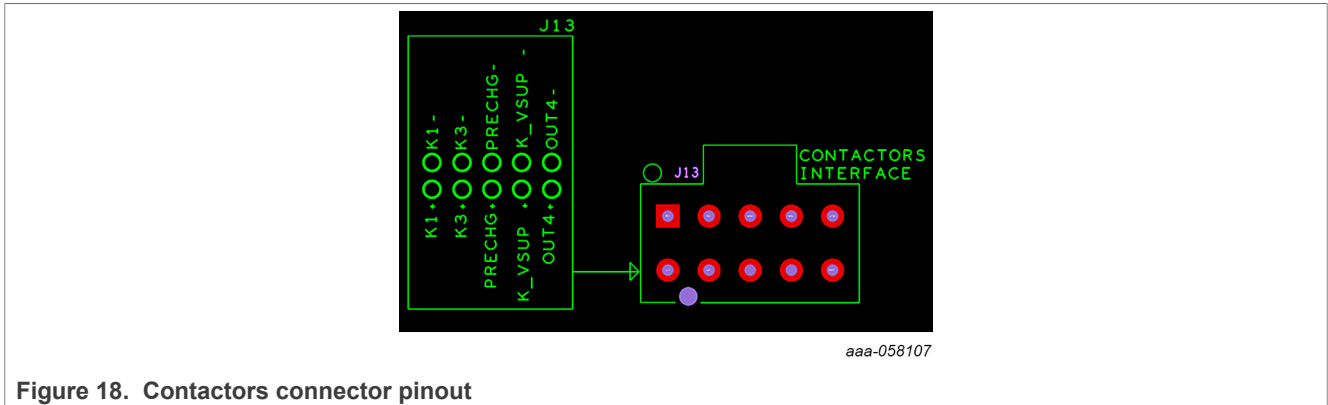


Figure 18. Contactors connector pinout

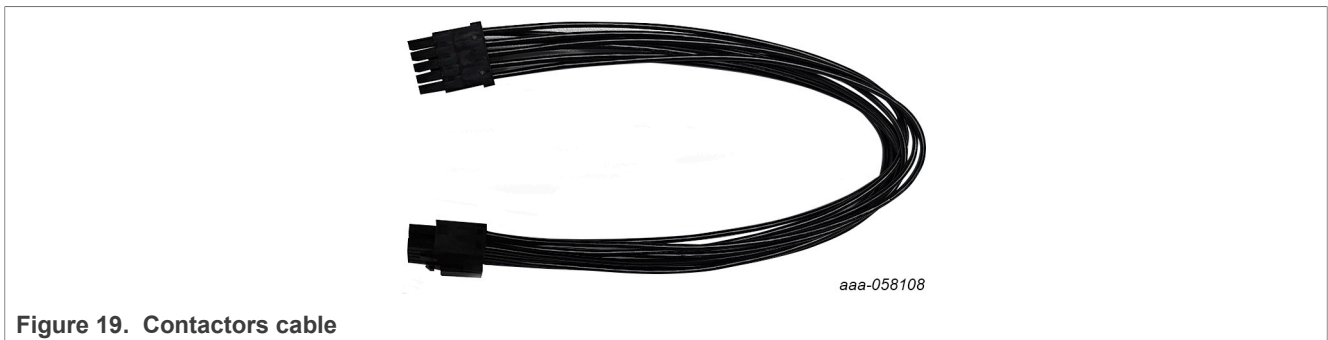


Figure 19. Contactors cable

Table 10. Contactors cable PN specification

Location	Description	Part number
PCB side	Connector header through hole ten position 0.138" (3.50 mm)	1722981210
Wire side	2x Ultra-Fit tangless receptacle housing, 3.50 mm pitch, dual row, ten circuits, black, glow-wire capable	1722583110

Table 10. Contactors cable PN specification...continued

Location	Description	Part number
	10x pre-crimped lead Ultra-Fit-tangless-female-to-Ultra-Fit-tangless-female, tin (Sn) plating, 300.00 mm length, 16 AWG, black	797582142

5.2.5.8 BJB power supply connector

The board is equipped with a four-positions surface mount right angle 0.118" (3.00 mm) connector (Molex 0436500413). This connector is connected to the first output channel of the load switch that provides short-circuit and reverse polarity protected 24 V output.

The reference designator for this connector is J15. A detailed pinout is shown in [Figure 20](#).

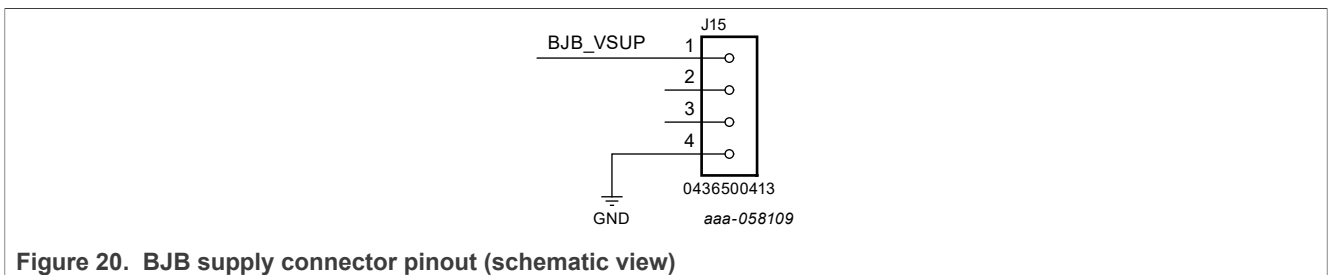
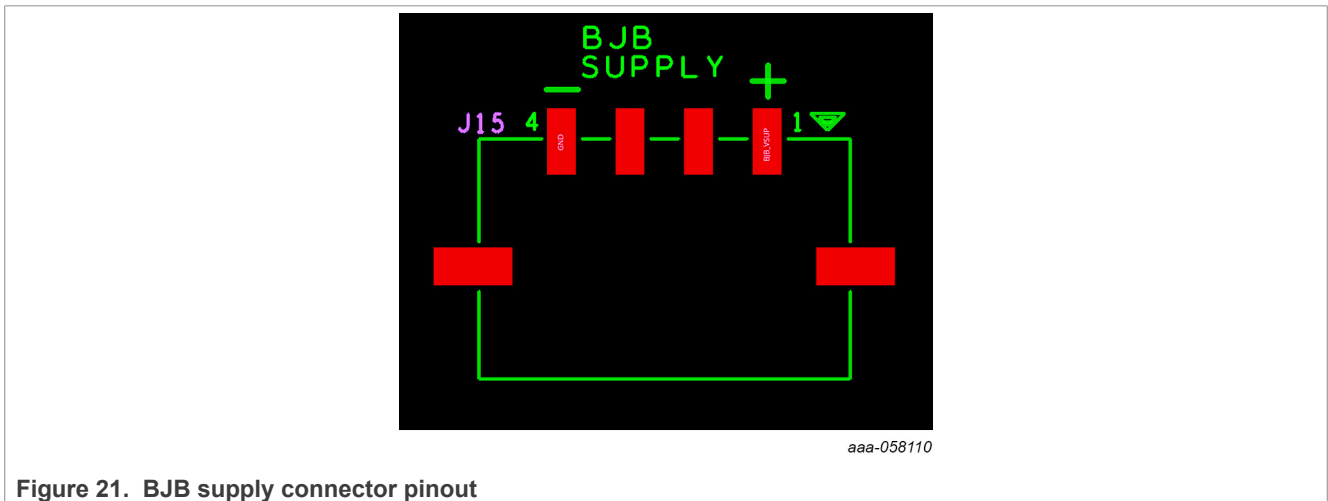


Figure 20. BJB supply connector pinout (schematic view)



aaa-058110

Figure 21. BJB supply connector pinout



aaa-058111

Figure 22. BJB supply cable

Table 11. BJB supply cable PN specification

Location	Description	PN.
PCB side	Connector header surface mount, right angle four position 0.118" (3.00 mm)	0436500413
Wire side	2x Micro-Fit 3.0 receptacle housing, single row, four circuits, UL 94V-2, glow-wire capable, black	436450410
	1x pre-crimped lead Micro-Fit 3.0 female-to-Micro-Fit 3.0 female, tin (Sn) plating, 450.00 mm length, 18 AWG, black	2147601125
	1x pre-crimped lead Micro-Fit 3.0 female-to-Micro-Fit 3.0 female, tin (Sn) plating, 450.00 mm length, 18 AWG, red	2147602125

5.2.5.9 Interlock connector

The board is equipped with a through hole two position 0.138" (3.50 mm) connector (Molex 1722861202) that interfaces the interlock loop input and interlock loop output signals. The board is equipped with a through hole two position 0.100" (2.54 mm) header (Würth Elektronik 61300211121) that can be used to short the interlock signals with a 2.54 mm jumper (Sullins Connector Solutions QPC02SXGN-RC).

The reference designator for this connector is J14. A detailed pinout is shown in [Figure 23](#).

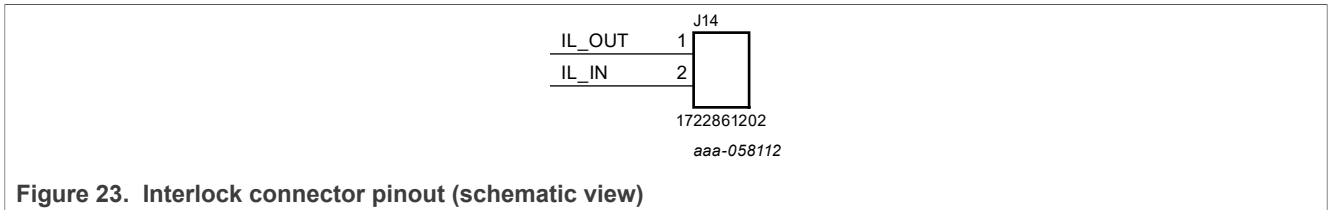


Figure 23. Interlock connector pinout (schematic view)

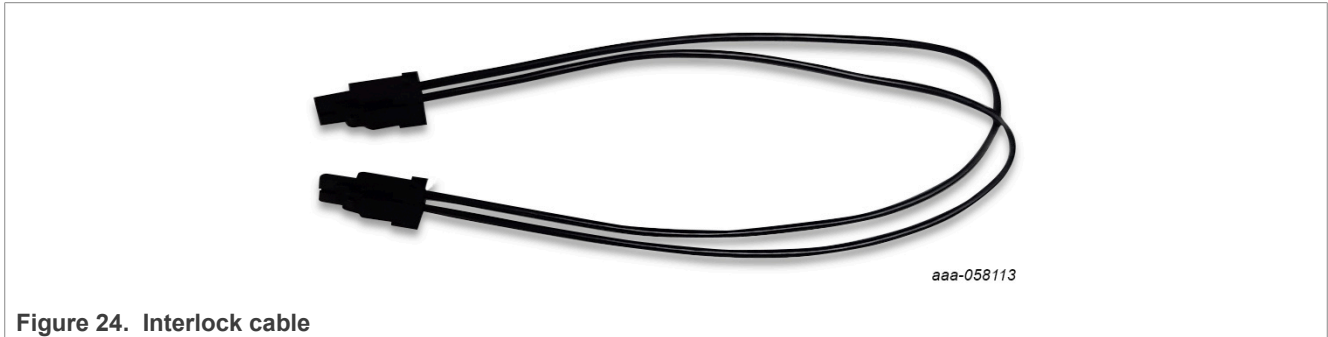


Figure 24. Interlock cable

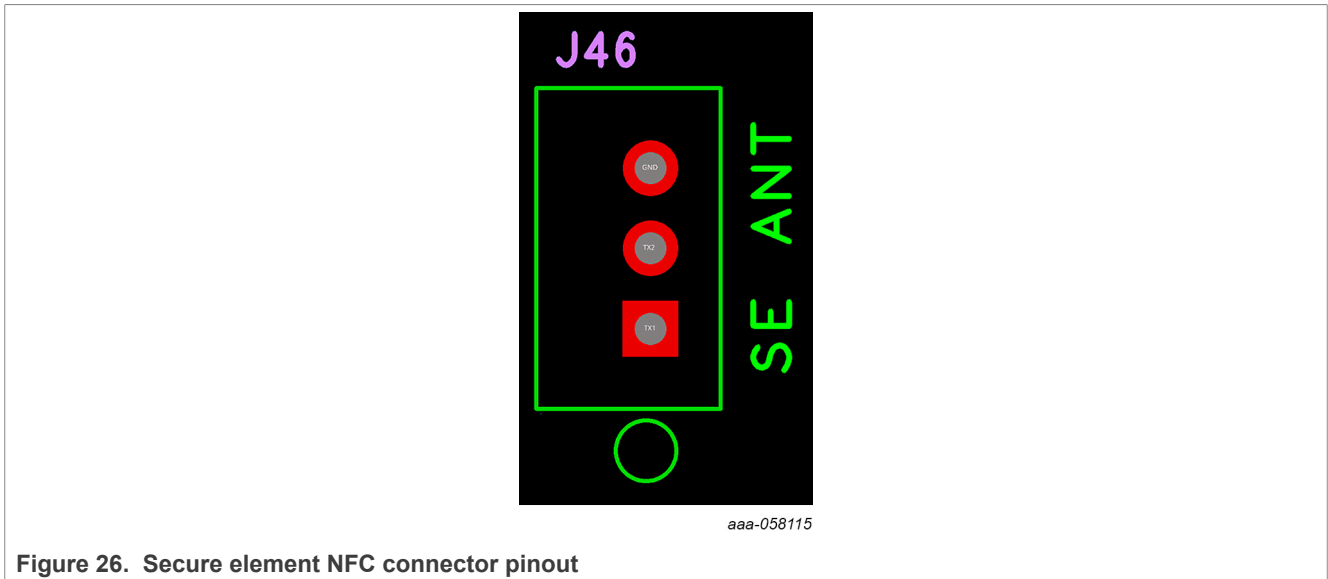
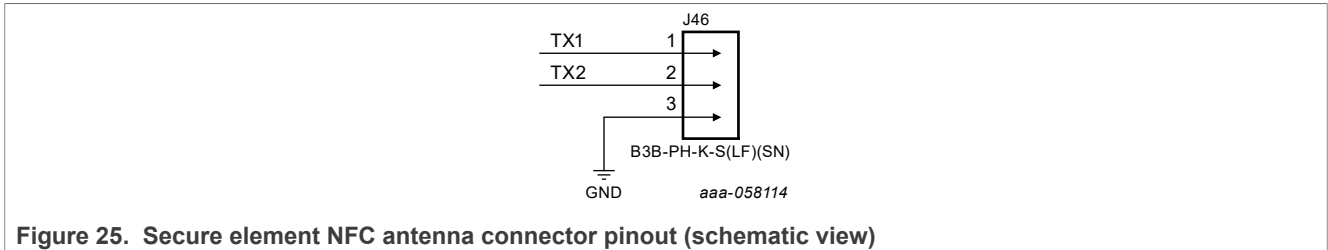
Table 12. Interlock cable PN specification

Location	Description	PN.
PCB side	Connector header through hole two position 0.138" (3.50 mm)	1722861202
Wire side	2x Ultra-Fit tangless receptacle housing, 3.50 mm pitch, single row, two circuits, black, glow-wire capable	1722563102
	2x pre-crimped lead Ultra-Fit tangless female-to-Ultra-Fit tangless female, tin (Sn) plating, 300.00 mm length, 16 AWG, black	797582142

5.2.5.10 Secure element antenna

The board is equipped with a through hole 3 position 0.079" (2.00mm) connector (JST B3B-PH-K-S) to support the secure element NFC antenna. The NFC interface is fully ISO/IEC 14443 and Tag Type A compliant. It supports data rates up to 848 kbit/s, symmetric and asymmetric data rate configurations. In addition, it supports a very high bit rate (VHBR) configuration of the contactless interface to minimize transaction time (3.2 Mbit/s in the card-to-reader direction).

The reference designator for this connector is J46. A detailed pinout is shown in the following figure.



5.2.6 Communication interfaces

5.2.6.1 ETPL ports

This reference design board uses electrical transport protocol link (ETPL) communication between BJB, CMU, and BMU. The board contains four isolated TPL ports available at connectors J2 (TPL 1), J3 (TPL 2), J4 (TPL 3), and J5 (TPL 4). Protocol supports up to 62 nodes per TPL chain. Transmitting data through these ports can be done through battery gateway MC33665A. The board supports either Single or Dual SPI mode.

Dual SPI mode is the default mode for this board. Dual SPI mode can be used to have independent data flows for requests and responses. In this setup, requests to MC33665A are fed through the request port and responses from the MC33665A are pushed via the response SPI controller to the MCU.

In Single SPI mode, both MC33665A SPIs are connected to a single MCU SPI, reducing the number of MCU resources used. The MCU works as a single SPI controller for the communication with the MC33665. Response data is transferred in parallel to request data. To enable this mode, R414, R416, and R417 must be populated on the PCB.

For more details about single and dual SPI modes, refer to the MC33665A data sheet.

Battery gateway Vdd is supplied even when the BMU is in Standby mode and MC33665A active high wake-up output is connected to SBC wake1. This ensures that the BMU unit can wake up when TPL wake-up frame is received.

The TPL ports connection and peripheral chip select assignment is shown in [Figure 28](#). [Table 13](#) summarizes the pinout between the battery gateway and MCU.

Table 13. Battery gateway pinout assignment

Port	Signal	SPI	MCU port
Response port	SCLK_RSP	LPSP1 PCS3	PTB14
	SDAT_RSP		PTB15
	CSN_RSP		PTB17
Request port	SDAT_REQ	LPSP2 PCS0	PTB27
	SCLK_REQ		PTE15
	CSN_REQ		PTE11
	SIN_RSP (for Single SPI mode only)		PTE16

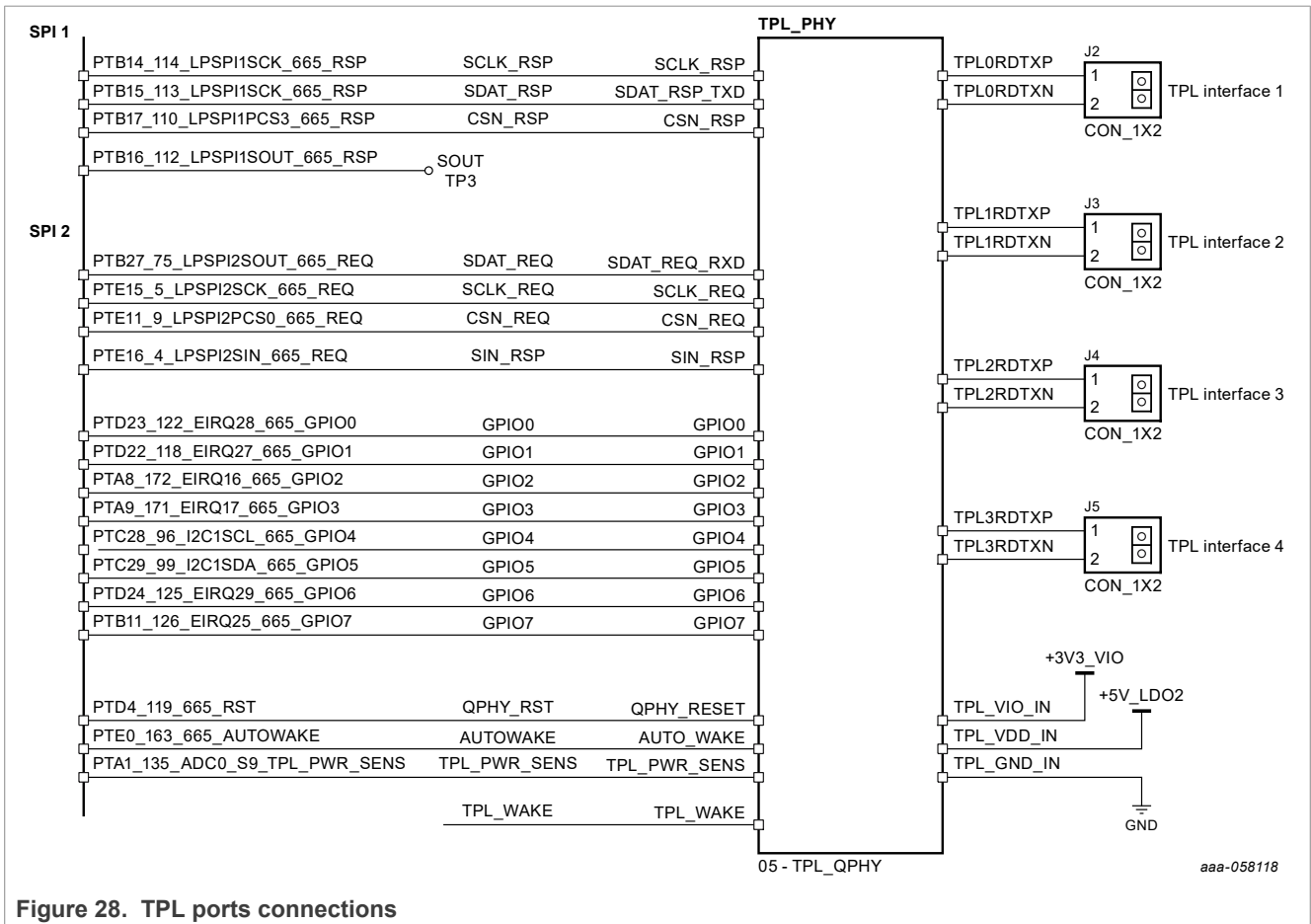


Figure 28. TPL ports connections

TPL ports are used for communication with the CMU and BJB units. These ports can be used as four separated daisy-chain ports or daisy chains with Loopback mode. Loopback mode provides additional safety, ensuring full functionality even if the daisy-chain wire is interrupted at one point.

Table 14. TPL port connector specification

Location	Description	Part number
PCB side	Micro-Fit 3.0 right angle header, 3.00 mm pitch, single row, two circuits, with solder tab, gold, glow-wire capable, black	436500214
Wire side	Micro-Fit 3.0 receptacle housing, single row, two circuits, UL 94V-2, glow-wire capable, black	436450210

5.2.6.2 Gigabit Ethernet interface

This reference design board uses the Ethernet interface to communicate between the BMU and the external control unit through the connector (J1). The Ethernet interface can also be used to monitor the system voltages, current and temperature, can be used to control the contactors, and can enable cell balancing through the BMS monitor GUI.

The Ethernet PHY has three separate electrical interfaces:

- MDI to copper cable
- RGMII
- The management interface

The MDI is always a media interface. The RGMII is always a system interface. The system interface is also known as MAC interface. It is typically the connection between the PHY and the MAC or the system microcontroller.

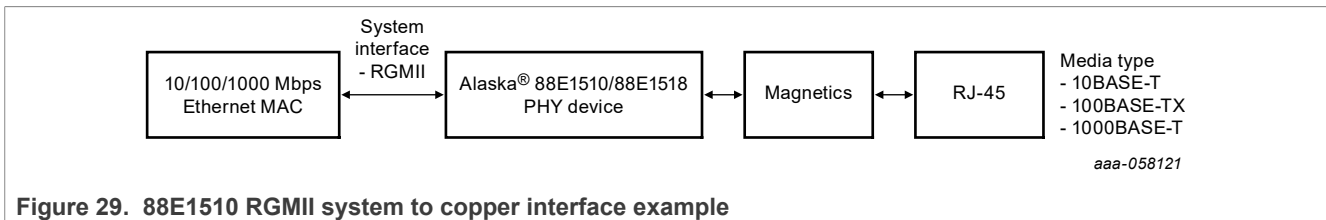


Figure 29. 88E1510 RGMII system to copper interface example

Software configuration

The management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3u clause 22 and clause 45 MDIO protocol.

MDC is the management data clock input and it can run from DC to a maximum rate of 12 MHz. At high MDIO fanouts, the maximum rate may be decreased depending on the output loading.

MDIO is the management data input/output and is a bidirectional signal that runs synchronously to MDC. The MDIO pin requires a pullup resistor in a range from 1.5 kΩ to 10 kΩ that pulls the MDIO high during the idle and turnaround phases of read and write operations.

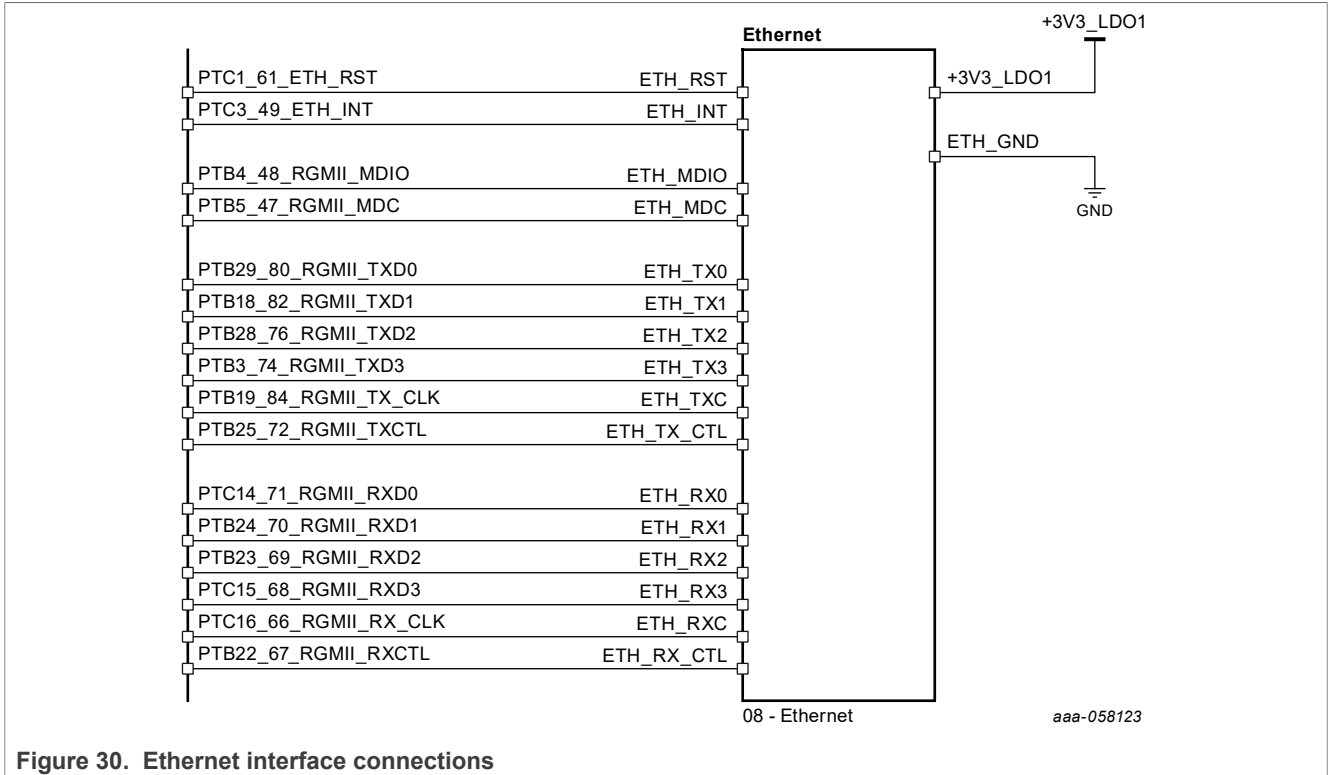


Figure 30. Ethernet interface connections

Table 15. Ethernet connector specification

Location	Description	PN.
PCB side	One port RJ45 through hole 10/100/1000 Base-T, AutoMDIX	ARJM11C7-502-AB-ER2-T
Wire side	Ethernet cable, UTP, patch lead, Cat6, RJ45 plug-to-RJ45 plug, blue, 1 m	PS11181

5.2.6.3 RS-485 interface

This reference design board uses the RS-485 interface to communicate between the BMU and the external control unit through the connector (J42). The RS-485 interface can also be used to monitor the system voltages, current and temperature, can be used to control the contactors, and enable cell balancing through the BMS monitor GUI.

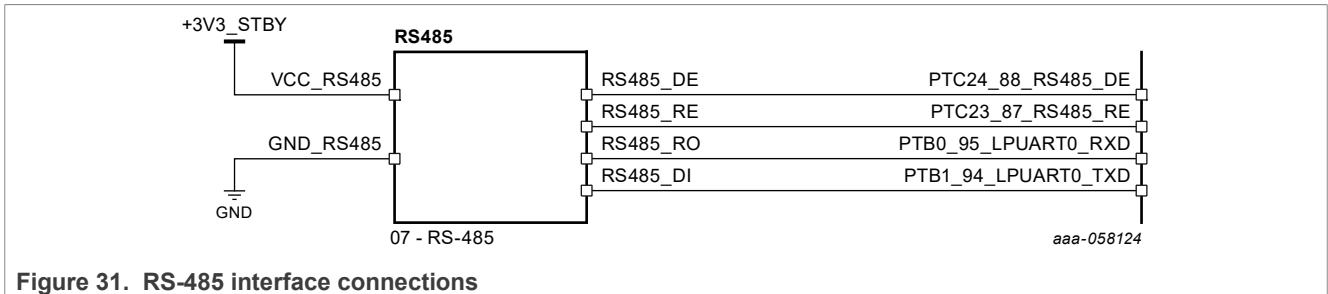


Figure 31. RS-485 interface connections

5.2.6.4 CAN interface

There is one CAN-FD capable port with an onboard transceiver available on the BMU board. The CAN interface is connected to CAN connector J12. The BMU board uses the CAN-FD interface to communicate with the MCU. The CAN-FD interface can also be used to monitor the system voltage, current and temperature, can be used to control the contactors, and enable cell balancing through the BMS monitor GUI.

The CAN controller interface is equipped with a high-speed TJA1463ATK/0Z transceiver. This transceiver supports signal improvement CAN (SIC) by means of a selective wake-up function. The transceiver inhibit pin is connected to the SBC wake2 signal, which wakes up the system when the wake-up command is received on the CAN port.

The CAN-FD transceiver is connected to the MCU through CAN 4 port and the other control pins are connected to the MCU, as per [Table 16](#).

Table 16. CAN-FD pinout assignment

Signal	Pin description	MCU port
CAN_TXD	Transmit data input; inputs data (from the CAN controller) to be written to the bus lines	PTC30
CAN_RXD	Receive data output; outputs data read from the bus lines (to the CAN controller)	PTC31
CAN_EN	Enable control input	PTD8
CAN_STBY	Standby mode control input (active low)	PTA7
CAN_ERR	Local failure detection; wake-up source recognition and power-on indication output (active low).	PTD9

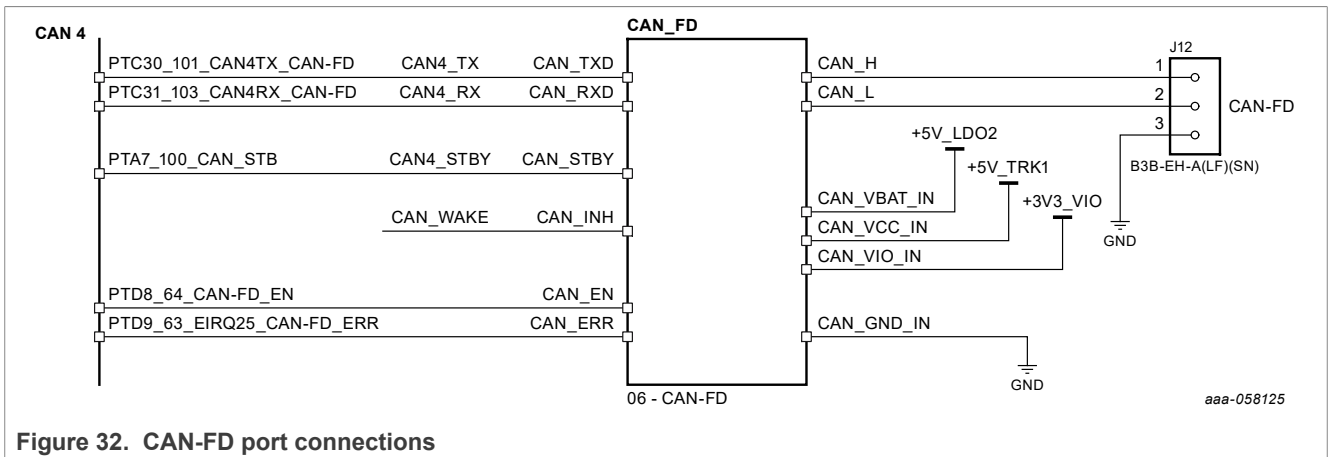


Figure 32. CAN-FD port connections

5.2.6.5 UART for GUI

A serial UART interface is available at the J8 debug header.

Note: This is directly connected to the MCU without any transceiver or protection circuit.

To communicate with the PC, the TTL-to-USB converter should be used (for example, FTDI TTL-232R-3V3). The port is intended for communication with the GUI or to use for terminal output. [Figure 33](#) shows the correct connection of the USB to UART adapter and [Table 17](#) shows connection of signals.

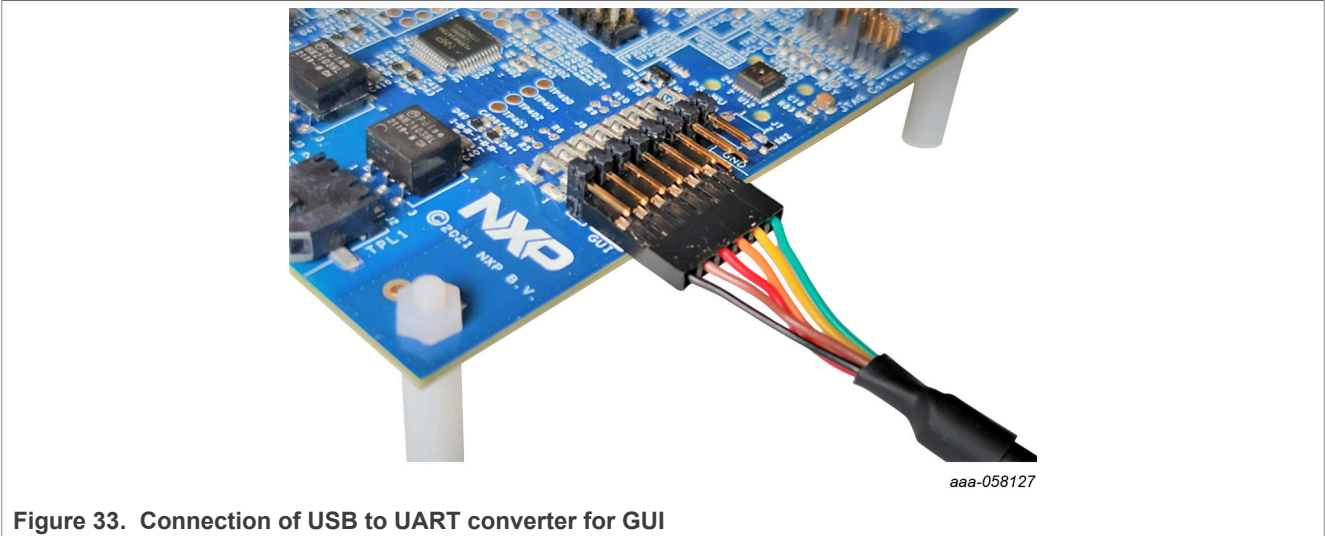


Table 17. Serial interface pinout

Signal	Pin	MCU port
GND	J8.1	—
UART_RX	J8.7	PTA19
UART_TX	J8.9	PTA18

5.2.6.6 Onboard SPI

There are seven SPI nodes on this BMU board. Assignment of peripheral chip select (PCS) and SPI instances are shown in [Table 18](#).

Table 18. Onboard SPI nodes

Node name	IC reference	SPI instance	Peripheral chip selects	Max CLK speed [MHz]
SBC (FS2633D)	U43	LPSPi0	PCS0	10
TPL Response	U400	LPSPi1	PCS3	10
TPL Request	U400	LPSPi2	PCS0	10
Load drivers	U40	LPSPi3	PCS1	10
HB2000 Contactor drivers	U301, U303	LPSPi4	PCS0, PCS1	10
External Flash Memory	U403	LPSPi5	PCS0	166

5.2.6.7 I2C interfaces

There are I2C nodes on this BMU board. Assignment of the I2C ports and device addresses are shown in [Table 19](#).

Table 19. I2C nodes

Node name	IC reference	I2C Port	Device Address	Max CLK speed [MHz]
Real-time clock (RTC)	U42	I2C0	0x53	0.4
Secure Element	U402	I2C0	0x48	3.4

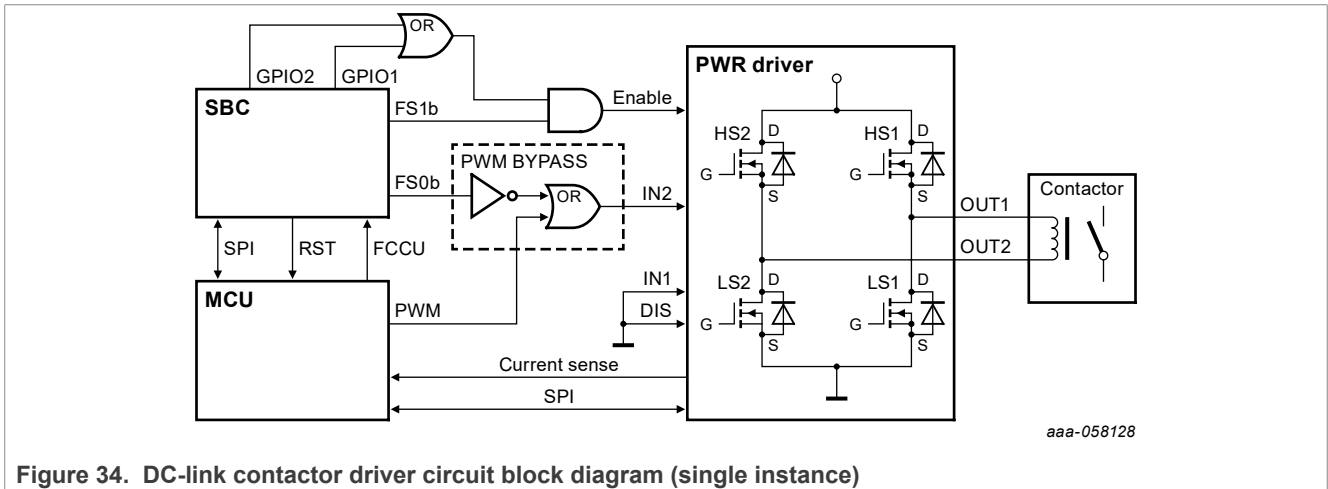
5.2.7 Auxiliary circuits

5.2.7.1 Contactor drivers

The BMU board allows the user to control two contactors (for DC-link circuit) with a maximum coil pick-up current up to 4 A for 1 s, then 0.8 A holding current per channel. The BMU also supports a DC bus capacitor precharge contactor with a maximum coil current of 1 A. The DC-link contactor circuitry implements an H-bridge driver to control the two coil terminals separately, support economizer PWM with active current recirculation, fast turn off, and high-side current monitoring. Each H-bridge driver is SPI-configurable, receives a 20 kHz PWM from the MCU's PWM generator, and sends the coil current feedback signal back to the MCU's ADC. Such a configuration enables closed-loop current control, ensuring an effective PWM economizer function for the contactors.

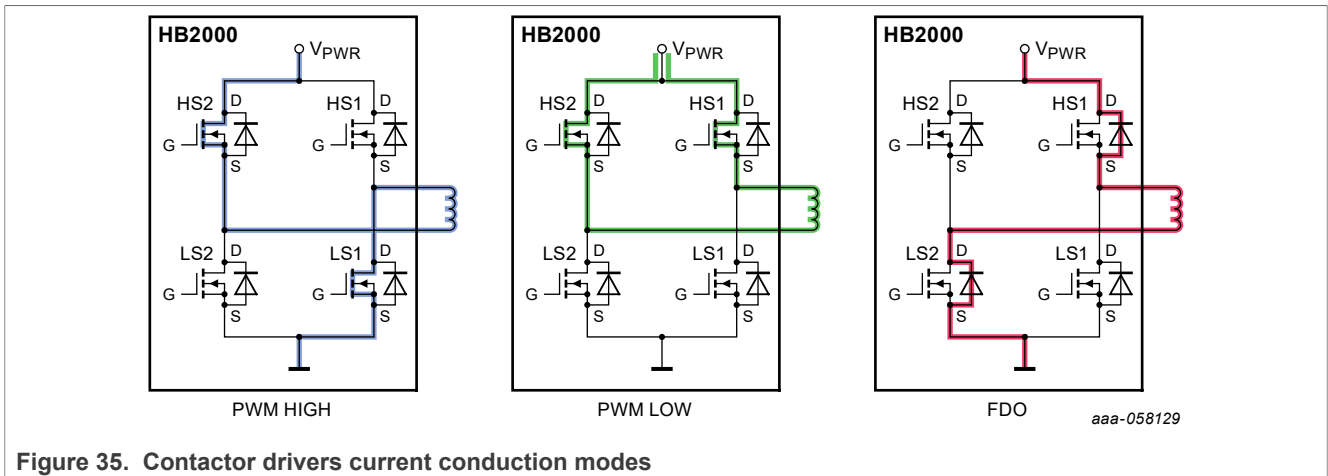
Contactors that require external economizer circuits typically have a limited amount of time to support a full 24 V supply, otherwise the coil may be damaged. To prevent overheating the coil, the duty cycle should be lowered to within a few hundred milliseconds, according to the contactor data sheet (for example, 200 ms). Always make sure that the coil current is maintained at the hold current recommended by the contactor manufacturer after the predefined duration of the pick-up pulse. This ensures reliable contactor closed state and optimal efficiency even if the input voltage is changed or the coil resistance varies with temperature.

The contactors' circuits also support fast dropoff (FDO) functionality, which ensures fast coil current decay to not limit the contactor mechanical performance when the contactor is opening. This helps to minimize contactor wearing and prevent contacts from welding during contactor operation.



DC-link contactor circuitry includes a fail operational circuit as shown in [Figure 34](#) and its control is described in sections [Contactors fail operational circuit](#) and [DC-link contactors close procedure](#).

It is intended that each contactor driver operates in three current conduction modes, depending on the driver inputs. All modes are illustrated in [Figure 35](#). Starting from the left in [Figure 35](#), the first mode is while the PWM input is in High state. In this mode, the contactor coil is connected to +24V_IN voltage through, HS2 and LS1 switches, which means the coil current is rising. After the PWM goes to Off state (middle picture), the LS1 switch is Off and HS1 is On, which leads to active current recirculation. The contactor coil current recirculates through HS2 and HS1. The contactor coil current is decreasing slowly, but due to low $R_{DS(on)}$, power losses are minimized in comparison to the conventional freewheeling approach. In case the contactor is requested to open, (see right picture) to decrease contactor coil current as soon as possible. During this mode, coil current is discharged back to the power supply through the HS1 and LS2 body diodes, causing the contactor to open quickly, known as fast dropout (FDO).



To ensure normal operation of the contactors, the SBC must be in Normal mode with proper watchdog refreshes. To enter Normal mode, see [Leave debug mode](#). Both safety outputs, FS0B and FS1B, must be released, so they must be in High state. Normal operation of the contactors in SBC Debug mode or without releasing the safety outputs is not possible.

5.2.7.1.1 Contactors fail operational circuit

The fail operational circuit ensures DC-link contactors' state can be maintained even in case of software error, MCU reset, or temporary unavailability of the MCU for a short period of time, shorter than the minimum fault detection time interval (FDTI) identified by the BMS safety analysis. The battery cannot be kept connected to a DC-link bus for longer than the FDTI if the MCU is not available.

In the event of an MCU software fault, the fault status is detected over the SPI communication between the MCU and the SBC or indicated on the pins of the fault collection and control unit (FCCU). Upon detection of the fault, the SBC asserts the FS0b pin to ground, causing PWM economizer function to be bypassed by an OR gate and the contactors to be driven with duty cycle of 100 % during the recovery period. From this moment, the SBC is taking full control over the contactors driving circuit to keep them in an unchanged state and none of the MCU pins (including PWM) can affect the contactors behavior. After asserting the FS0B, the SBC can trigger a reset on the MCU or the MCU can self-trigger a power-on reset (POR) to start the recovery phase.

Upon successful recovery within the predefined timeout (for example, 1 s), the MCU requests again for the FS0b to be released to take over the contactors' control, including the economizer functionality, without the need to open the contactors and to disconnect the battery from the DC-link bus.

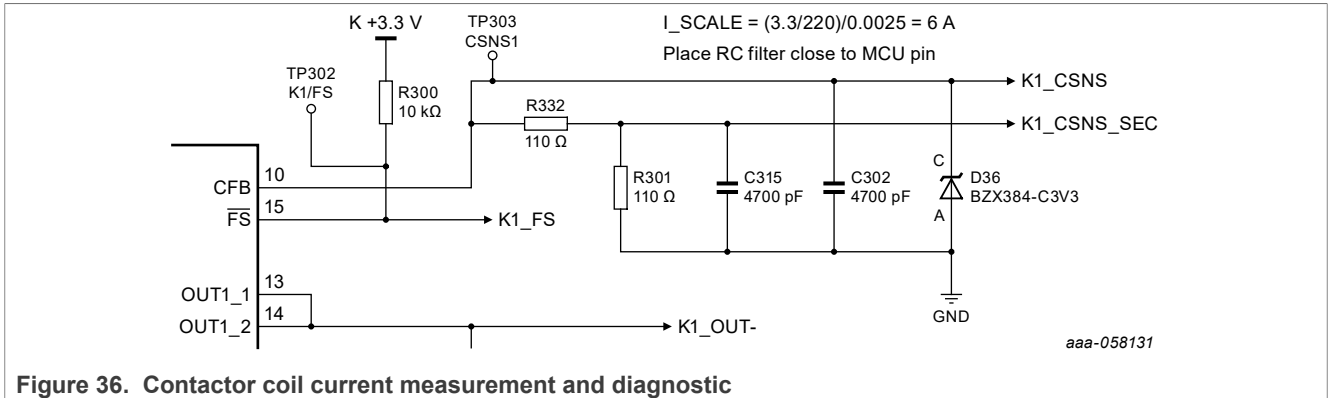
Upon unsuccessful recovery within the predefined timeout (normally equal to the shortest FDTI linked to the BMS), the SBC asserts the FS1b safety output, and leads the system to a Safe state by disabling the contactors' driving circuits and opening the DC-link contactors to disconnect the battery from the DC-link bus.

The system solution uses the SBC GPIO outputs, which act as a memory to preserve the contactor state during the MCU recovery period. The system uses two GPIO outputs together with an OR gate to prevent single-point of failure (SPF) at the SBC GPIO output. In this configuration, the contactors' driving circuit enable pin is driven by both GPIO1 and GPIO2 connected through an OR gate. The redundant GPIO configuration in the SBC improves the safe fault fraction (SFF) in the safety analysis and improves the reliability on the circuit memory.

5.2.7.1.2 Contactor coil current measurement diagnostic

For safety reasons, the contactor coil current measurement is done by two ADCs as primary and secondary measurement. To improve diagnostic coverage, the current sense resistor is divided into two resistors (R332 and R301 for K1), where one ADC measures the midpoint of the resistor divider, while the second ADC measures the total voltage drop across both resistors. The secondary measurement should always indicate half

the value of the primary measurement. If it does not, it may indicate a drift in the current sensing resistor, so the software can take appropriate action. The current measurement circuit is shown in [Figure 36](#):



The connection of the driver current feedback signals to the appropriate MCU pins is described in [Table 20](#):

Table 20. Contactor current sense channel assignment

Contactor	ADC channel	Port
K1 DC-link+ (primary ADC)	ADC2_P3	PTE21
K1 DC-link+ (secondary ADC)	ADC1_P5	PTE2
K3 DC-link - (primary ADC)	ADC2_P5	PTE23
K3 DC-link- (secondary ADC)	ADC1_P3	PTE1

5.2.7.1.3 HB2000 recommended settings

The MC33HB2000 is a monolithic H-bridge power IC, enhanced with SPI configurability and diagnostic capabilities. To ensure required functionality required for RD-K358BMU, specific register settings must be applied. Special attention should be paid to slew rate settings as HB2000 has eight selectable slew rates from 0.25 V/μs to over 16 V/μs for EMI and thermal performance optimization. Operation of HB2000 with default register settings will impact the board thermal behavior and may cause an overtemperature shutdown.

HB2000 settings depend on contactor types, required EMI performance, and other factors. [Table 21](#) shows the settings that have been used during board validation. In this configuration, the device is in H-bridge mode with fast slew rate.

Table 21. HB2000 configuration and control register example settings

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	CL	TM	AL	ILM1	ILM0	SR2	SR1	SR0	EN	MODE	Input	VIN2	VIN1
Write	1	1	1	0	1	1	0	1	0	0	1	1	1	0	0	0

5.2.7.1.4 DC-link contactors closing procedure

DC-link contactor control circuits include a fail operation circuit and an economizer circuit. Therefore, special attention must be paid to ensure proper control of the driver circuit.

Note: In Default state, the HB2000 drivers are disabled and no communication via SPI is possible with these devices.

To enable communication and to close DC-link contactors, the following sequence must be followed:

1. Make sure the SBC is in Normal mode.
2. Set the PWM to 0 % duty cycle.

3. Make sure U40 OUT #2 is active and provides the power supply for contactor drivers.
4. Release the SBC FS1B and FS0B outputs.
5. Set the SBC GPIO1 and GPIO2 pins high, to enable the contactor drivers.
6. Send the HB2000 configuration through SPI and check device status.
7. Set PWM to 100 % duty cycle.
8. Wait until the pick-up pulse is long enough to meet the contactor manufacturer's requirements.
9. Start close loop current control, to regulate current to hold the current setpoint.

5.2.7.1.5 DC-link contactor opening procedure

To open DC-link contactors, the following sequence must be followed:

1. Clear the SBC GPIO1 and GPIO2 pins to disable contactor drivers.
2. Set PWM duty cycle to 0 %.

5.2.7.2 High-voltage interlock pilot loop

The high-voltage interlock loop (HVIL) is a loop that monitors disconnection or tampering of all high-voltage components (for example, power inverter, connectors, and so on ...). This BMU board is equipped with PWM-based interlock that can detect loop interruption, loop short to ground or short to +24V_IN supply. The interlock consists of two parts: transmitter and receiver. The impedance of the correctly operating loop between transmitter and receiver shall be below 3.5 kohms.

The transmitter provides a 24 V PWM signal with a frequency of 33 Hz supplied by an internal PWM of the S32K358 MCU. The signal is protected against short to the +24V_IN supply and short to ground by a current limiting circuit. The loop current is limited to 8 mA.

The receiver scales signal amplitude and feeds PWM signal into S32K358 input capture module. The MCU can check if the period, frequency, and phase of the signal from the interlock loop are correct. Receiving a signal with the same period, frequency, and phase means the loop is closed and operates correctly. Measuring a constant high level indicates short to the +24V_IN supply, and measuring constant low level indicates short to ground or a high impedance of the interlock loop.

5.2.7.3 AMUX analog value monitoring

By using the SBC internal analog multiplexer (AMUX), the MCU has access to the SBC internal and external voltage and temperature values. The voltage channels delivered to the AMUX pin can be selected using SPI. The AMUX output is connected to MCU ADC1P1 PTA13. The AMUX can be used by the system to monitor various parameters from the FS26 and the application.

The typical use case is the VBATP supply voltage measurement. The channel selection list and divider ratios can be found in FS26 data sheet.

5.3 Board accessories

5.3.1 Included accessories

The BMU board comes with a cable harness, one ETPL cable, a 24 V/3.75 A power supply, and a USB to serial converter (see the BMU package content in [Figure 37](#)). Other cables or accessories are not part of the BMU board package. The list of recommended accessories can be found in [Table 22](#).

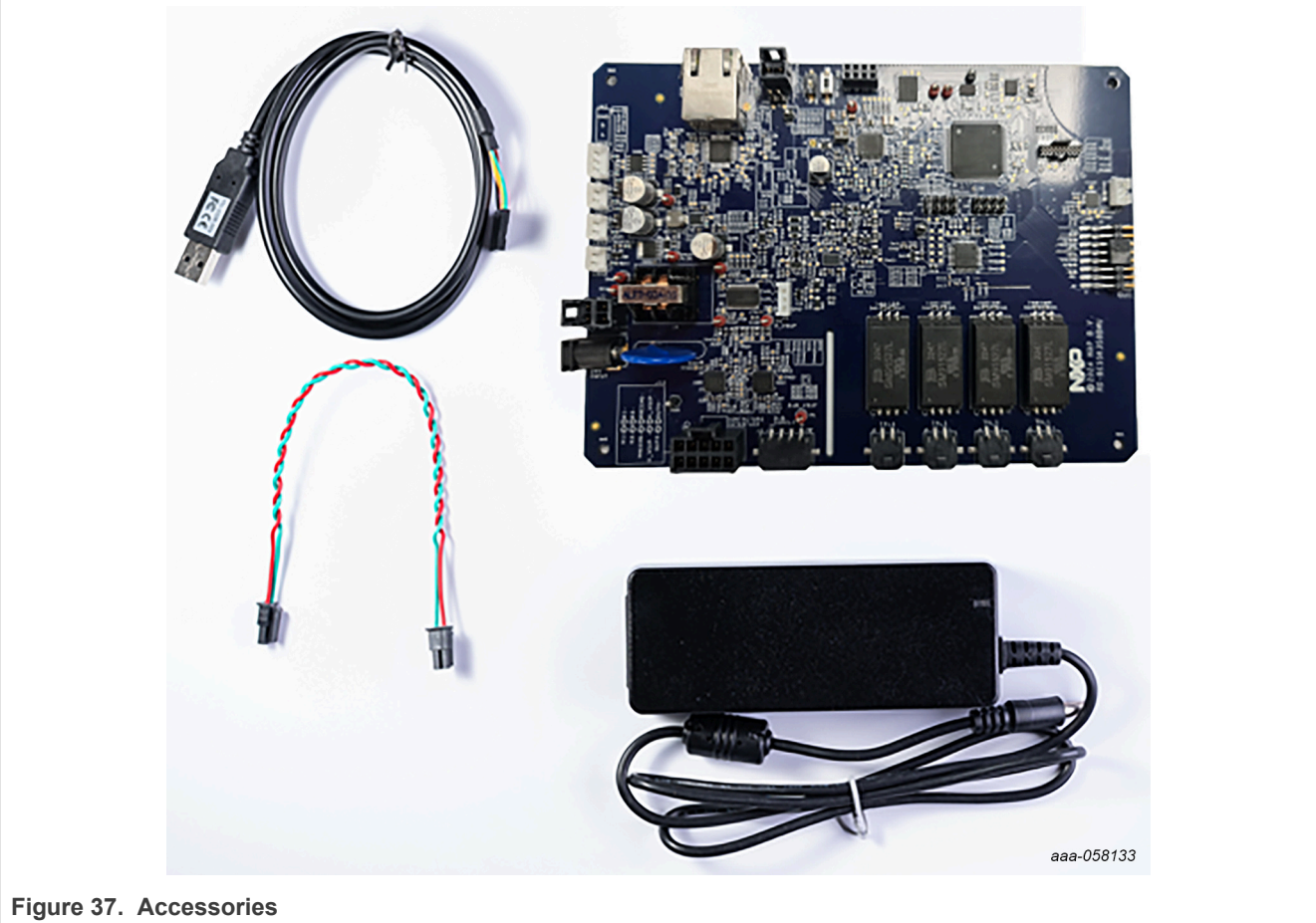




Figure 38. BMU board package content

5.3.2 Recommended accessories

To make full use of the board's features, additional accessories are needed. Figure 39 shows a typical system interconnection and Table 22 provides list of recommended accessories for the RD-K358BMU board.

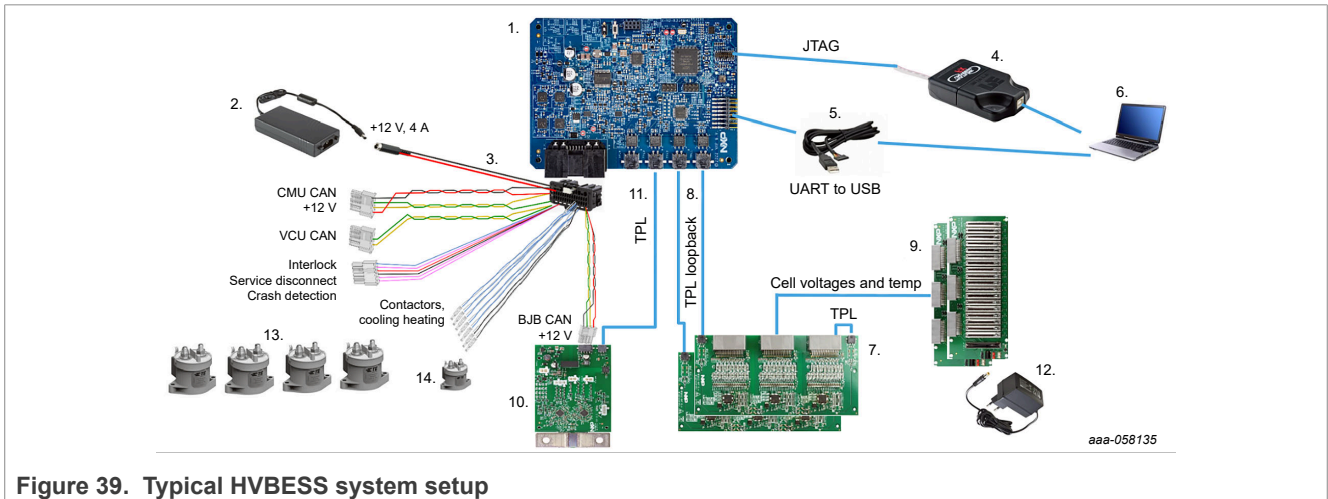


Figure 39. Typical HVBESS system setup

Table 22. Recommended accessories

Number	Name	QTY	Type	Optional/mandatory	Purpose
1	BMU board (included)	1		Mandatory	
2	Power supply (included)	1	24V DC, 3.75A	Mandatory	BMU power supply

Table 22. Recommended accessories...continued

Number	Name	QTY	Type	Optional/ mandatory	Purpose
3	Ethernet cable (included)	1	Ethernet Cable, UTP, Patch Lead, Cat6, RJ45 Plug to RJ45 Plug, Blue, 1 m included in the BMU package	Mandatory	Connect the BMU with the laptop to use the GUI
4	Debugger	1	PEmicro MUL TILINK or Lauterbach Power Debug	Mandatory	Flashing firmware on S32K358 MCU
5	PC	1	PC with three USB ports	Mandatory	
6	Cell monitoring unit (CMU)	1 or more	RDBESS774A3 EVB	Mandatory	Li-ion cell monitoring based on MC33774
7	CMU ETPL twisted pair cable	1	Included in CMU package	Mandatory	Communication with the CMU unit
8	18-cell battery pack emulator	1	BATT-18 CEMULATOR	Optional	Emulate a multicell battery pack
9	Battery junction box (BJB)	1	RDBESS772 BJBEVB	Optional	Current, voltage and isolation measurement
10	BJB ETPL twisted pair cable	1	Included in the BJB package	Optional	Communication with the BJB unit
11	BJB power supply cable	1	Included in the BJB package	Mandatory	To power the BJB board from the BMU
12	BJB Hall sensor cable	2	Included in the BJB package	Mandatory	
13	External NTC cable	2	Included in the BJB package	Optional	
14	Emulator power supply	1	5 V DC, 4A	Optional	BATT-18CEMULATOR supply
15	Battery contactors	2	For example: AEVT500-C	Optional	Battery terminal control
16	Precharge contactor	1	For example: AEVTS300-C	Optional	Inverter capacitor precharge

5.4 Tips and recommendations

5.4.1 Recommendation for capacitors

It is recommended to use soft termination or fail open capacitor in critical functions to improve board reliability (for example, C312).

5.4.2 Vmonext usage

Vmonext is the signal for internal/external voltage monitoring. In the current schematic, this signal monitors TRK2 output to increase the diagnostic coverage. However, monitoring this signal is not required by the safety analysis. Therefore, customers can use the Vmonext signal for other purposes as required by the final application.

If the signal is not being used, make sure this functionality is disabled in FS2633 OTP configuration, or make sure Vmontext is supplied with a 0.8 V (for example, use voltage divider from Vcore). A wrong Vmonext voltage will cause FS2633 to assert MCU reset low, and the system will not be able to start.

5.4.3 JTAG adapters

The BMU board is equipped with a small 20-pin 1.27 mm ARM Cortex Debug + ETM connector (Samtec FTSH-110) (see [Section 5.2.5.3](#) for details). Various debug probes come with a different set of connectors and adapters, therefore it is important to check whether the debug probe is compatible with the BMU JTAG interface. If this is not the case, the appropriate adapter for the probe is necessary. There are several adapters available in the market. Select appropriate adapters according the debug probe type. Here are some examples:

1. Lauterbach [LA-3770](#) - Converter Arm-20 to MIPI-10/20/34
2. JTAG_SWD_Adapter - Cyclone MAX Adapter for ARM processors
3. 8.06.00 J-LINK 19PIN CMADAPTER

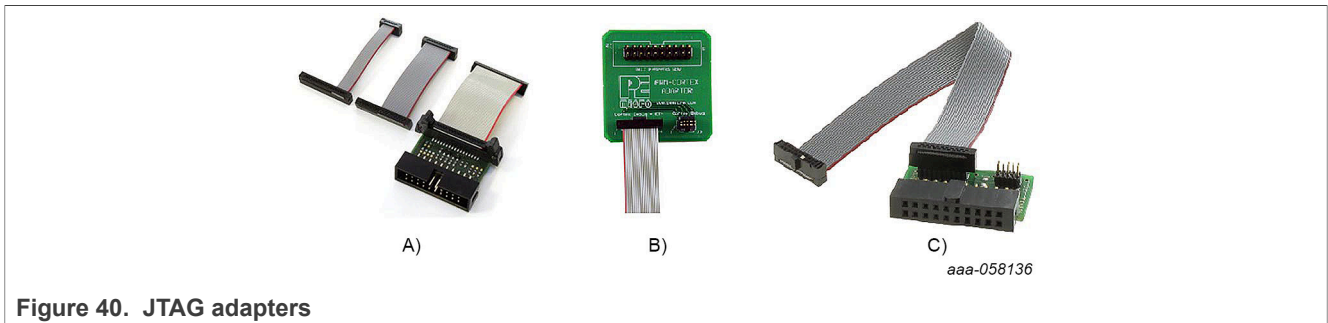


Figure 40. JTAG adapters

5.5 MCU pinout

[Table 23](#) shows the S32K358 MAXQFP172 pinout and signal distribution for the BMU.

Table 23. Signal distribution across MCU package

S32K358_172mqfp	Pin name	Functionality required	Purpose in BESS ref design	Pin type
1	PTA18	LPUART1_TX	FMSTR_UART_TX	UART
2	PTA19	LPUART1_RX	FMSTR_UART_RX	UART
3	PTA20	TRGMUX_IN14	PWM_IL_IN	IN/PWM
4	PTE16	LPSP12_SIN	MC33665_RSP_SIN	SPI
5	PTE15	LPSP12_SCK	LPSP12SCK_MC33665_REQ	SPI
6	PTA21	GPIO_PTA21	LED_RED	OUT
7	PTD1	LPSP13_SCK	GTP3	BI
8	PTD0	LPSP13_SOUT	GTP4	BI
9	PTE11	LPSP12_PCS0	LPSP12PCS0_MC33665_REQ	SPI
10	PTE10	LPSP13_SIN	GTP5	BI
11	PTE13	GPIO_PTE13	LED_RED_1	OUT
12	PTE5	GPIO_PT5	RTC_TS1	OUT
13	PTE4	LPSP10_PCS0	LPSP10PCS0_SBC	SPI
14	PTA24	GPIO_PTA24	GTP2	DBG
15	PTA25	OSC32K_EXTAL	OSC32K	CLK
16	VREFH	PWR		PWR

Table 23. Signal distribution across MCU package...continued

S32K358_172mqfp	Pin name	Functionality required	Purpose in BESS ref design	Pin type
17	VREFL	PWR		PWR
18	VDD_HV_A	PWR		PWR
19	V25	PWR		PWR
20	V15	PWR		PWR
21	V11	PWR		PWR
22	VSS	PWR		PWR
23	EXTAL	EXTAL		CLK
24	VSS	VSS		PWR
25	XTAL	XTAL		CLK
26	VSS_DCDC			PWR
27	PMOS_CTRL			PWR
28	VDD_DCDC			PWR
29	PTE12	GPIO_PTE12 + IRQ11	SBC INTB	IN
30	PTA28	eMIOS_1_CH[11]_H	K3_PWM_FB	IN/PWM
31	PTD17	LPSP13_PCS0	GTP6	BI
32	PTA29	GPIO_PTA29	FS1B	IN
33	PTA30	LPSP10_SOUT	LPSP10SOUT_SBC	SPI
34	PTD16	LPSP10_SIN	LPSP10_SIN_SBC	SPI
35	PTD15	LPSP10_SCK	LPSP10_SCK_SBC	SPI
36	V15	PWR		PWR
37	VSS	PWR		PWR
38	VDD_HV_B	PWR		PWR
39	PTA31	GPIO_PTA31	GTP1	BI
40	PTD14	LPSP15_SCK	LPSP15SCK_FLASH	SPI
41	PTD13	LPSP15_SIN	LPSP15SIN_FLASH	SPI
42	PTB18	eMIOS_1_CH[15]_H	K1_PWM_FB	IN/PWM
43	PTB19	-	-	NC
44	PTB20	-	-	NC
45	PTB21	GPIO_PTB21 + IRQ	FS0B	IN
46	PTE8	LPSP15_PCS1	GTP10	BI
47	PTB5	RGMII_MDC	RGMII_MDC	GMAC
48	PTB4	RGMII_MDIO	RGMII_MDIO	GMAC
49	PTC3	GPIO_PTC3	ETH_INT	IN
50	PTC2	-	-	NC
51	PTD7	-	-	NC
52	PTD6	GPIO_PTD6	SE_RST	OUT
53	PTD5	GPIO_PTD5	FLASH_RST	OUT
54	PTD12	-	-	NC
55	PTD11	-	-	NC
56	PTD10	TP8 CLK_RUN	TP8	CLK

Table 23. Signal distribution across MCU package...continued

S32K358_172mqfp	Pin name	Functionality required	Purpose in BESS ref design	Pin type
57	VDD_HV_B	PWR		PWR
58	VSS	PWR		PWR
59	V11	PWR		PWR
60	V15	PWR		PWR
61	PTC1	GPIO_PTC1	ETH_RST	OUT
62	PTC0	GPIO_PTC0	FLASH_WP	OUT
63	PTD9	PTD9_63_EIRQ25	CAN-FD_ERR	IN
64	PTD8	GPIO_PTD8	CAN-FD_EN	OUT
65	PTC17	-	-	NC
66	PTC16	RGMII_RX_CLK	RGMII_RX_CLK	GMAC
67	PTB22	RGMII_RXCTL	RGMII_RXCTL	GMAC
68	PTC15	RGMII_RXD3	RGMII_RXD3	GMAC
69	PTB23	RGMII_RXD2	RGMII_RXD2	GMAC
70	PTB24	RGMII_RXD1	RGMII_RXD1	GMAC
71	PTC14	RGMII_RXD0	RGMII_RXD0	GMAC
72	PTB25	RGMII_TXCTL	RGMII_TXCTL	GMAC
73	PTB26	eMIOS_1_ch22	K1_PWM	OUT/PWM
74	PTB3	RGMII_TXD3	RGMII_TXD3	GMAC
75	PTB27	LPSPi2_SOUT	MC33665_REQ_SOUT	SPI
76	PTB28	RGMII_TXD2	RGMII_TXD2	GMAC
77	VDD_HV_B	PWR	-	PWR
78	VSS	PWR	-	PWR
79	V15	PWR	-	PWR
80	PTB29	RGMII_TXD0	RGMII_TXD0	GMAC
81	PTC13	GPIO_PTC13	K1_FDO	OUT
82	PTC18	RGMII_TXD1	RGMII_TXD1	GMAC
83	PTC12	GPIO_PTC12	K3_FDO	OUT
84	PTC19	RGMII_TX_CLK	RGMII_TX_CLK	GMAC
85	PTC20	eMIOS_2_ch13	K3_PWM	OUT/PWM
86	PTC21	GPIO_PTC21	LED_GRN	OUT
87	PTC23	-	-	NC
88	PTC24	-	-	NC
89	PTC25	LPSPi4_PCS1	LPSPi4PCS1_K3	SPI
90	PTC11	LPSPi4_SOUT	LPSPi4SOUT_K	SPI
91	PTC26	LPSPi4_SIN	LPSPi4SIN_K	SPI
92	PTC10	LPSPi4_PCS0	LPSPi4PCS0_K1	SPI
93	PTC27	LPSPi4_SCK	LPSPi4SCK_K	SPI
94	PTB1	LPUART0_TXD	RS-485_UART_TX	UART
95	PTB0	LPUART0_RXD	RS-485_UART_RX	UART
96	PTC28	I2C1_SCL	MC33665_GPIO4	DBG

Table 23. Signal distribution across MCU package...continued

S32K358_172mqfp	Pin name	Functionality required	Purpose in BESS ref design	Pin type
97	PTC9	I2C0_SDA	SDA_RTC_SE	I2C
98	PTC8	I2C0_SCL	SCL_RTC_SE	I2C
99	PTC29	I2C1_SDA	MC33665_GPIO5	DBG
100	PTA7	GPIO_PTA6	CAN_STB	OUT
101	PTC30	CAN4_TX	CAN_TX	CAN
102	PTA6	LPSPi3_PCS1	LPSPi3PCS1_LOADSW	SPI
103	PTC31	CAN4_RX	CAN_RX	CAN
104	PTE7	LPSPi3_SCK	LPSPi3SCK_LOADSW	SPI
105	V15	PWR	-	PWR
106	V11	PWR	-	PWR
107	VSS	PWR	-	PWR
108	VDD_HV_A	PWR	-	PWR
109	PTA17	LPSPi3_SOUT	LPSPi3SOUT_LOADSW	SPI
110	PTB17	LPSPi1_PCS3	LPSPi1PCS3_MC33665_RSP	SPI
111	PTD20	LPSPi3_SIN	LPSPi3SIN_LOADSW	SPI
112	PTB16	LPSPi1_SOUT	LPSPi1SOUT_MC33665_RSP	SPI
113	PTB15	LPSPi1_SIN	LPSPi1SIN_MC33665_RSP	SPI
114	PTB14	LPSPi1_SCK	LPSPi1SCK_MC33665_RSP	SPI
115	PTD21	GPIO_PTD21	LOADSW_RST	OUT
116	PTB13	eMIOS_0_ch1	PWM_IL_OUT	OUT/PWM
117	PTB12	GPIO_PTB12	K3_FS	IN
118	PTD22	GPIO_PTD22_EIRQ27	MC33665_GPIO1	BI
119	PTD4	GPIO_PTD4	MC33665_RST	OUT
120	PTD3	NMI	NMI	IN
121	PTD2	LPSPi5_SOUT	LPSPi5SOUT_FLASH	SPI
122	PTD23	GPIO_PTD23_EIRQ28	MC33665_GPIO0	BI
123	PTA3	FCCU_ERR_IN1	FCCU_IN2	OUT/FCCU
124	PTA2	FCCU_ERR_IN0	FCCU_IN1	OUT/FCCU
125	PTD24	GPIO_PTD24_EIRQ29	MC33665_GPIO6	BI
126	PTB11	GPIO_PTB11_EIRQ25	MC33665_GPIO7	BI
127	VSS	PWR	-	PWR
128	VDD_HV_A	PWR	-	PWR
129	PTB10	-	-	NC
130	PTB9	CMP2_IN2	GTP13	BI
131	PTD26	LPSPi5_SCK	GTP7	BI
132	PTD27	LPSPi5_SOUT	GTP8	BI
133	PTB8	-	-	NC
134	PTD28	LPSPi5_SIN	GTP9	BI
135	PTA1	ADC0_S9	TPL_PWR_SENS	IN/ANA
136	PTD29	GPIO_PTD29	LED_1	OUT

Table 23. Signal distribution across MCU package...continued

S32K358_172mqfp	Pin name	Functionality required	Purpose in BESS ref design	Pin type
137	PTA0	ADC0_S8	TEMP_SENS	IN/ANA
138	PTD30	GPIO_PTD30	LED_2	OUT
139	PTD31	GPIO_PTD31	LED_3	OUT
140	PTC7	LPI2C1_SCL	GTP11	BI
141	PTC6	LPI2C1_SDA	GTP12	BI
142	PTE17	-	-	NC
143	PTA16	ADC1_S13	+24V_SENS	SPI
144	PTE18	GPIO_PTE18	LOADSW_LHM	OUT
145	PTA15	LPSPi5_PCS0	LPSPi5PCS0_FLASH	SPI
146	PTE6	GPIO_PTE6_EIRQ6	LOADSW_Fault	IN
147	PTE2	ADC1_P5	K1_CSNS_SEC	IN/ANA
148	V15	PWR	-	PWR
149	V11	PWR	-	PWR
150	VSS	PWR	-	PWR
151	VDD_HV_A	PWR	-	PWR
152	PTA14	-	-	NC
153	PTE21	ADC2_P3	K1_CSNS	IN/ANA
154	PTE22	GPIO_PTE22	LOADSW_IN1	OUT
155	PTA13	ADC1_P1	SBC_AMUX_IN	IN/ANA
156	PTE23	ADC2_P5	K3_CSNS	IN/ANA
157	PTE24	GPIO_PTE24	LOADSW_IN2	OUT
158	PTE25	GPIO_PTE25	LOADSW_IN3	OUT
159	PTA12	GPIO_PTA12	K1_FS	IN
160	PTA11	GPIO_PTA11	RTC_INTA	IN
161	PTA10	JTAG_TDO / TRACE _{no} ETM_SWO	JTAG / Trace	DBG
162	PTE1	ADC1_P3	K3_CSNS_SEC	IN/ANA
163	PTE0	GPIO_PTE0	MC33665_AUTOWAKE	DBG
164	PTE26	GPIO_PTE22	LOADSW_IN4	OUT
165	PTC5	JTAG_TDI	JTAG	DBG
166	PTC4	JTAG_TCK / SWD_CLK	JTAG/SWD	DBG
167	PTA5	Reset_b	Reset	BI
168	VSS	PWR	-	PWR
169	VDD_HV_A	PWR	-	PWR
170	PTA4	JTAG_TMS / SWD_DIO	JTAG/SWD	DBG
171	PTA9	GPIO PTA9 IRQ17	MC33665_GPIO3	DBG
172	PTA8	GPIO PTA8 IRQ16	MC33665_GPIO2	DBG

6 Revision history

Table 24. Revision history

Document ID	Release date	Description
UM12196 v.1.0	10 December 2024	Initial version

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