

NOTES (UNLESS OTHERWISE SPECIFIED):

- THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).
- THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
- BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98
 T_g - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
 T_d - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
- COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
- CHARACTERISTIC IMPEDANCE - SEE TABLE 'B'
- MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .008"/.005"
- PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
 .05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER
 2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.

- ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.
- SOLDERMASK - GREEN COLOR (TAIYO OR EQUIVALENT), BOTH SIDES.
 MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE.
- SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.

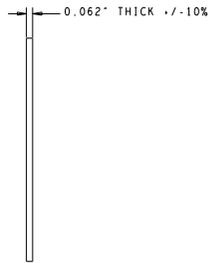
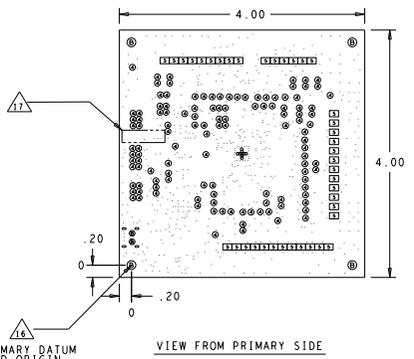
- ELECTRICAL TEST - 100% IPCD356.
- PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
- DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS.
 UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.
- ADD TEARDROPS TO ALL SIGNAL LAYERS.
- 2 SOLDER SAMPLES TO BE PROVIDED.

- BASIC GRID INCREMENT AT 1:1 IS .0001.
- SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
 MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

- THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (P6)
- THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (E60P)
- ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.
 ALL HOLE LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM.
- FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURING REQUIREMENT.
 ADDITION OF .25" RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER AND FAB HOUSE.
 PANELIZATION MUST BE APPROVED BY FREESCALE.

- THIS BOARD USES VIA-IN-PAD:
 A. VIA-IN-PAD TO BE FILLED WITH NON-CONDUCTIVE VIA FILL.
 LACKWERKE-PETERS PP2795 OR EQUIVALENT AND MADE PLANAR TO THE PADS.
 B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.
- THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS.
 KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES

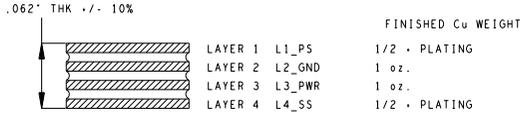
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
A		ORIGINAL RELEASE	05-17-17	L. P.



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
-	10.0	+0.0/-10.0	PLATED	630
o	10.1	+0.0/-10.0	PLATED	9
⊙	40.0	+3.0/-3.0	PLATED	121
⊗	52.0	+3.0/-3.0	PLATED	39
⊕	130.0	+3.0/-3.0	PLATED	4
⊖	36.0	+2.0/-2.0	NON-PLATED	2
-	67.0x31.0	+2.0/-2.0	PLATED	4

DETAIL B
 IMPEDANCE REQUIREMENTS
 IMPEDANCE TOLERANCE IS 10%

LAYERS	SINGLE ENDED		DIFFERENTIAL	
	TRACE WIDTH (MILS)	IMPEDANCE (OHMS)	TRACE WIDTH (MILS)	TRACE SPACING (MILS)
L1_PS	10.0	50	10.0	12.0
L3_PWR	8.0	50		
L4_SS	10.0	50	10.0	12.0



DETAIL A
 LAYER STACKUP
 SCALE: NONE

PART NO. 170-29826		NXP SEMICONDUCTORS	
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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS ANGLES .XX .XX .05 .0-30° ✓ FINISH ALL MACHINED SURFACES BREAK ALL SHARP EDGES AND CORNERS. DIMENSIONS SHOWN NOT TO SCALE. THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.		6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA TITLE: PRINTED WIRING BOARD X-KITPF4210EPEVB	
APPROVALS DRAWN: VANIPRIYA[Lnt] CHECKED: LEO_PAN DESIGN ENGINEER: OIAO_JUN		DATE: 05-17-17 DATE: 05-17-17 DATE: 05-17-17	
SIZE: <input type="checkbox"/> <input checked="" type="checkbox"/>	CAD FILE NAME: LAY-29826	DWG. NO.: FAB-29826	REV: A
SCALE: 1/1		DO NOT SCALE DRAWING	
SHEET 1		OF 1	