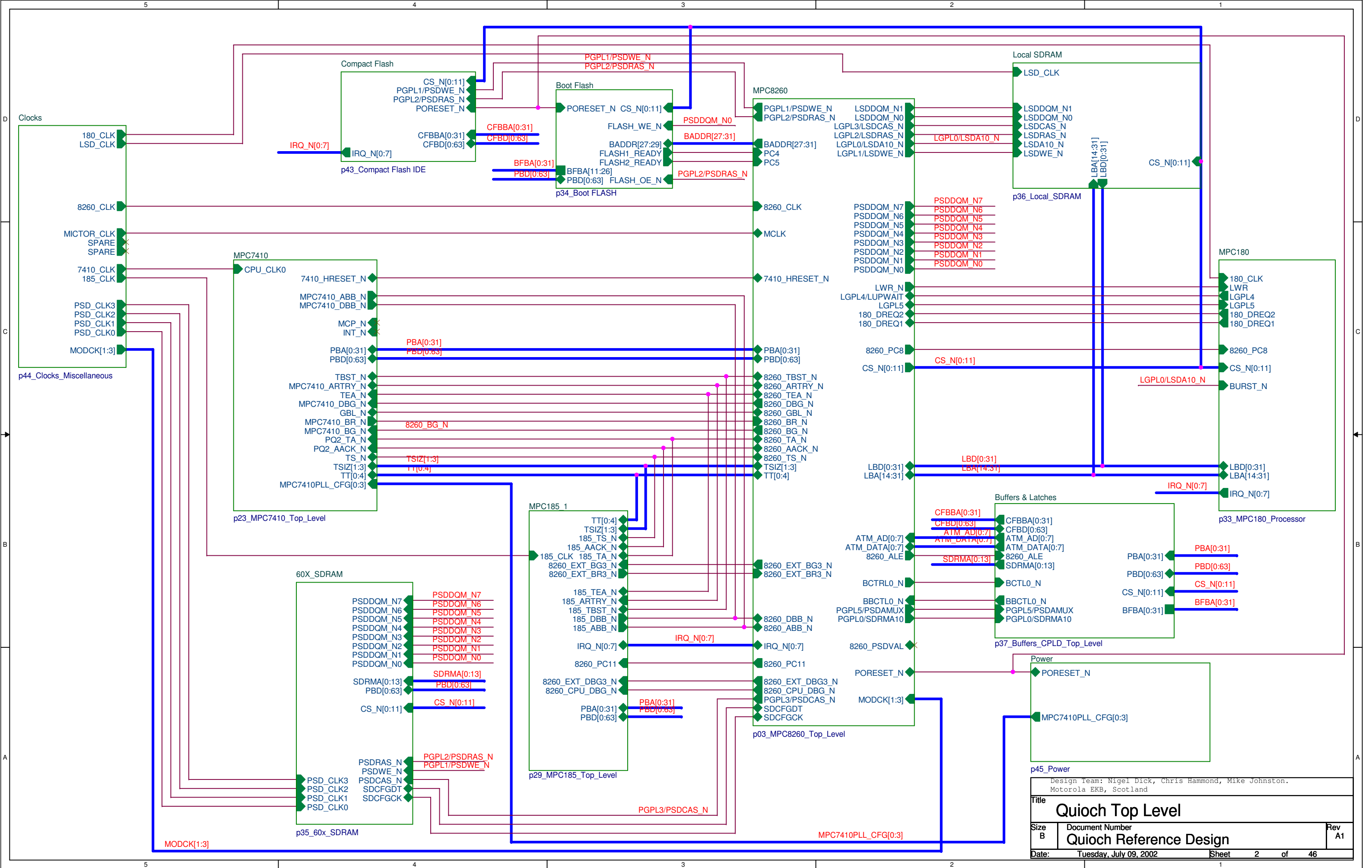


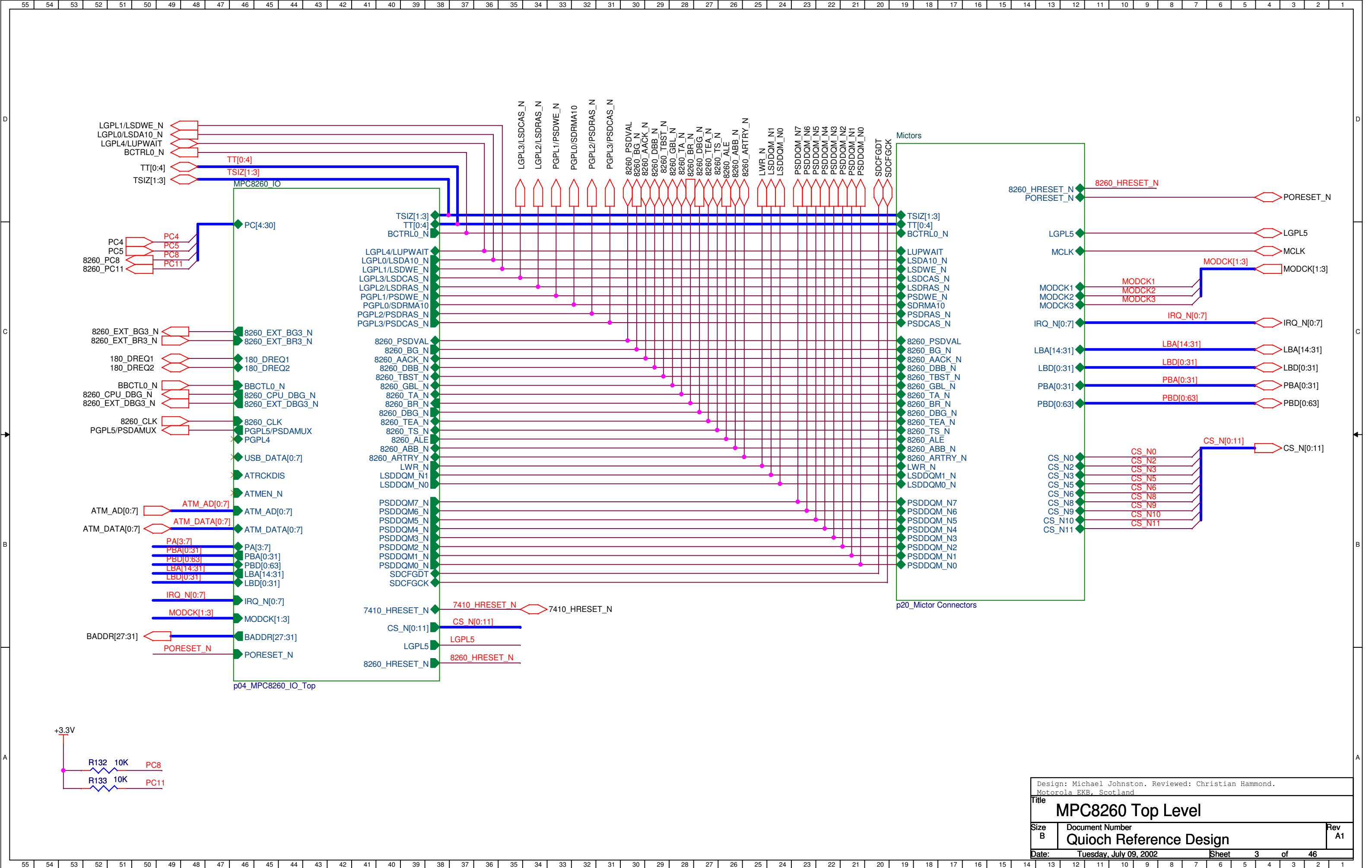
1	Quioch Design Contents List
2	Quioch Top Level Schematic
3	MPC8260 Top Level
4	MPC8260 I/O Top Level
5	MPC8260 Mid Level Hierarchy
6	MPC8260 Microprocessor
7	MPC8260 COP Configuration
8	MPC8260 Memory Config
9	MPC8260 Peripherals
10	MPC8260 60x Configuration
11	MPC8260 Power Configuration
12	Ethernet Transceiver Config
13	Ethernet Transceiver Config
14	Ethernet Transceiver Config
15	ATM 155Mbps Optical Config
16	ATM 155Mbps Optical Power
17	Ethernet RJ45 Connectors
18	FCC1 MUX Configuration
19	SMC UART Configuration
20	Bus Mictor Connectors
21	USB Configuration
22	MPC8260 IO Configuration
23	MPC7410 Top Level
24	MPC7410 Microprocessor
25	MPC7410 COP Configuration
26	MPC7410 L2 Interface
27	MPC7410 Power Configuration
28	MPC7410 L2 SRAM

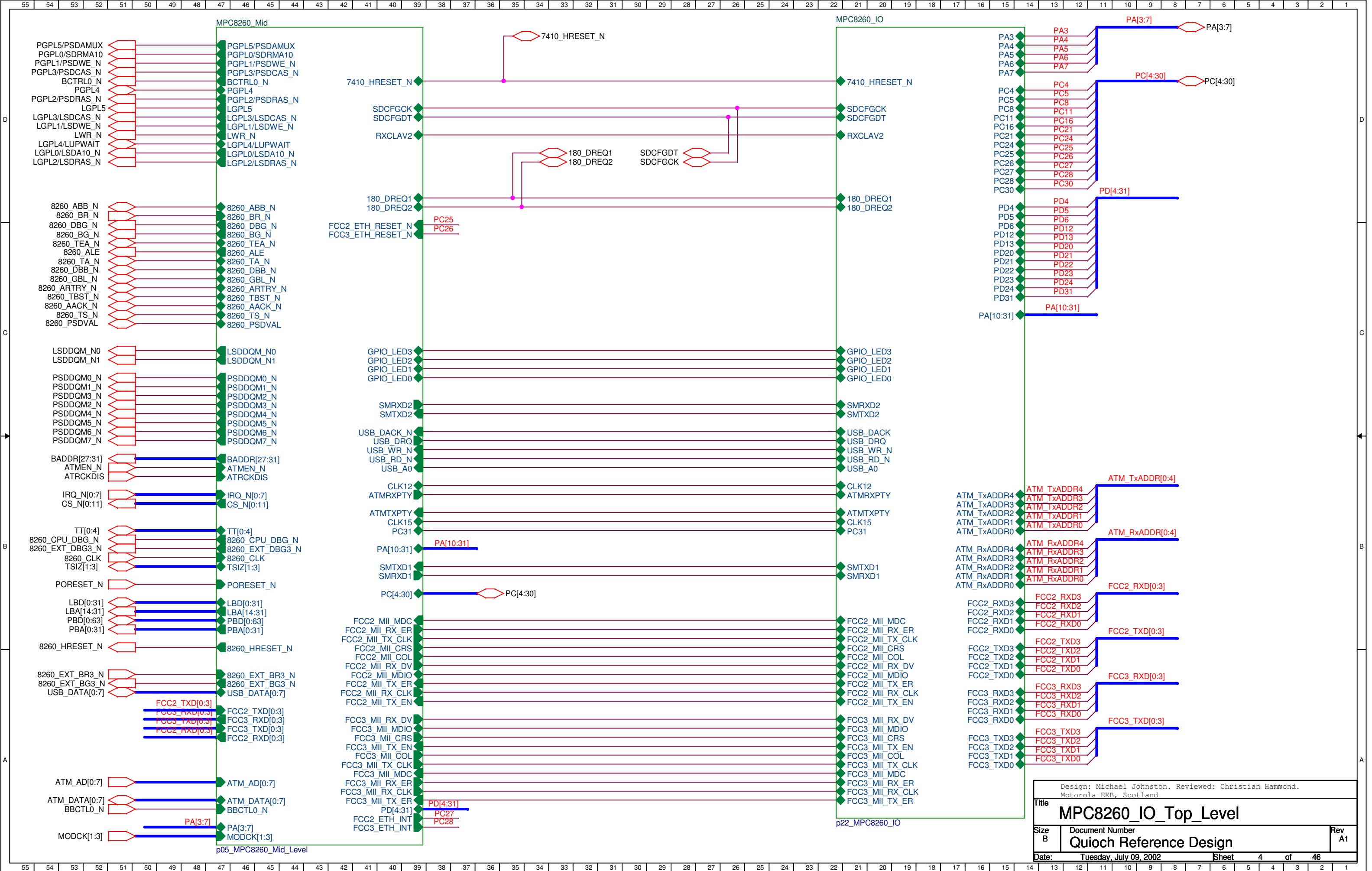
29	MPC185 Top Level Config
30	MPC185 Security Processor
31	MPC185 COP Configuration
32	MPC185 Power Configuration
33	MPC180 Security Processor
34	Boot FLASH
35	60x Bus SDRAM Configuration
36	Local Bus SDRAM Config
37	Buffers: CPLD Top Level
38	60x Latch Configuration
39	ATM Buffer Configuration
40	Compact Flash Buffer Config
41	Compact Flash Buffer Config2
42	CPLD Configuration
43	Compact FLASH IDE
44	Clock Circuitry
45	PORESET & PLL Configuration
46	Power Supply Configuration

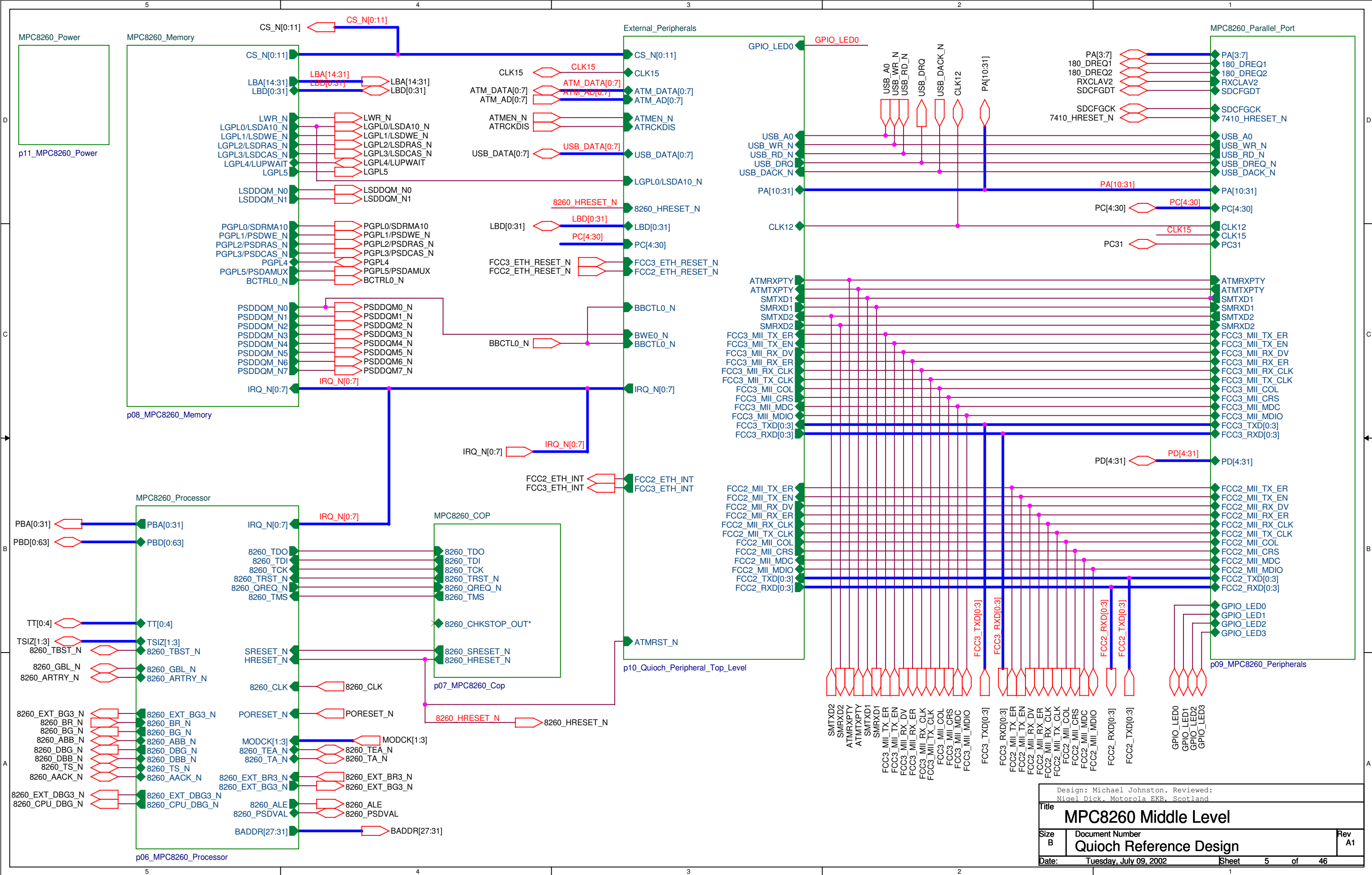
Design Team: Nigel Dick, Chris Hammond, Mike Johnston. Motorola EKB, Scotland		
Title Contents List		
Size B	Document Number Quioch Reference Design	Rev A1
Date:	Tuesday, July 09, 2002	Sheet 1 of 46

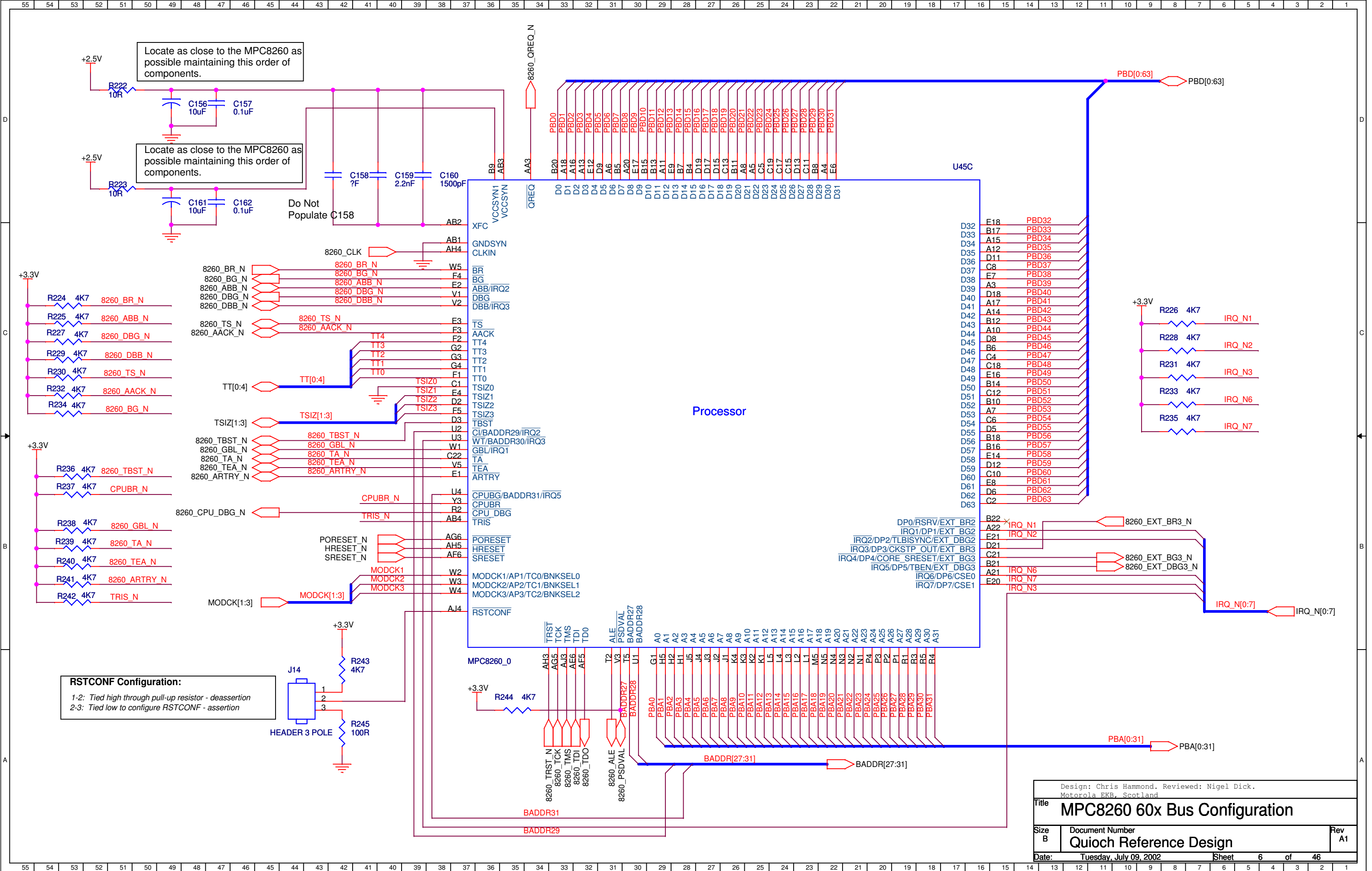


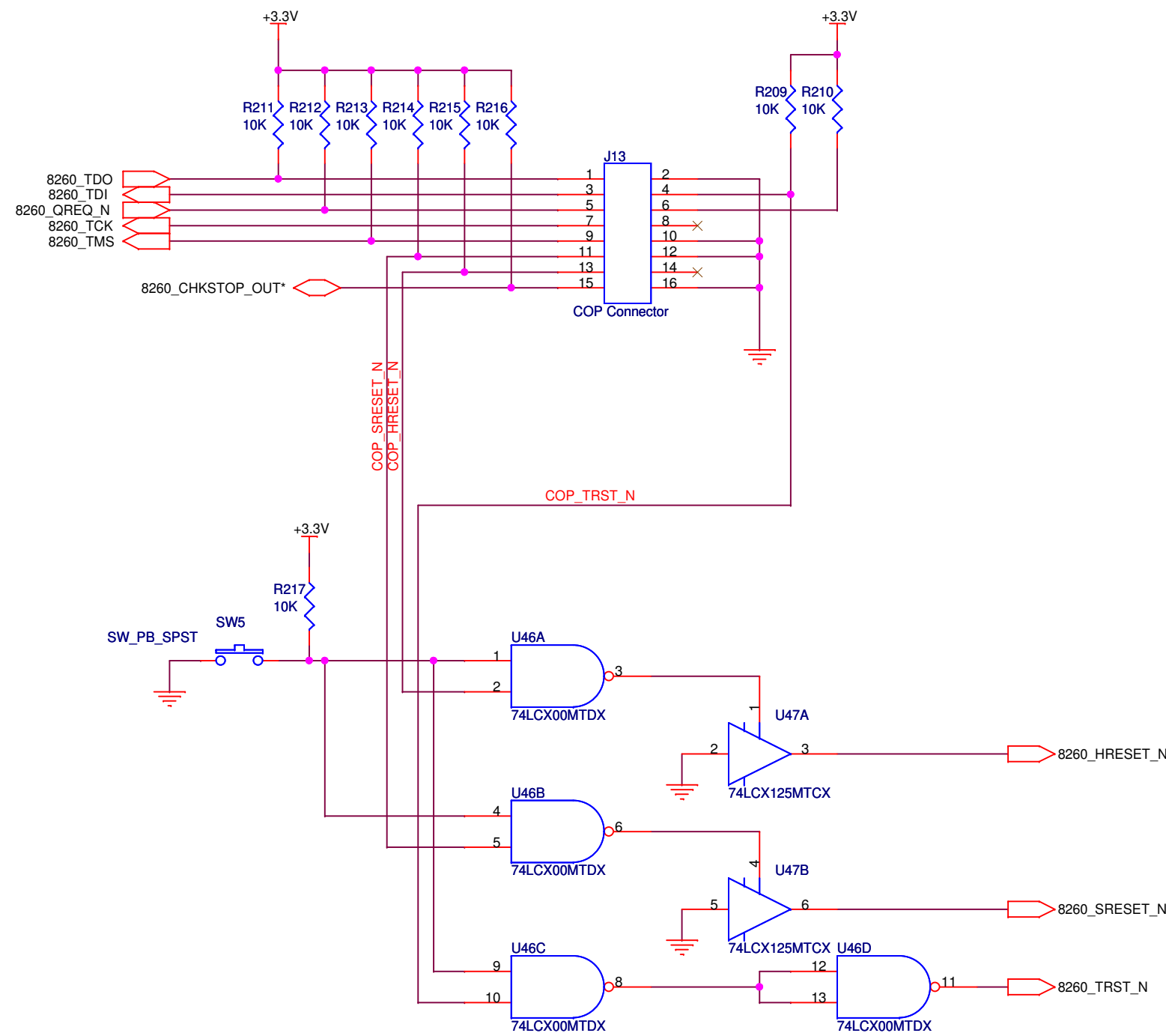
Design Team: Nigel Dick, Chris Hammond, Mike Johnston. Motorola EKB, Scotland		
Title Quioch Top Level		
Size B	Document Number Quioch Reference Design	Rev A1
Date: Tuesday, July 09, 2002	Sheet 2	of 46



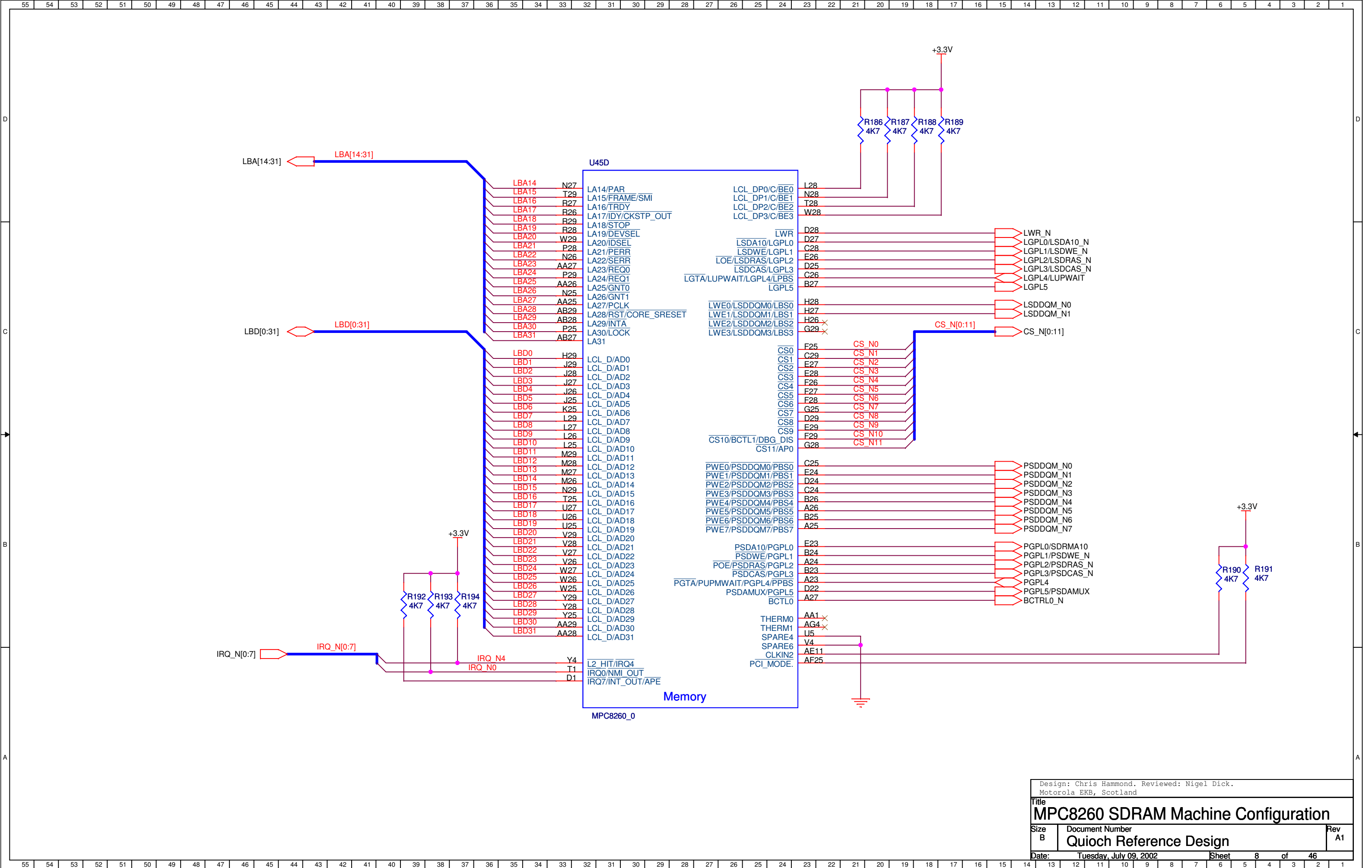


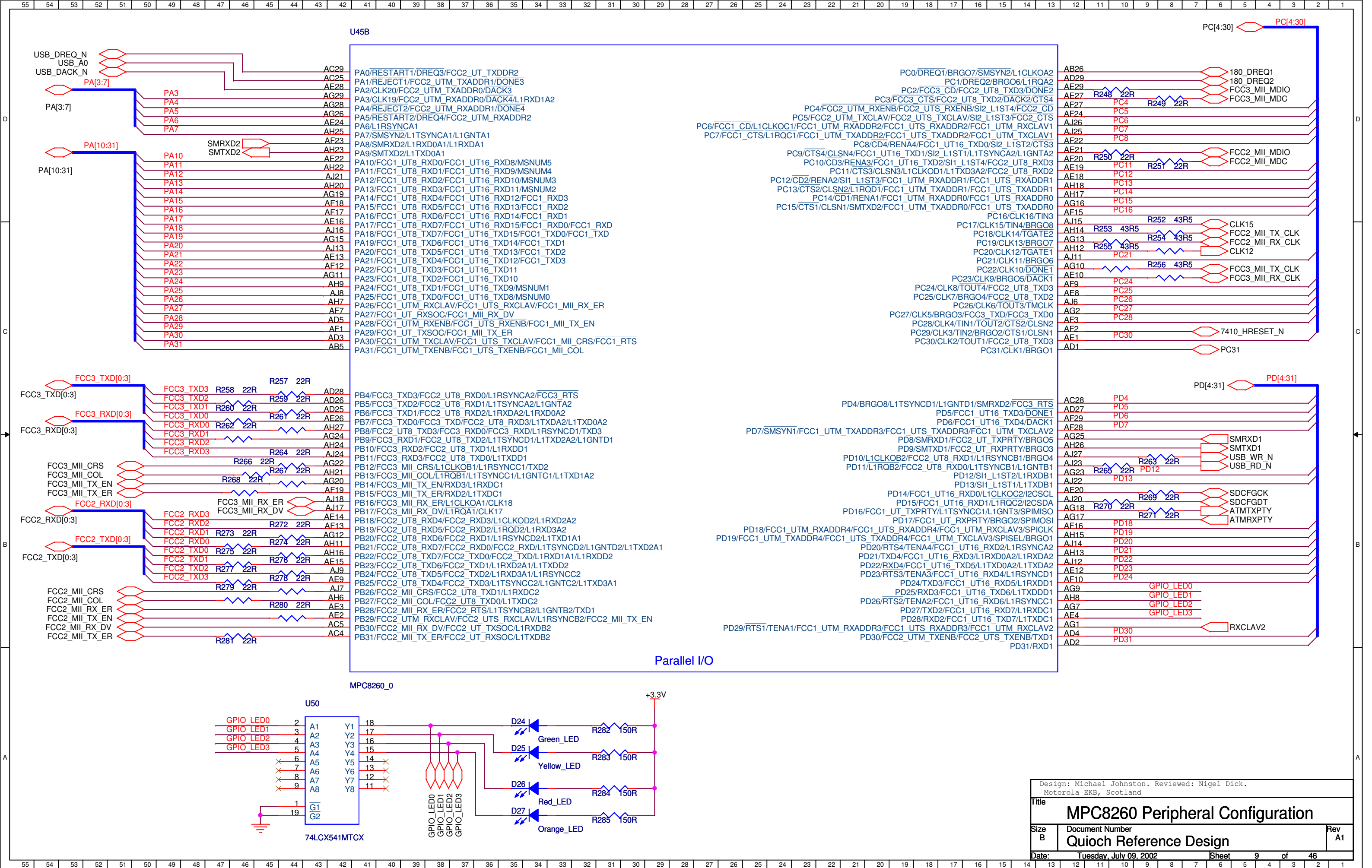


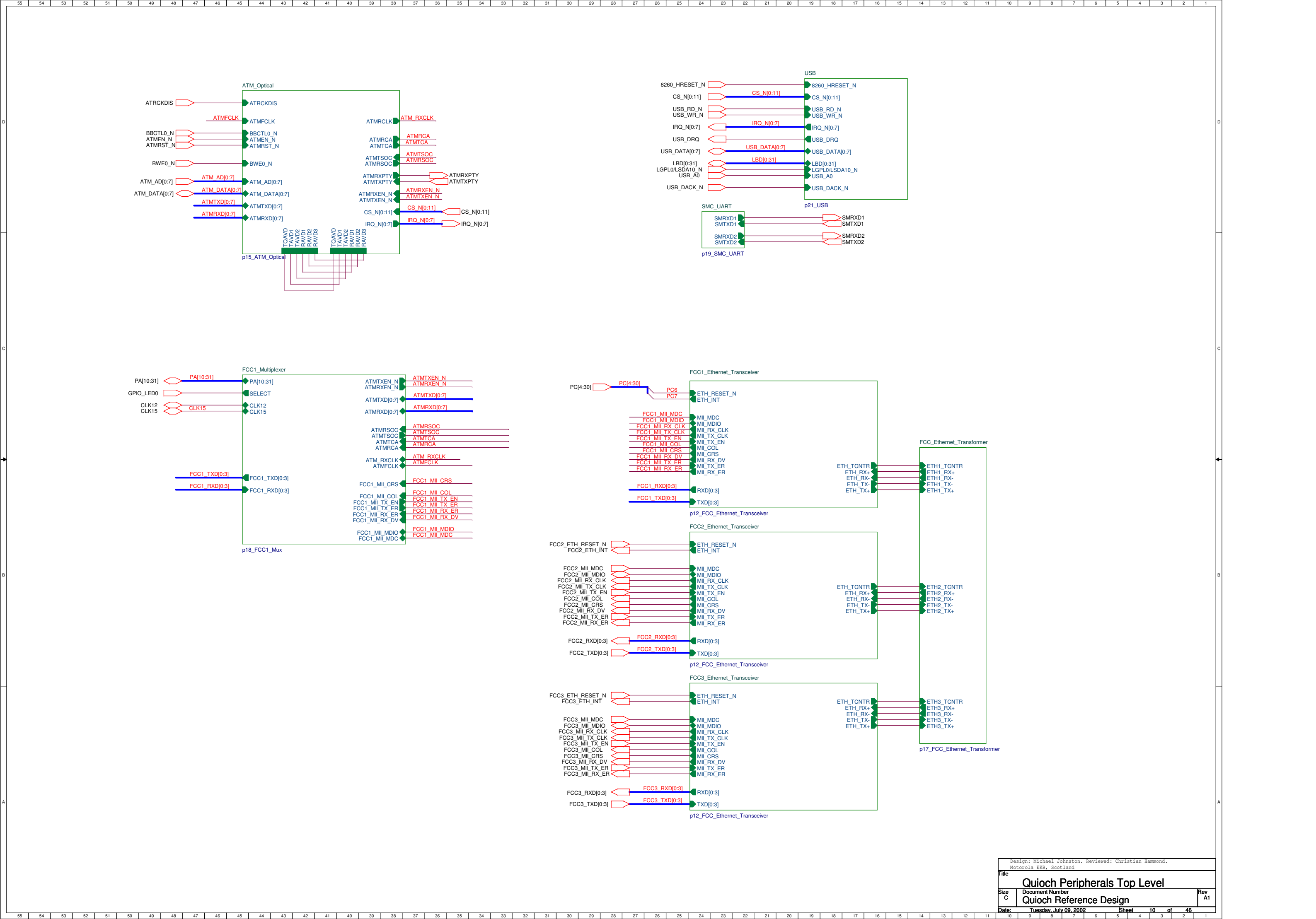


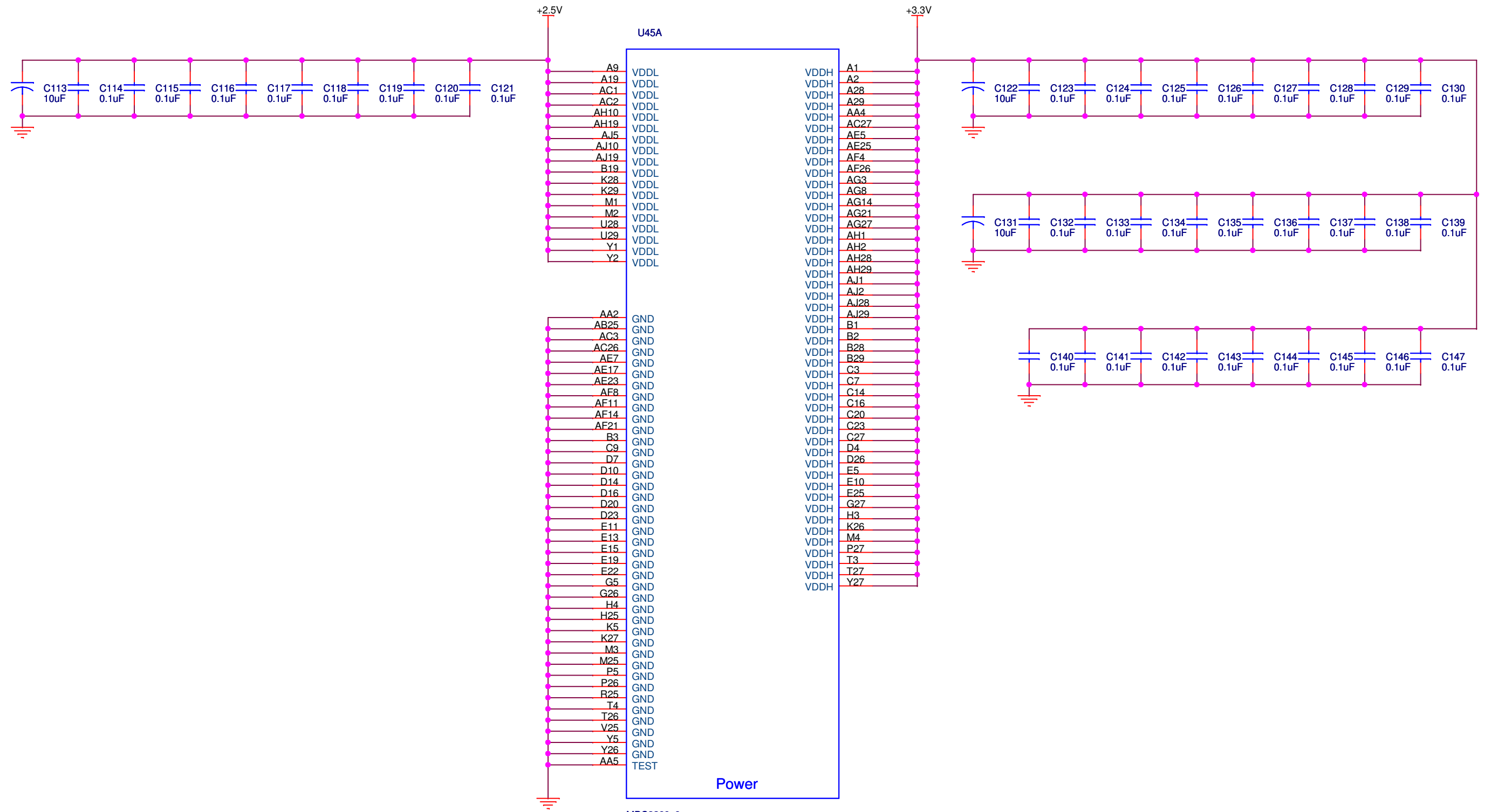


Design: Chris Hammond. Reviewed: Michael Johnston. Motorola EKB, Scotland									
Title <div>MPC8260 Cop Configuration</div>									
Size B		Document Number <div>Quioch Reference Design</div>							Rev A1
Date:		Tuesday, July 09, 2002				Sheet		7 of 46	



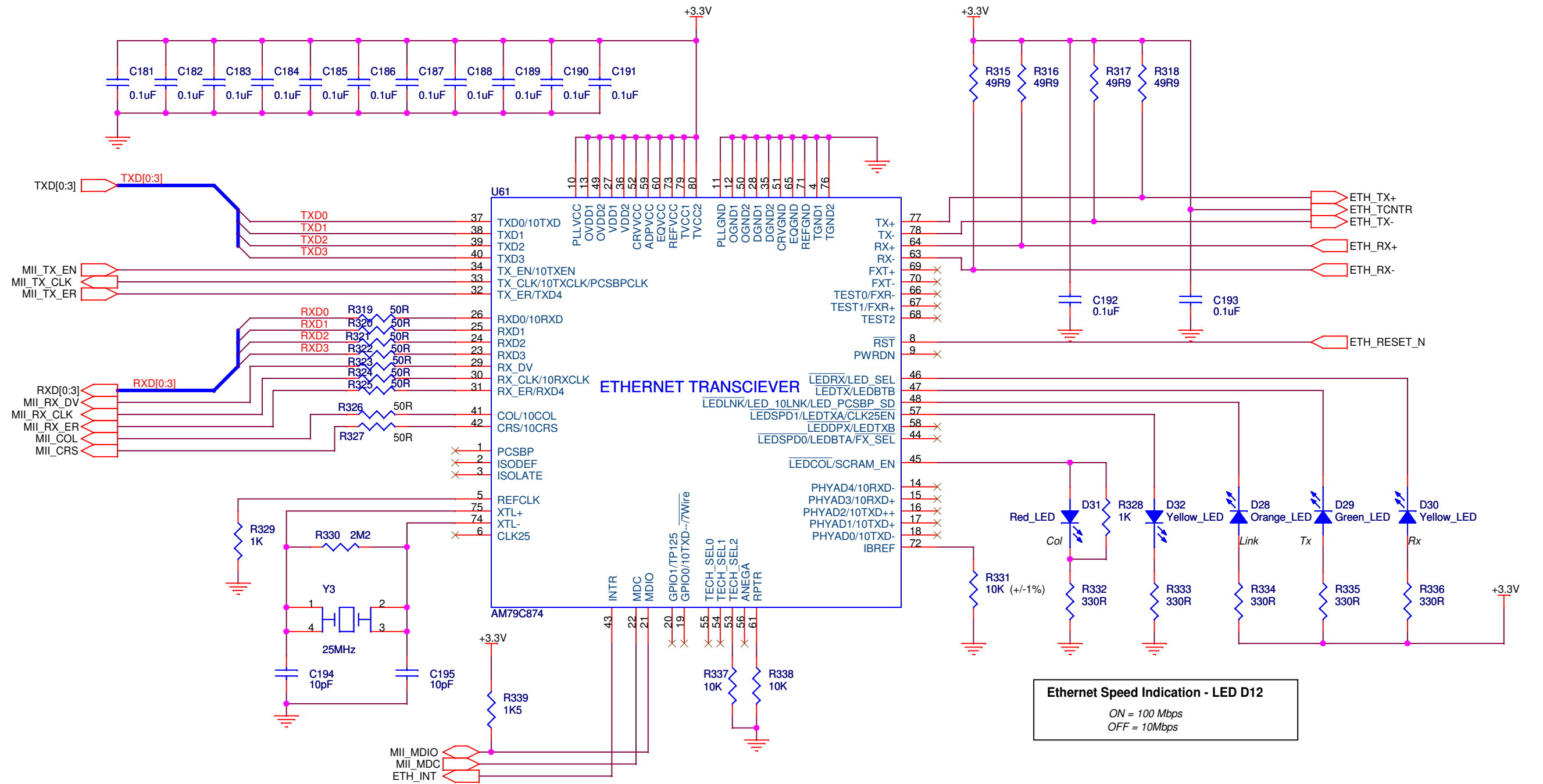






Design: Chris Hammond. Reviewed: Nigel Dick. Motorola EKB, Scotland									
Title MPC8260 Power Configuration									
Size B	Document Number Quioch Reference Design							Rev A1	
Date:	Tuesday, July 09, 2002				Sheet	11	of	46	1

Bypass capacitors of 0.1 uF between the power and ground pins are recommended. The four areas where the capacitors must be very close to the pins (within 3 mm) are the PLL (pins 10 and 11), Clock Re-recovery (pins 51 and 52), Equalizer (pins 60 and 65), and Bandgap Reference (pins 71 and 73) areas. The other bypass capacitors should be placed as close to the pins as possible.

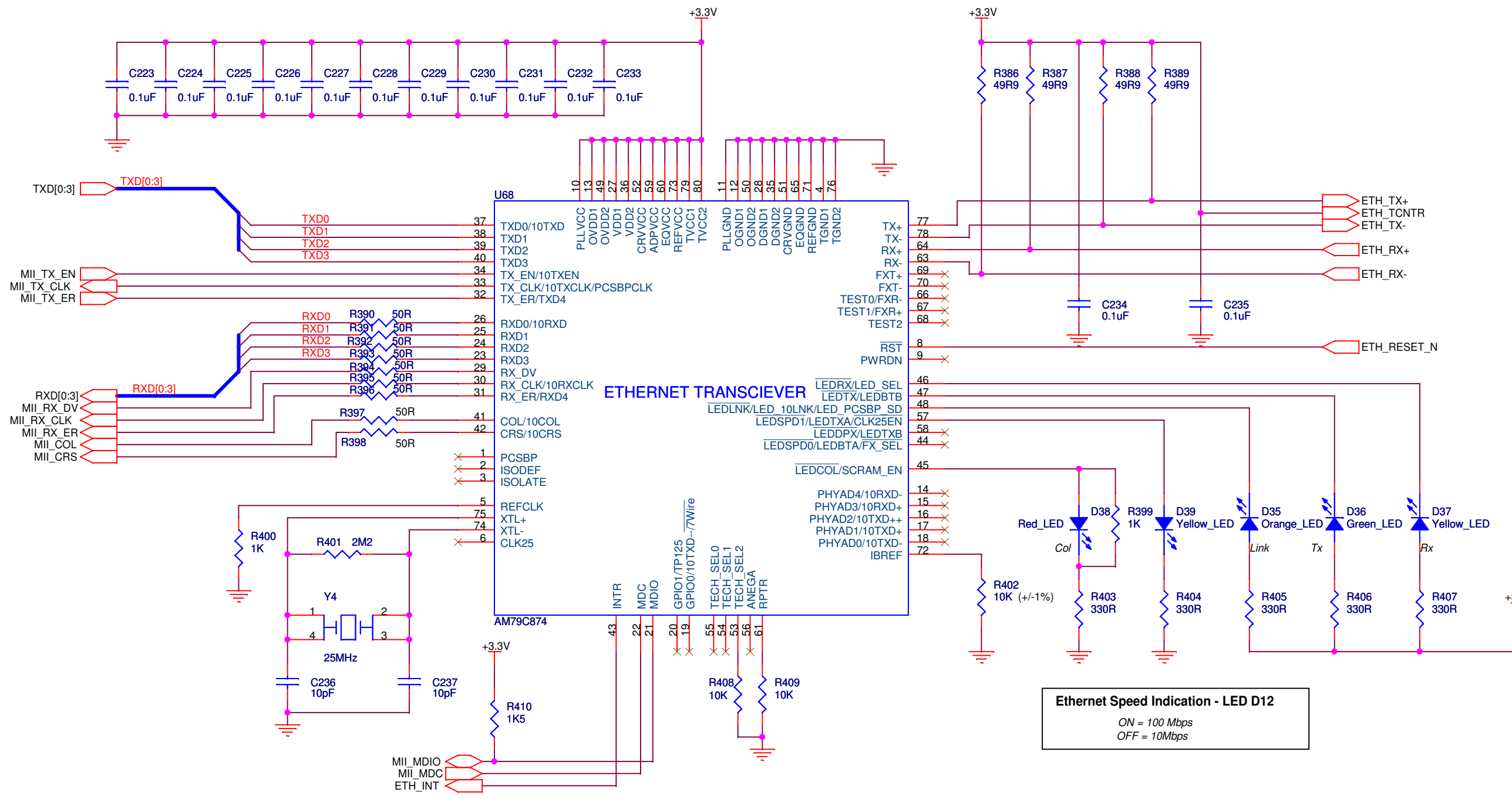


Ethernet Speed Indication - LED D12

ON = 100 Mbps
OFF = 10Mbps

Design: Christian Hammond. Reviewed: Michael Johnston. Motorola EKE, Scotland			
Title Ethernet Transciever Configuration			
Size B	Document Number		Rev A1
Quioch Reference Design			
Date:	Tuesday, July 09, 2002	Sheet 12 of 46	

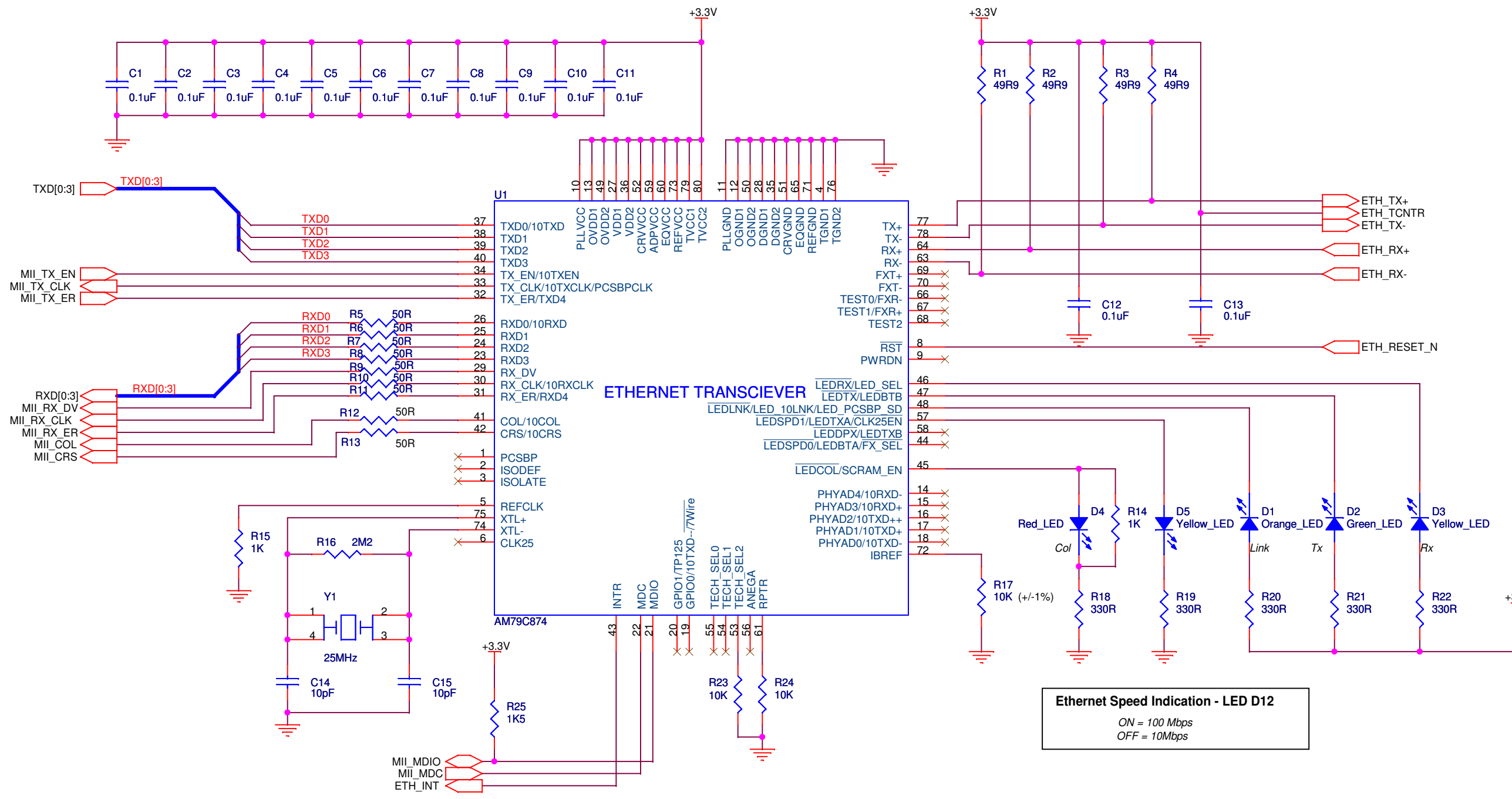
Bypass capacitors of 0.1 uF between the power and ground pins are recommended. The four areas where the capacitors must be very close to the pins (within 3 mm) are the PLL (pins 10 and 11), Clock Re-covey (pins 51 and 52), Equalizer (pins 60 and 65), and Bandgap Reference (pins 71 and 73) areas. The other bypass capacitors should be placed as close to the pins as possible.



Ethernet Speed Indication - LED D12
ON = 100 Mbps
OFF = 10Mbps

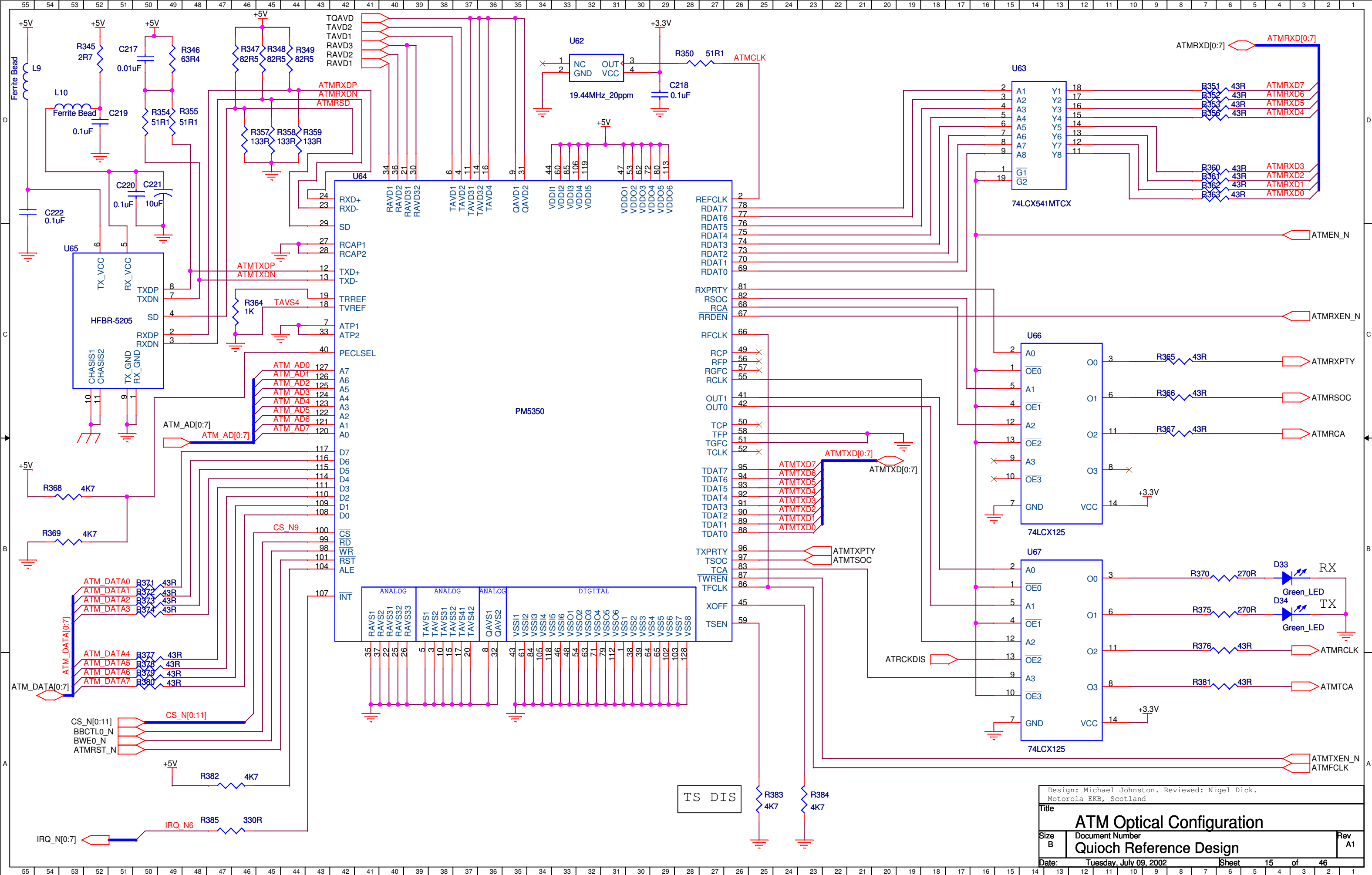
Design: Christian Hammond. Reviewed: Michael Johnston. Motorola EKB, Scotland		
Title Ethernet Transceiver Configuration		
Size B	Document Number Quioch Reference Design	Rev A1
Date: Tuesday, July 09, 2002	Sheet 12	of 46

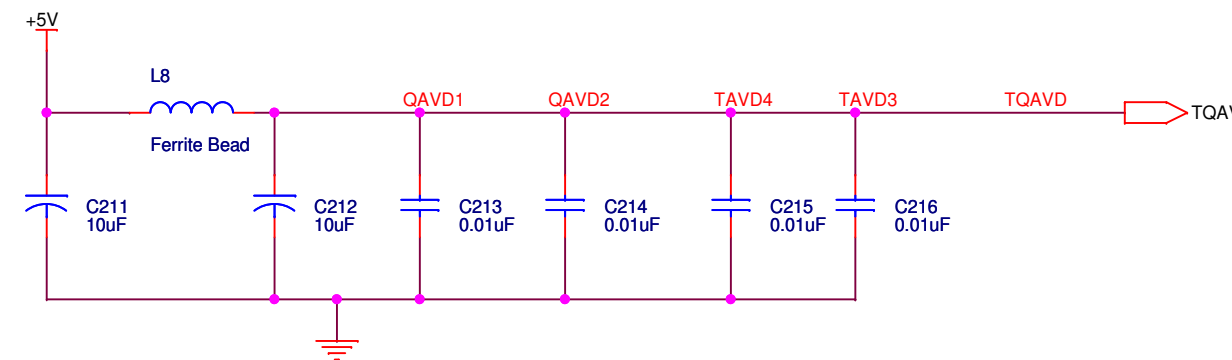
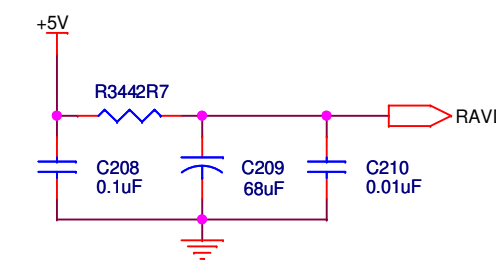
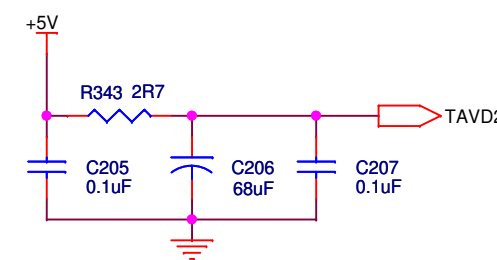
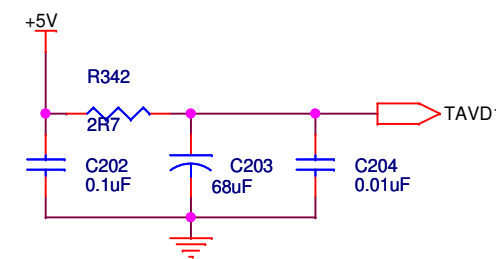
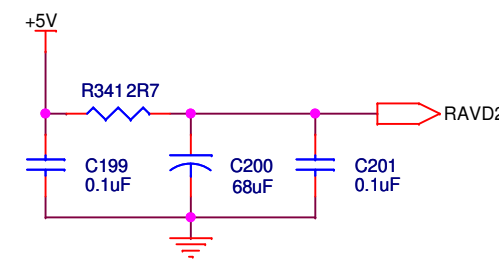
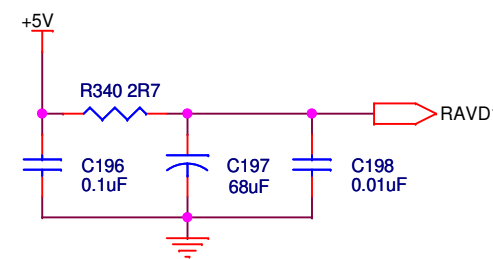
Bypass capacitors of 0.1 uF between the power and ground pins are recommended. The four areas where the capacitors must be very close to the pins (within 3 mm) are the PLL (pins 10 and 11), Clock Re-covey (pins 51 and 52), Equalizer (pins 60 and 65), and Bandgap Reference (pins 71 and 73) areas. The other bypass capacitors should be placed as close to the pins as possible.



Ethernet Speed Indication - LED D12
ON = 100 Mbps
OFF = 10Mbps

Design: Christian Hammond. Reviewed: Michael Johnston. Motorola EKB, Scotland		
Title Ethernet Transceiver Configuration		
Size B	Document Number Quioch Reference Design	Rev A1
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These circuits are used for:

TDAV1 - Power pin for transmit clock synthesizer reference circuitry.

RAVD1 - Power pin for receive clock and data recovery block

See data sheet for PMC5350 to get descriptions of others

Design: Michael Johnston. Reviewed: Nigel Dick.
Motorola EKB, Scotland

Title

ATM Optical Power Configuration

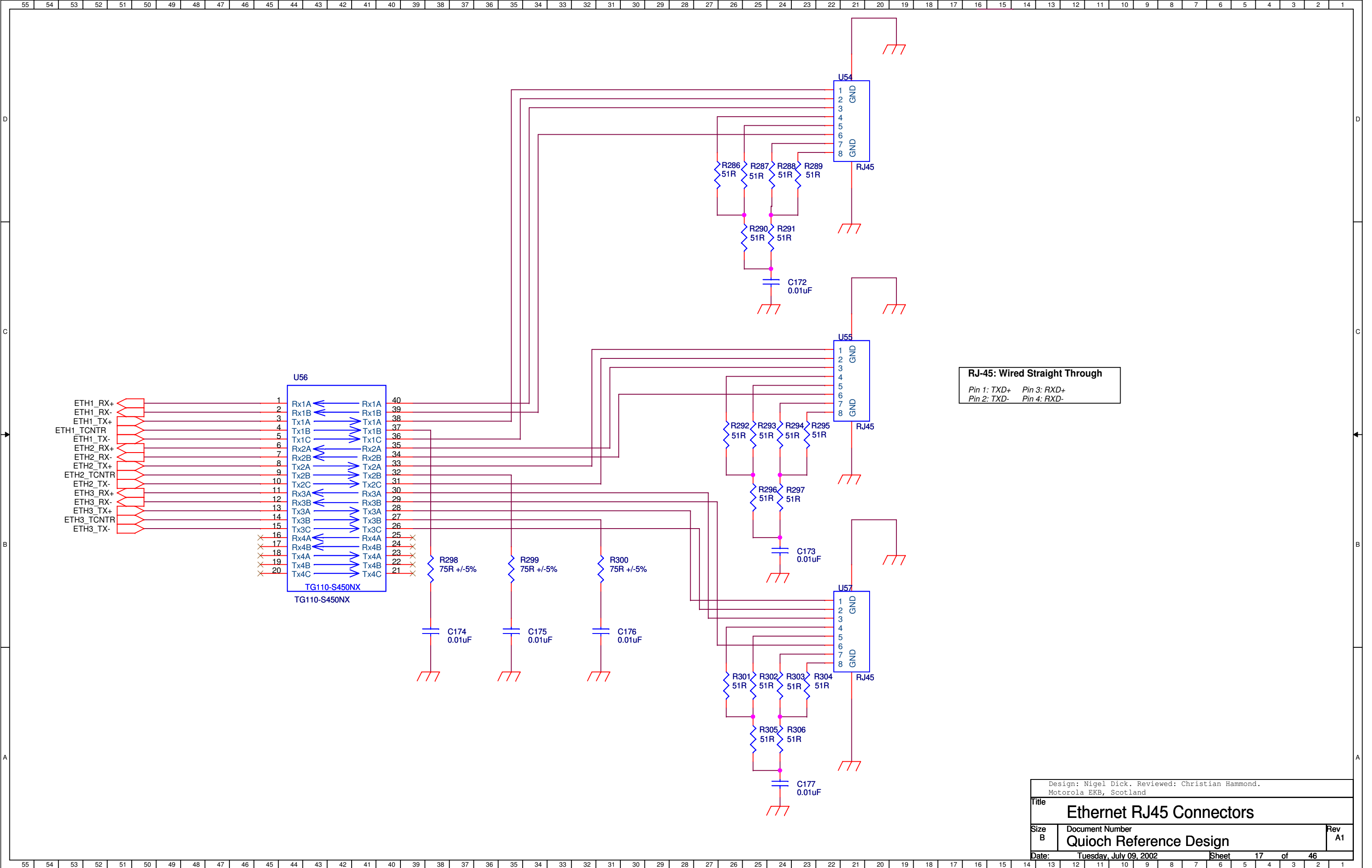
Size
B

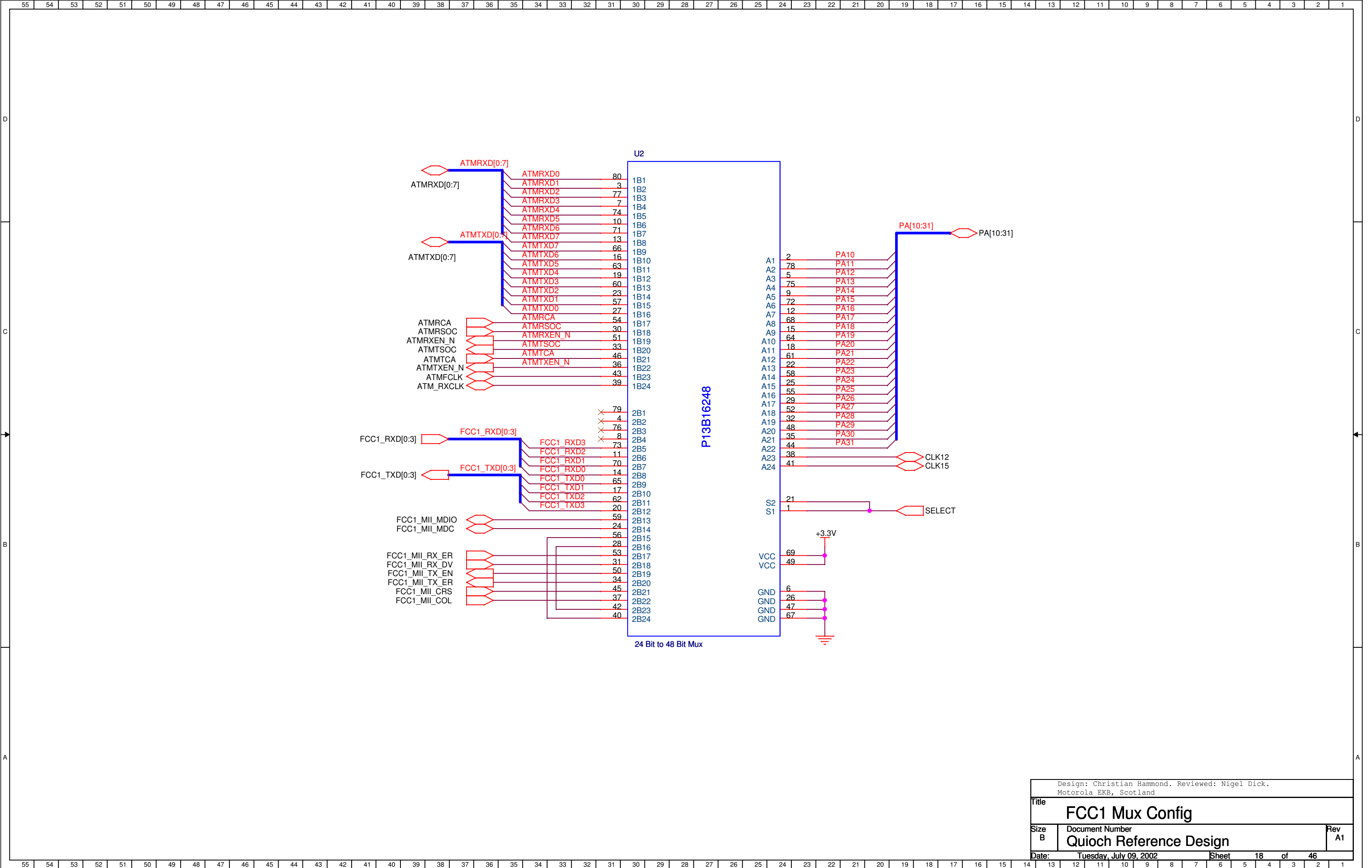
Size B	Document Number Quioch Reference Design
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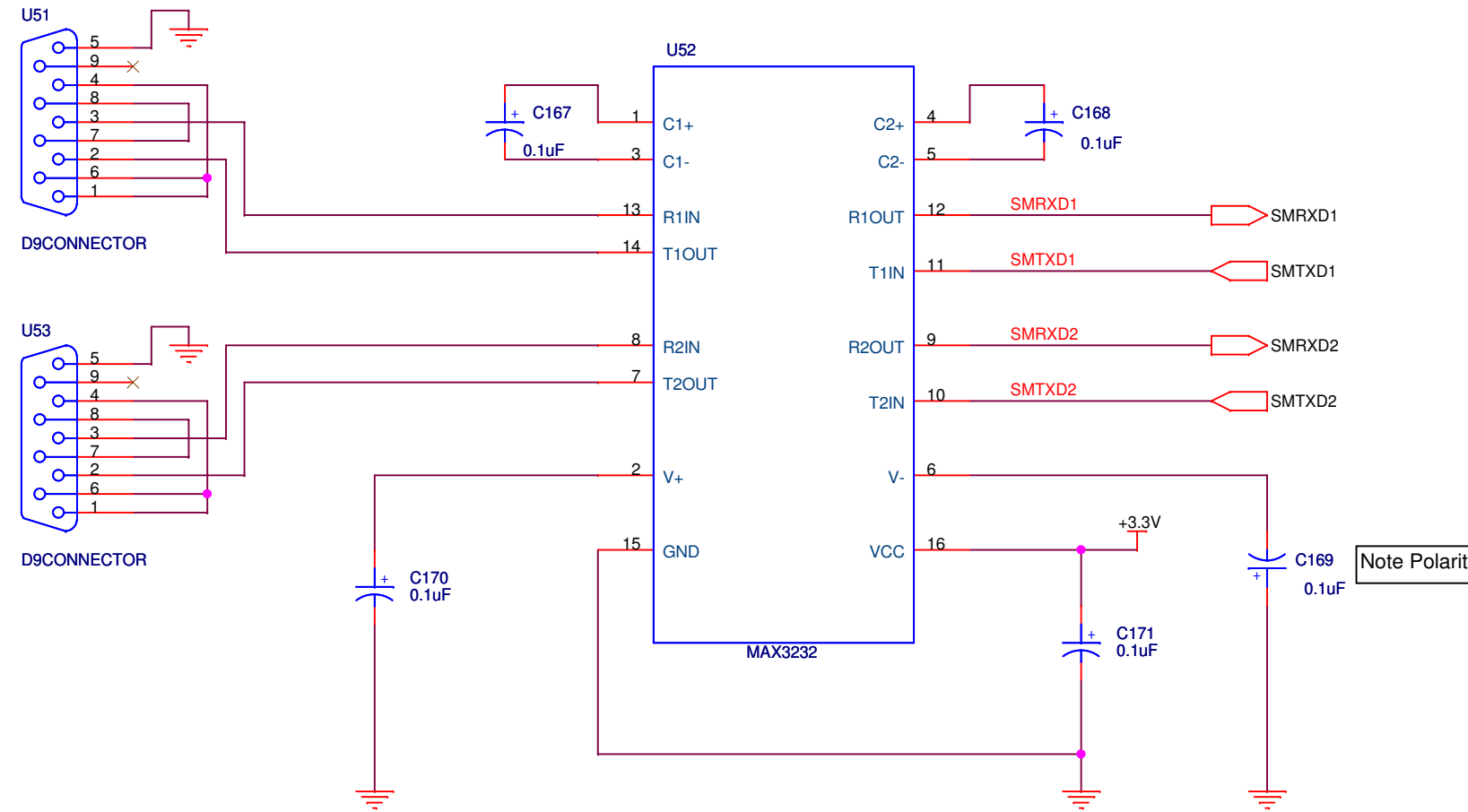
Date:

Date:	Tuesday, July 09, 2002	Sheet	16	of	46
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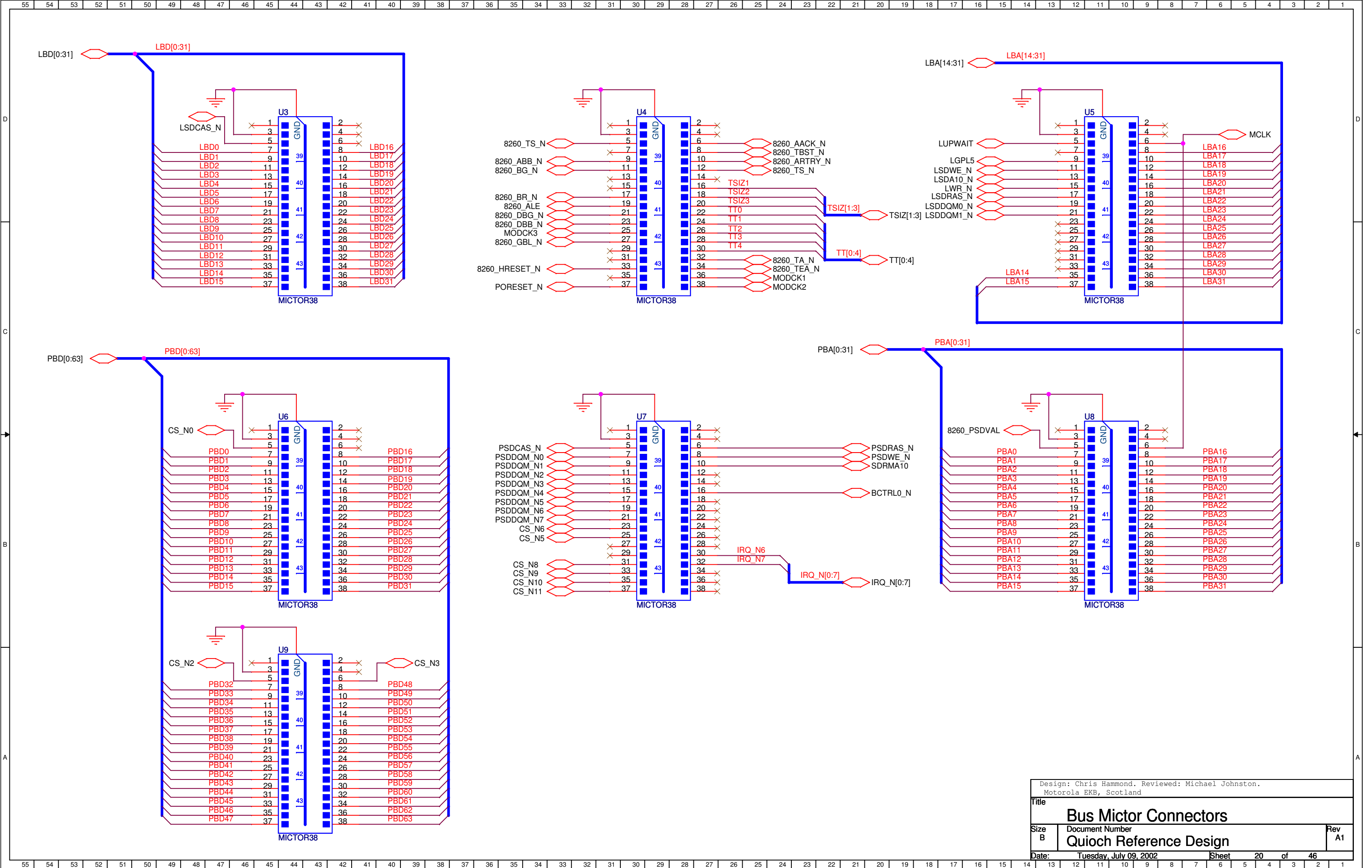
4	13	12	11	10	9	8	7	6	5	4	3	2
---	----	----	----	----	---	---	---	---	---	---	---	---

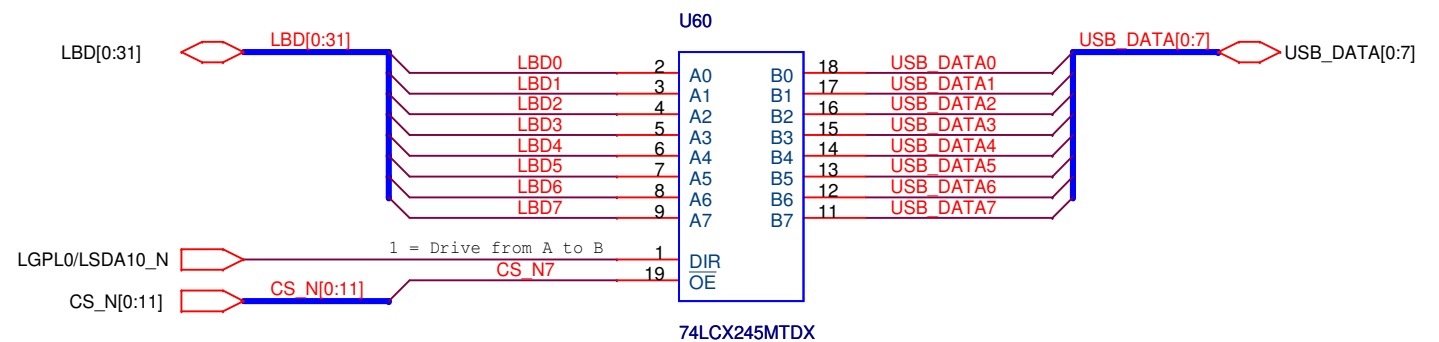
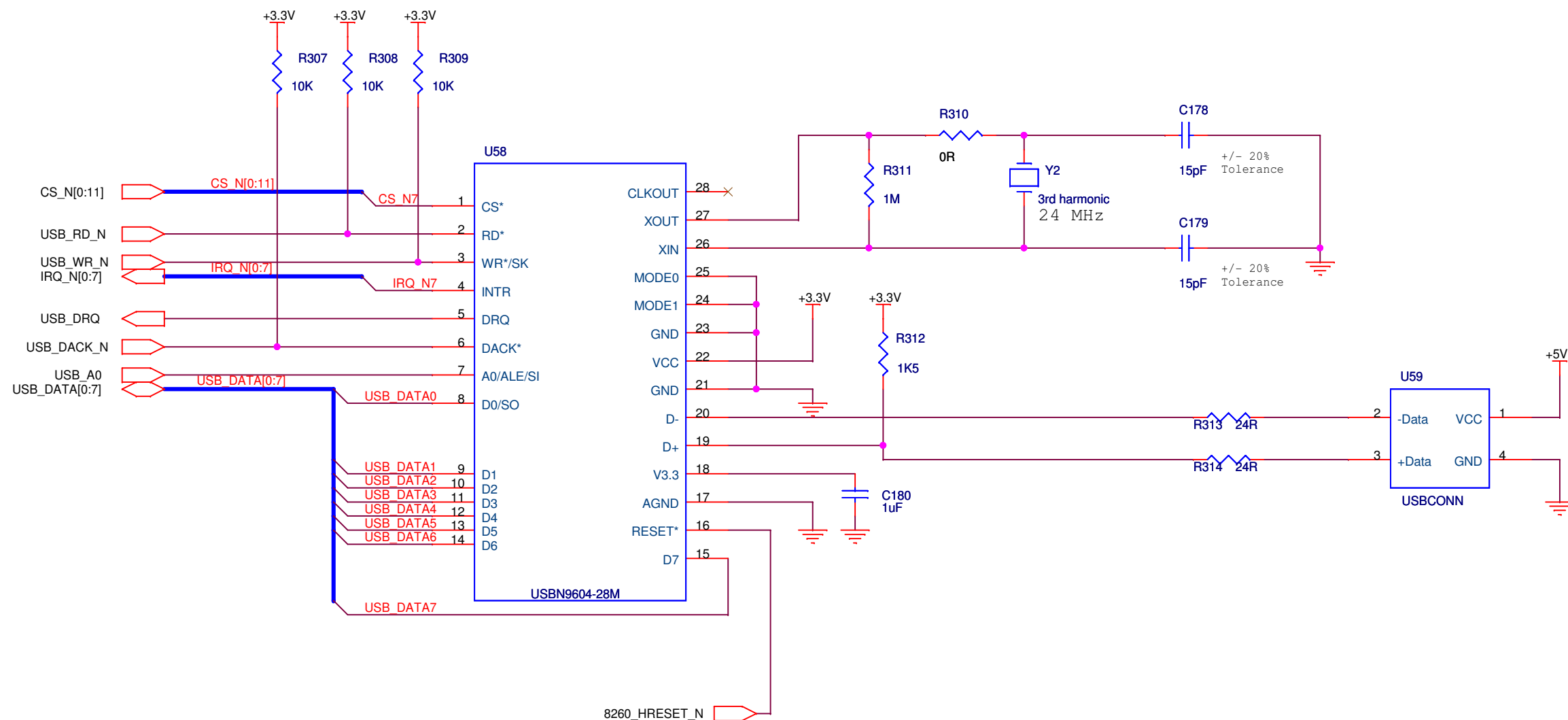




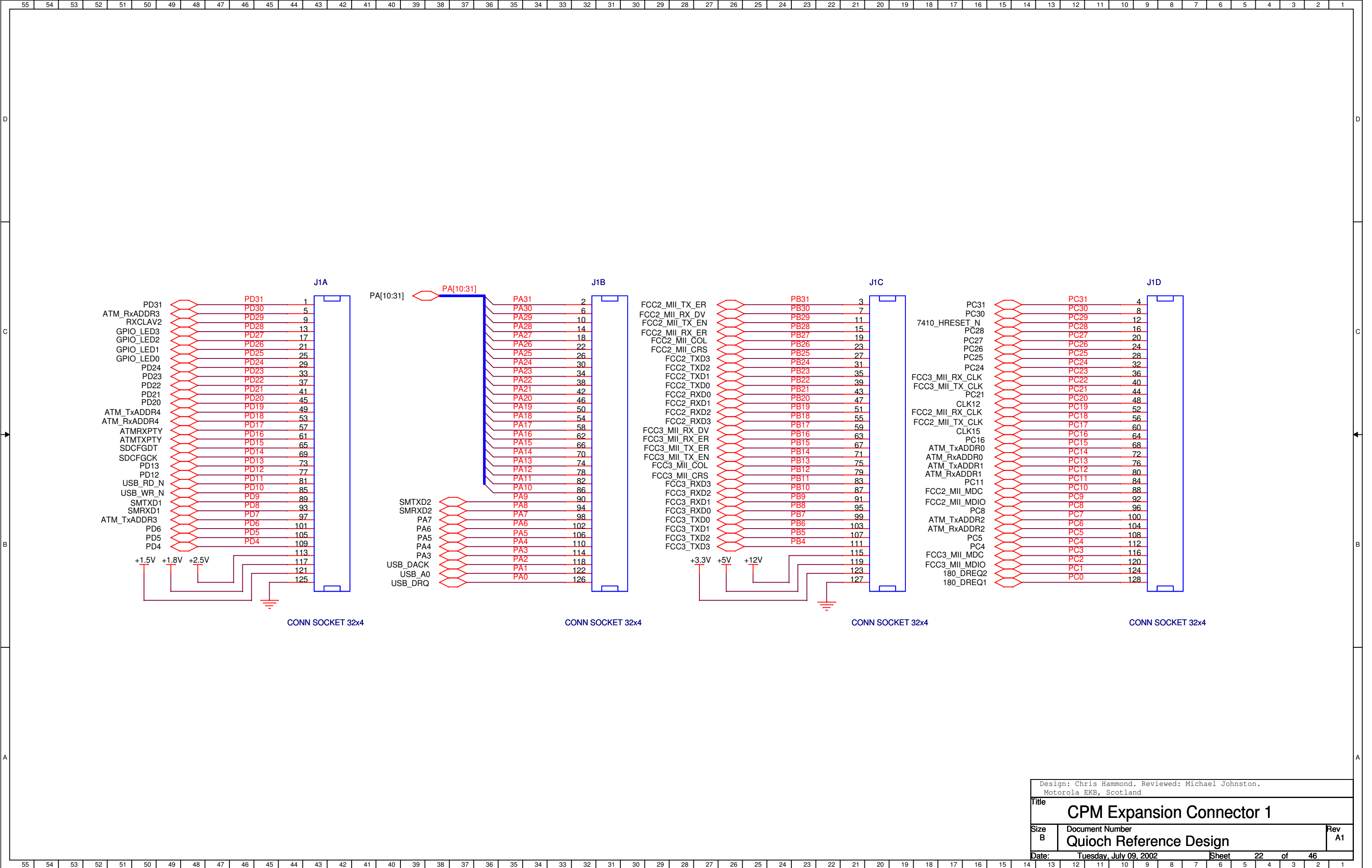


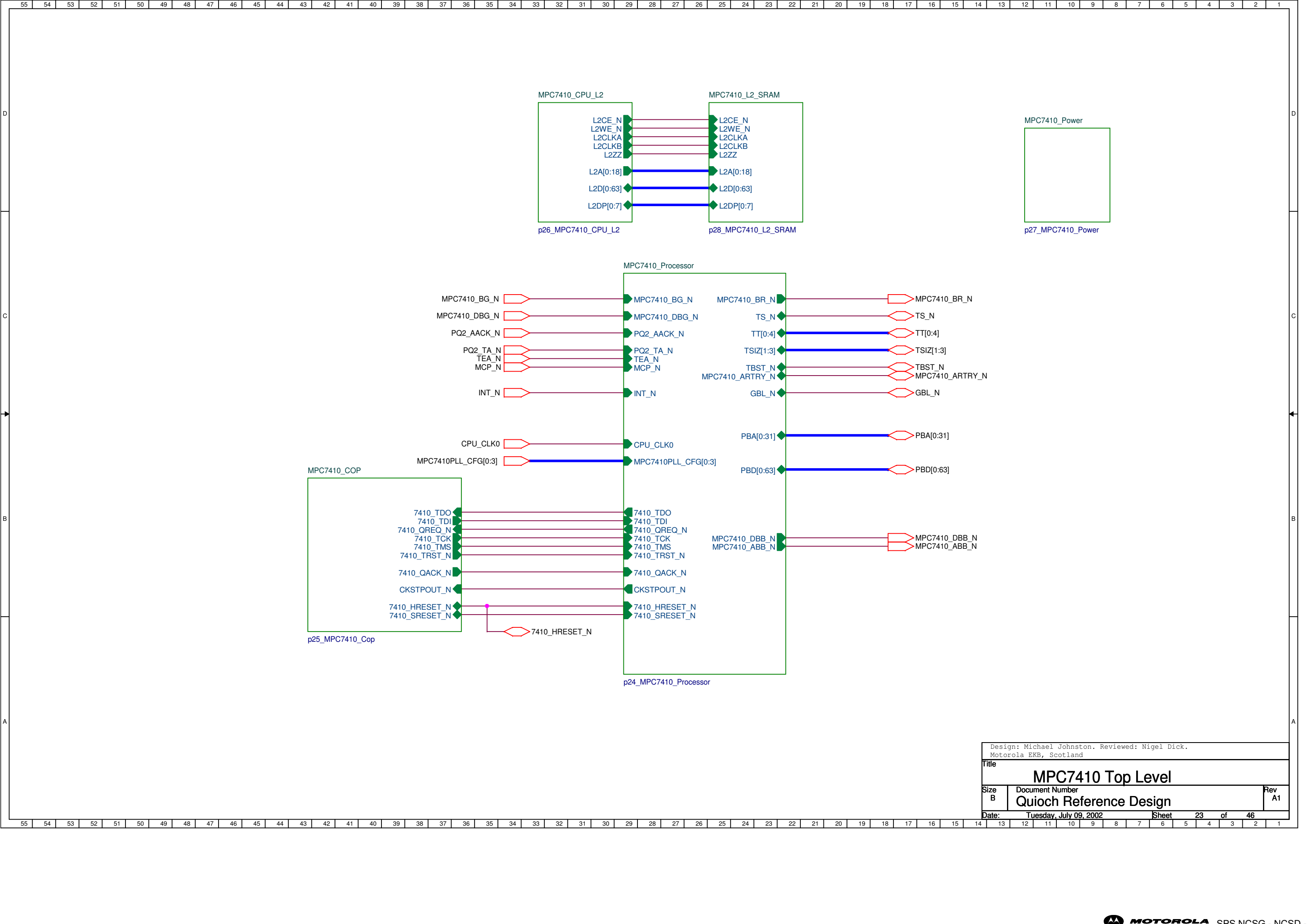
Design: Michael Johnston. Reviewed: Chris Hammond. Motorola EKB, Scotland									
Title									
SMC UART Configuration									
Size B	Document Number Quioch Reference Design								Rev A1
Date:	Tuesday, July 09, 2002				Sheet	19	of	46	



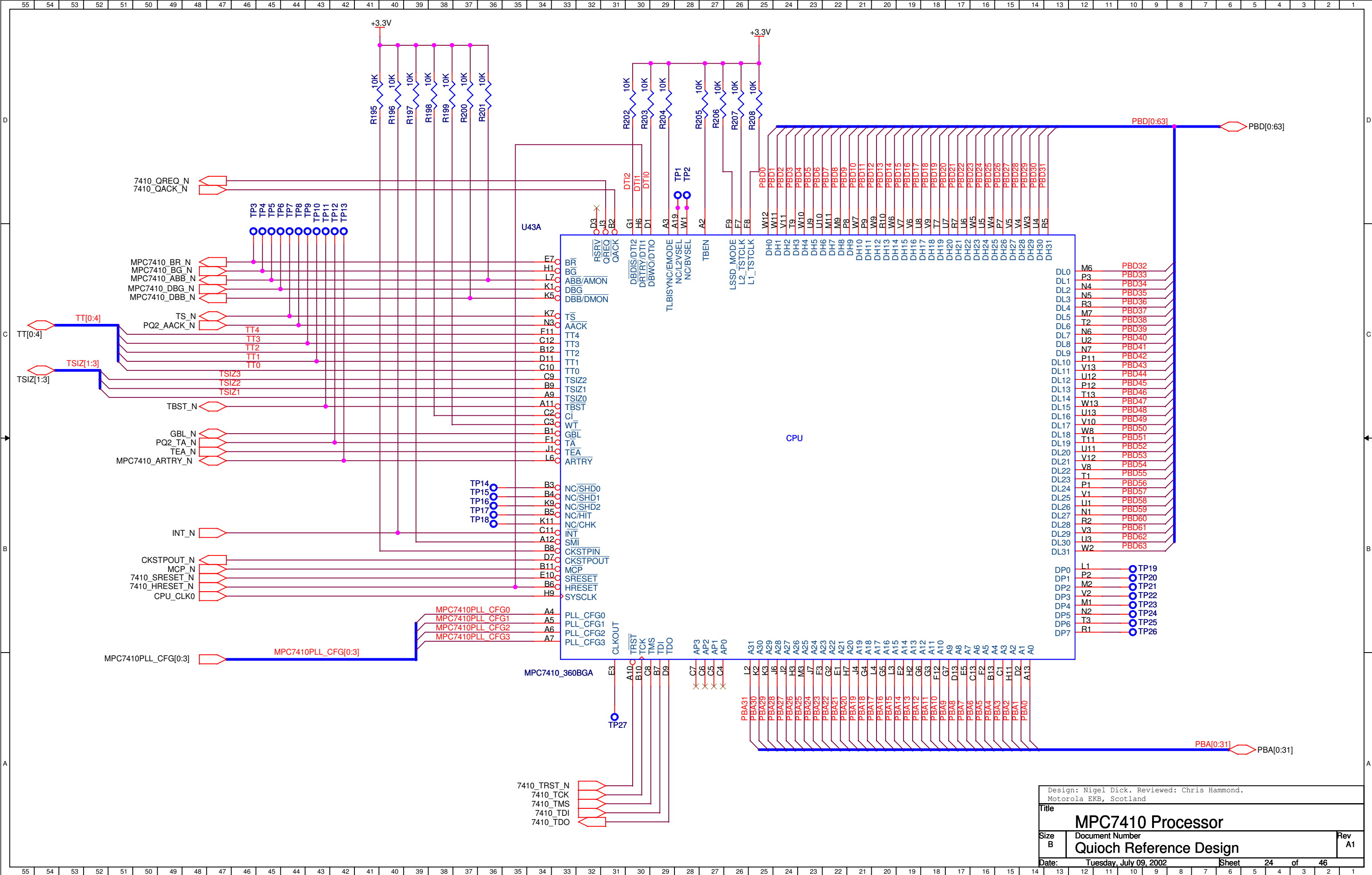


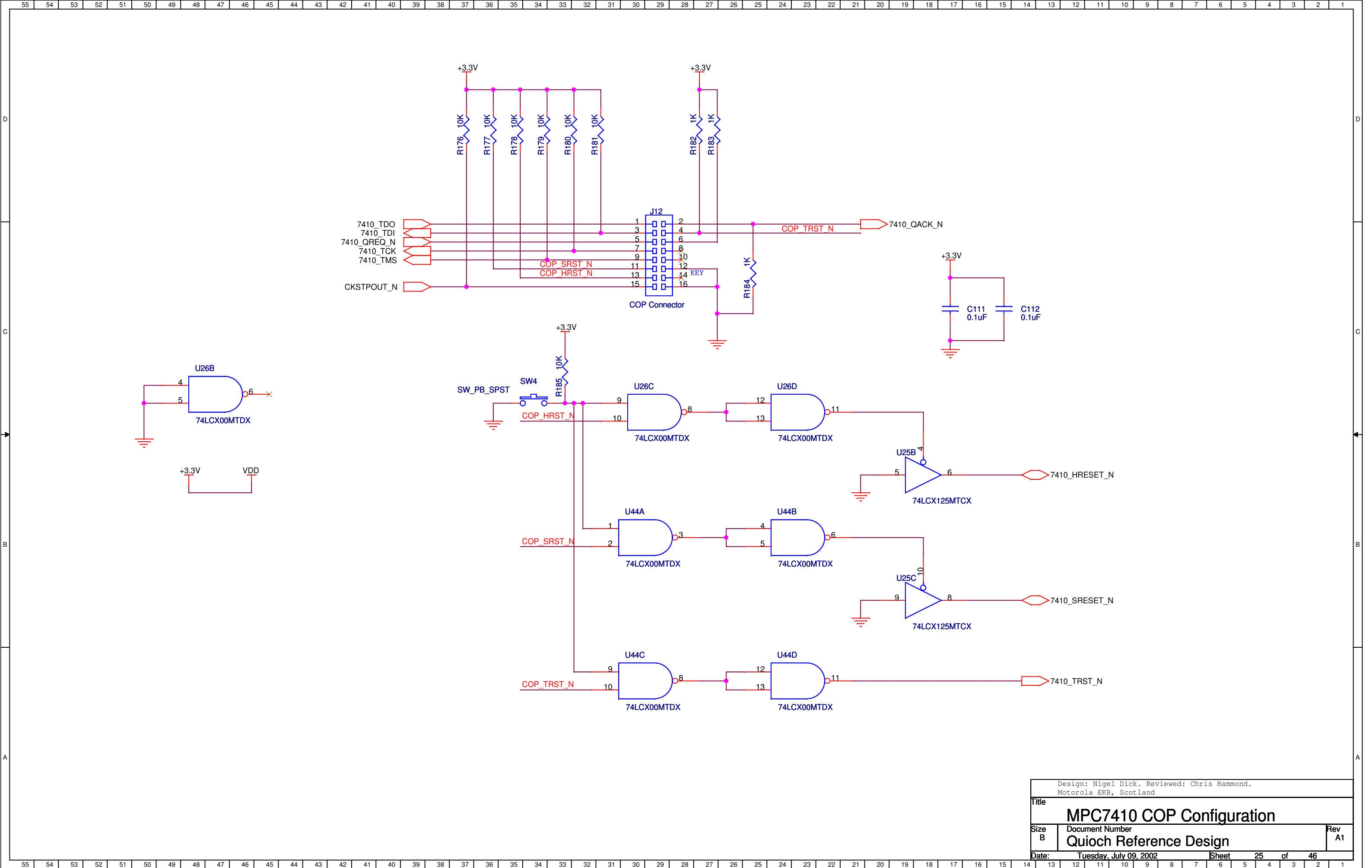
Design: Michael Johnston. Reviewed: Nigel Dick. Motorola EKB, Scotland									
Title									
USB Configuration									
Size B	Document Number								Rev A1
Quioch Reference Design									
Date:	Tuesday, July 09, 2002				Sheet	21	of	46	



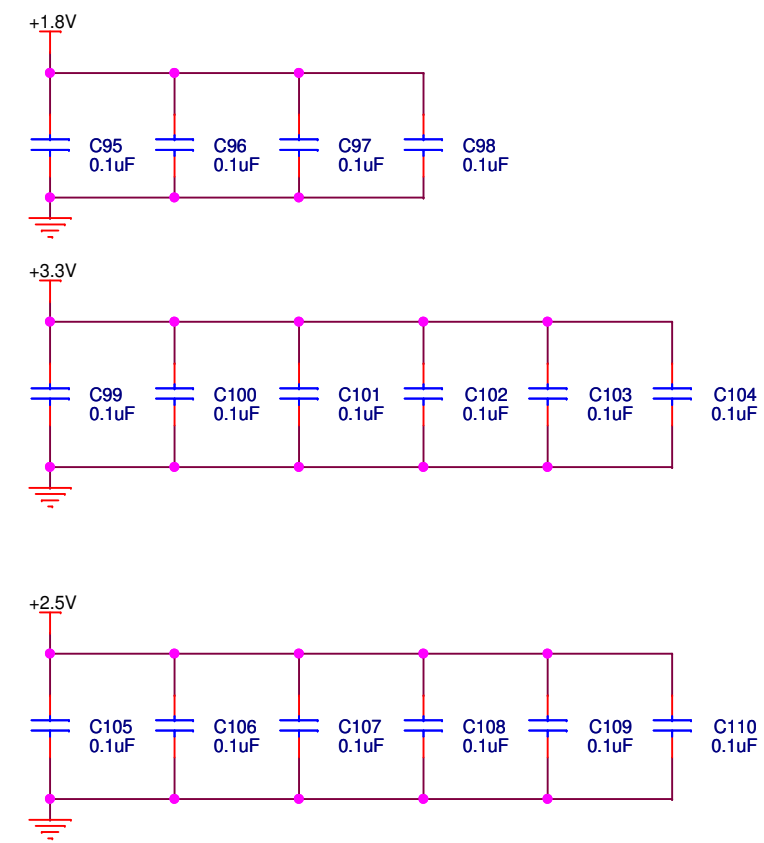
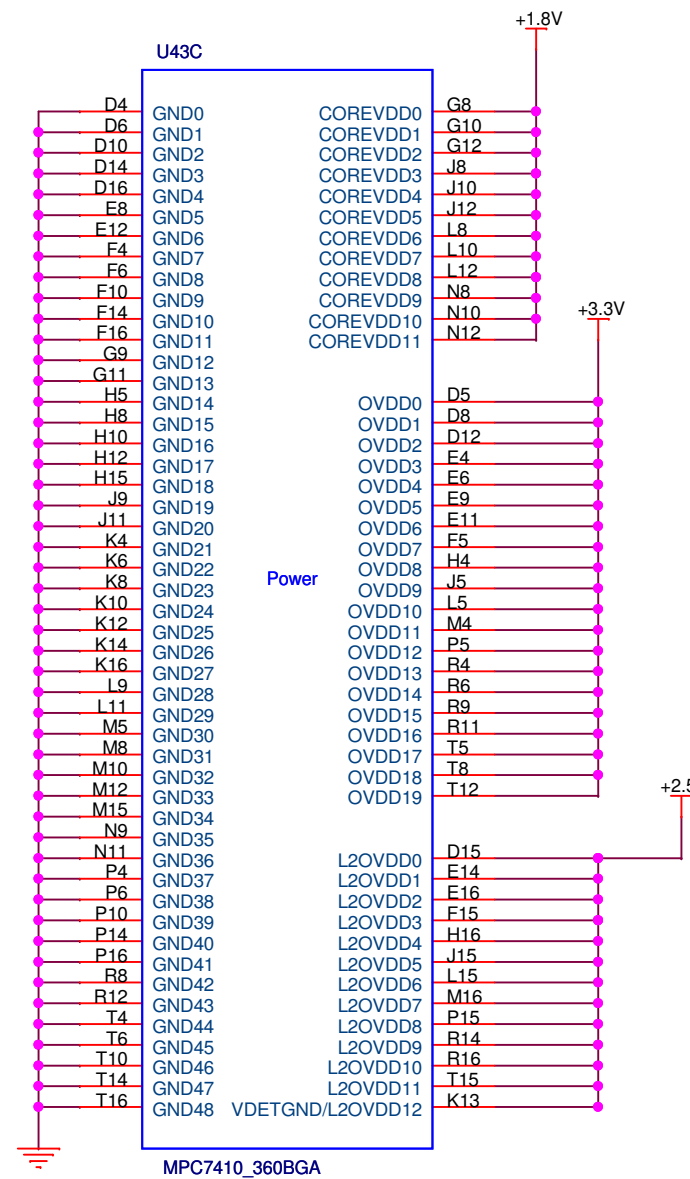


Design: Michael Johnston. Reviewed: Nigel Dick. Motorola EKB, Scotland																			
Title MPC7410 Top Level																			
Size B	Document Number Quioch Reference Design																	Rev A1	
Date:	Tuesday, July 09, 2002					Sheet					23	of					46		

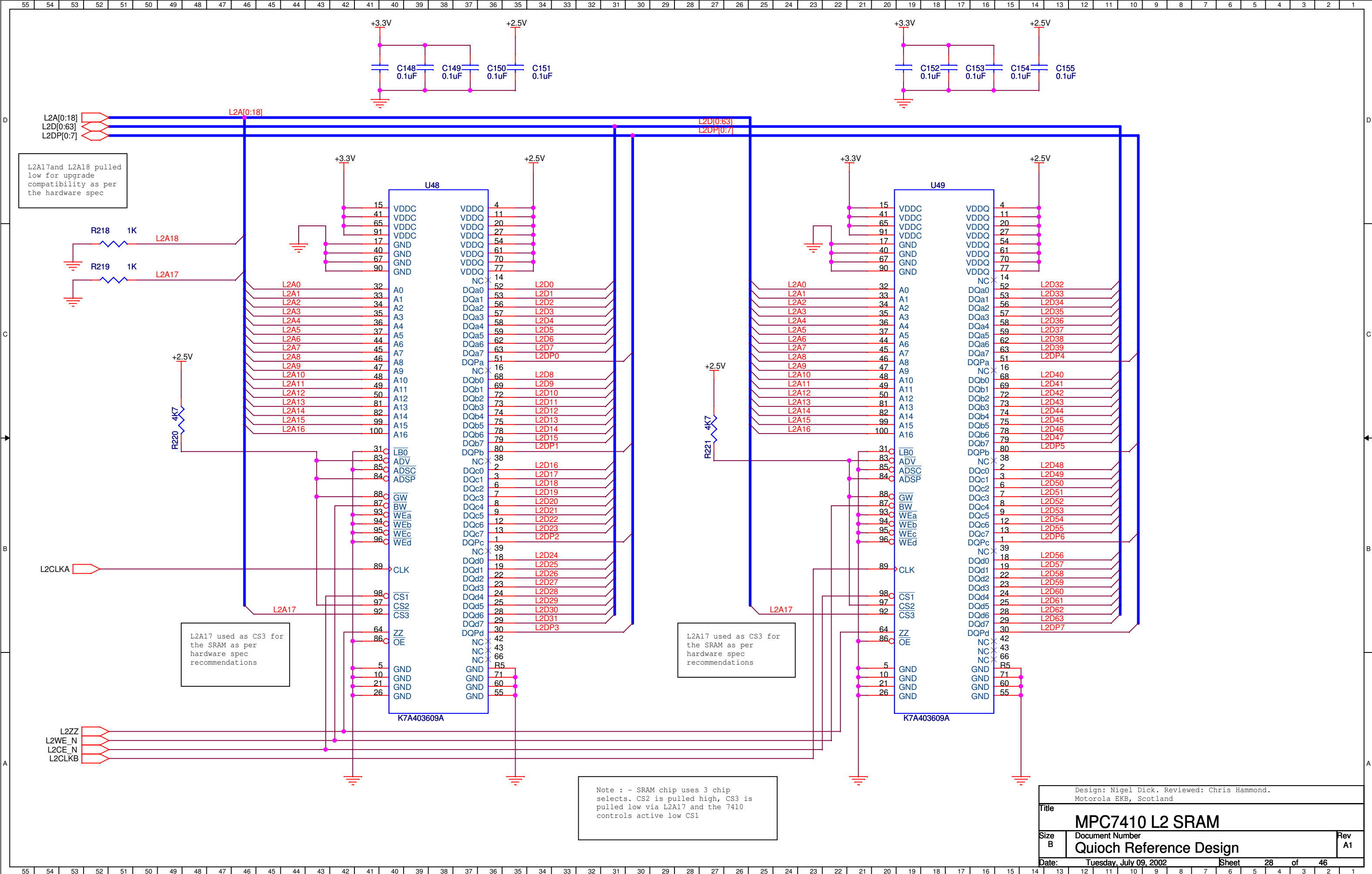


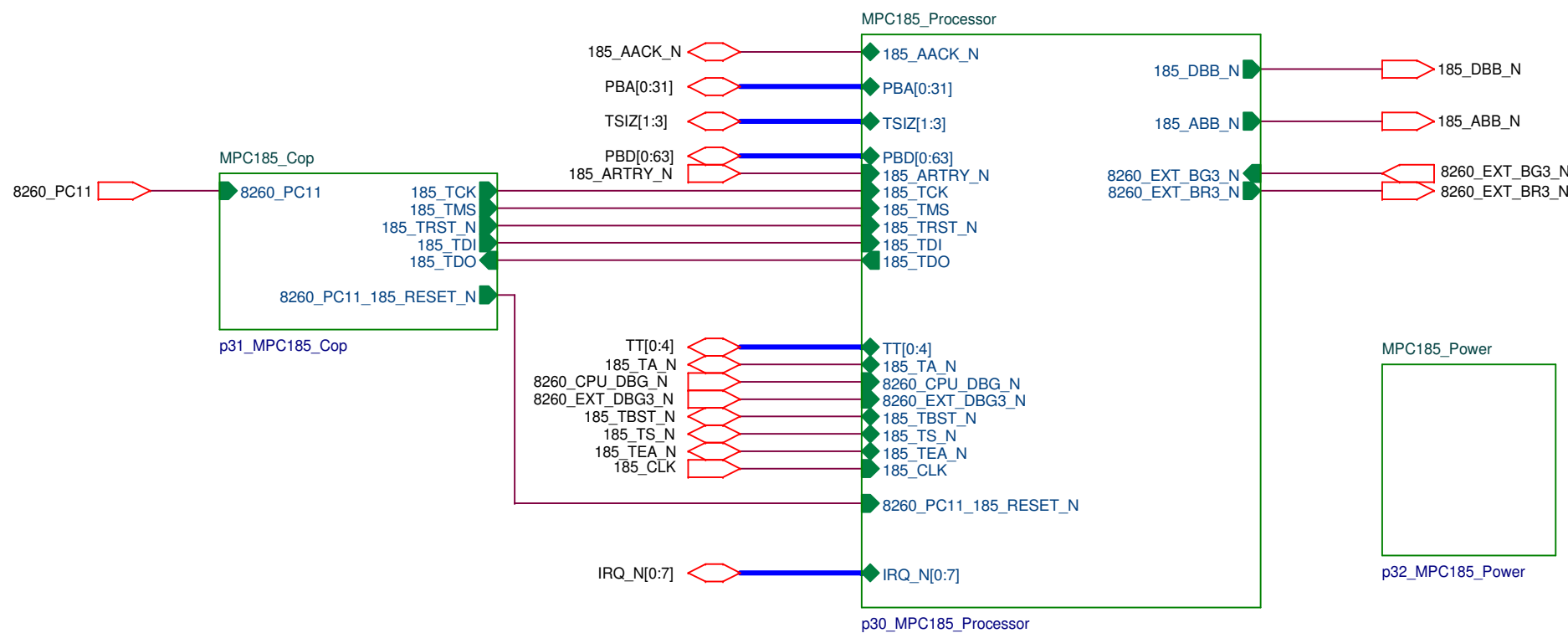


Design: Nigel Dick. Reviewed: Chris Hammond. Motorola EKB, Scotland													
Title MPC7410 COP Configuration													
Size B		Document Number Quioch Reference Design										Rev A1	
Date:		Tuesday, July 09, 2002					Sheet	25	of	46			
1	3	12	11	10	9	8	7	6	5	4	3	2	1



Design: Nigel Dick. Reviewed: Chris Hammond. Motorola EKB, Scotland																			
Title MPC7410 Power																			
Size B		Document Number Quioch Reference Design															Rev A1		
Date:		Tuesday, July 09, 2002										Sheet		27		of		46	
14	13	12	11	10	9	8	7	6	5	4	3	2	1						



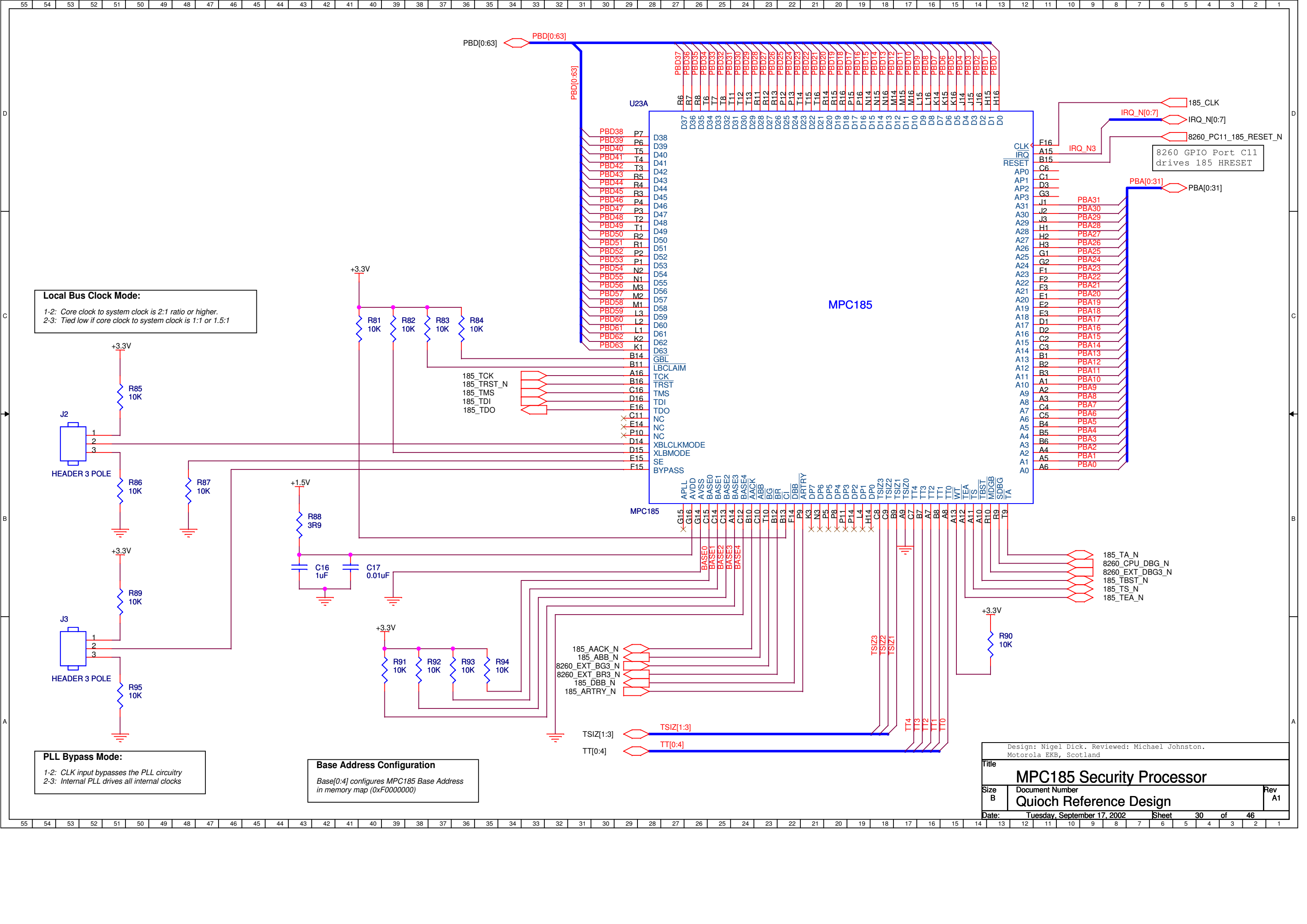


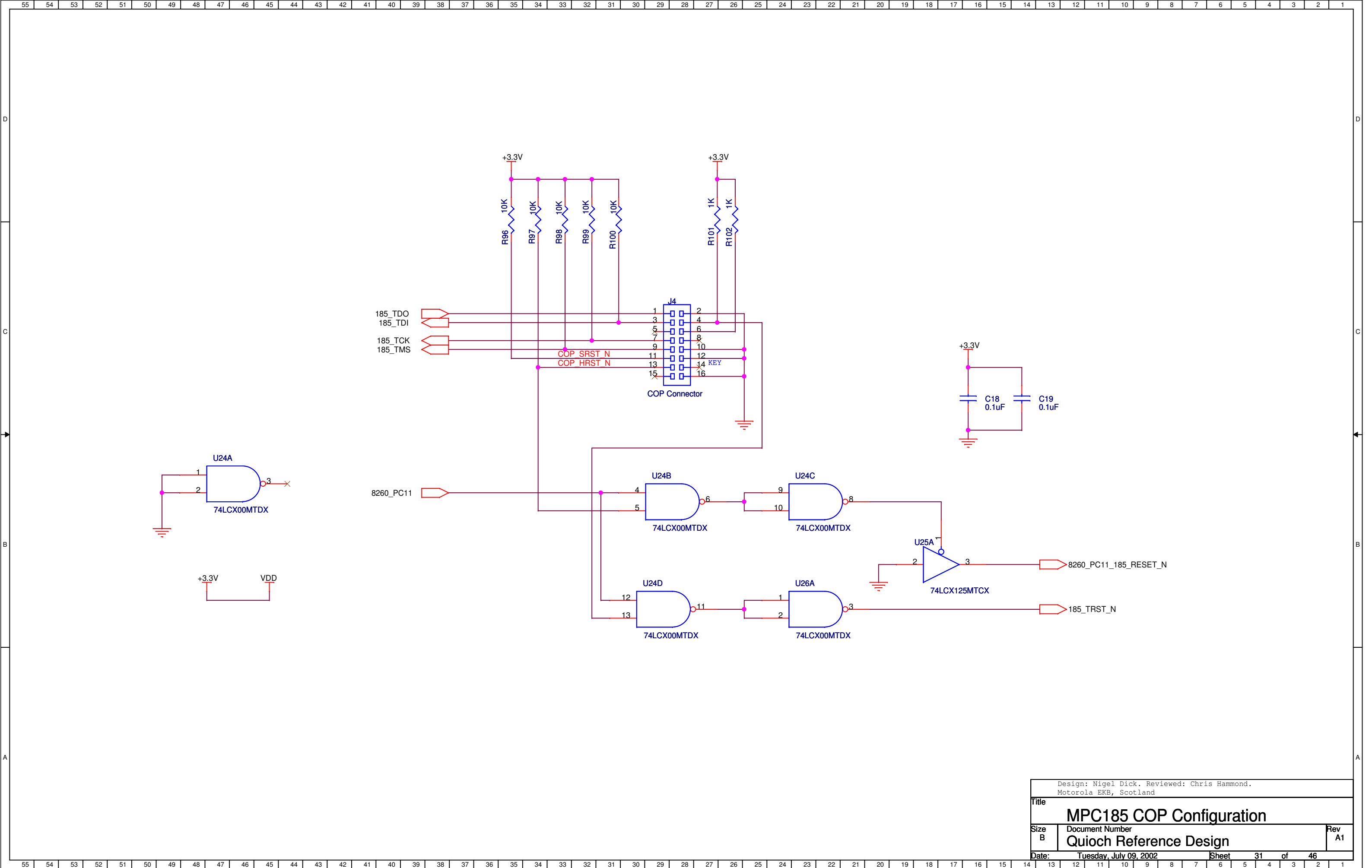
Local Bus Clock Mode:
1-2: Core clock to system clock is 2:1 ratio or higher.
2-3: Tied low if core clock to system clock is 1:1 or 1.5:1

PLL Bypass Mode:
1-2: CLK input bypasses the PLL circuitry
2-3: Internal PLL drives all internal clocks

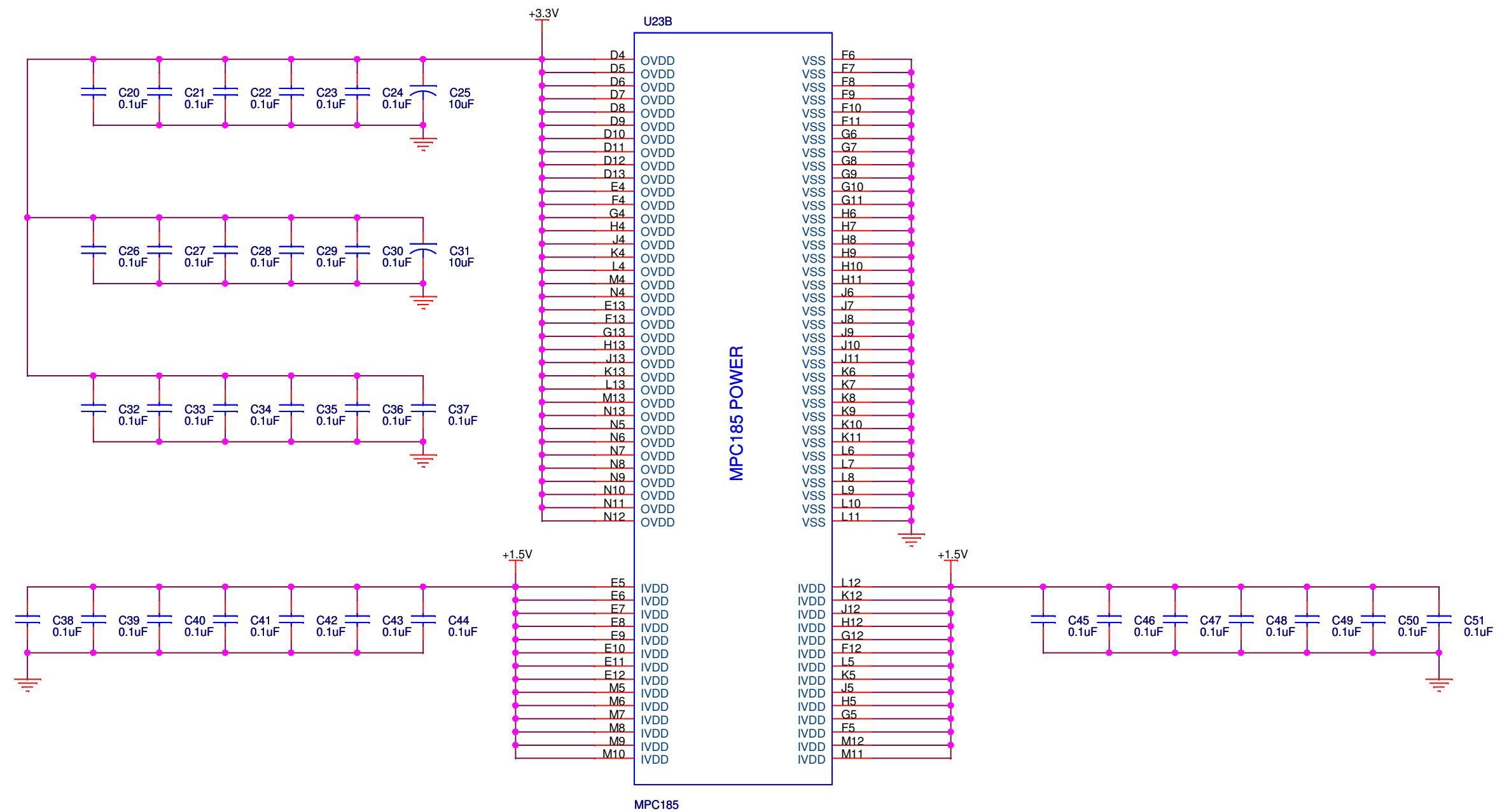
Base Address Configuration
Base[0:4] configures MPC185 Base Address in memory map (0xF0000000)

Design: Nigel Dick. Reviewed: Michael Johnston. Motorola EKB, Scotland											
Title MPC185 Security Processor											
Size B		Document Number Quioch Reference Design								Rev A1	
Date:		Tuesday, September 17, 2002				Sheet		30		of 46	

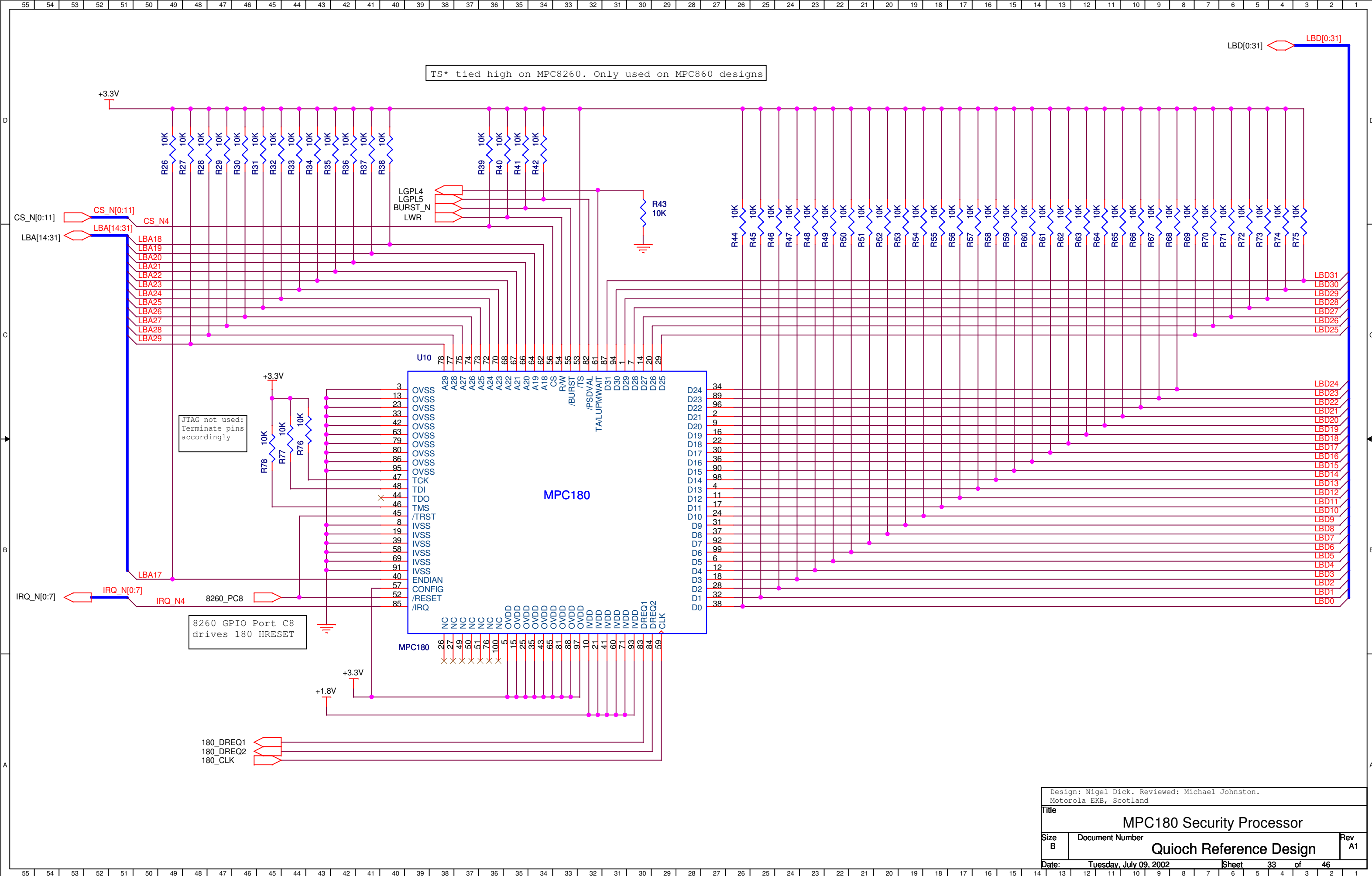


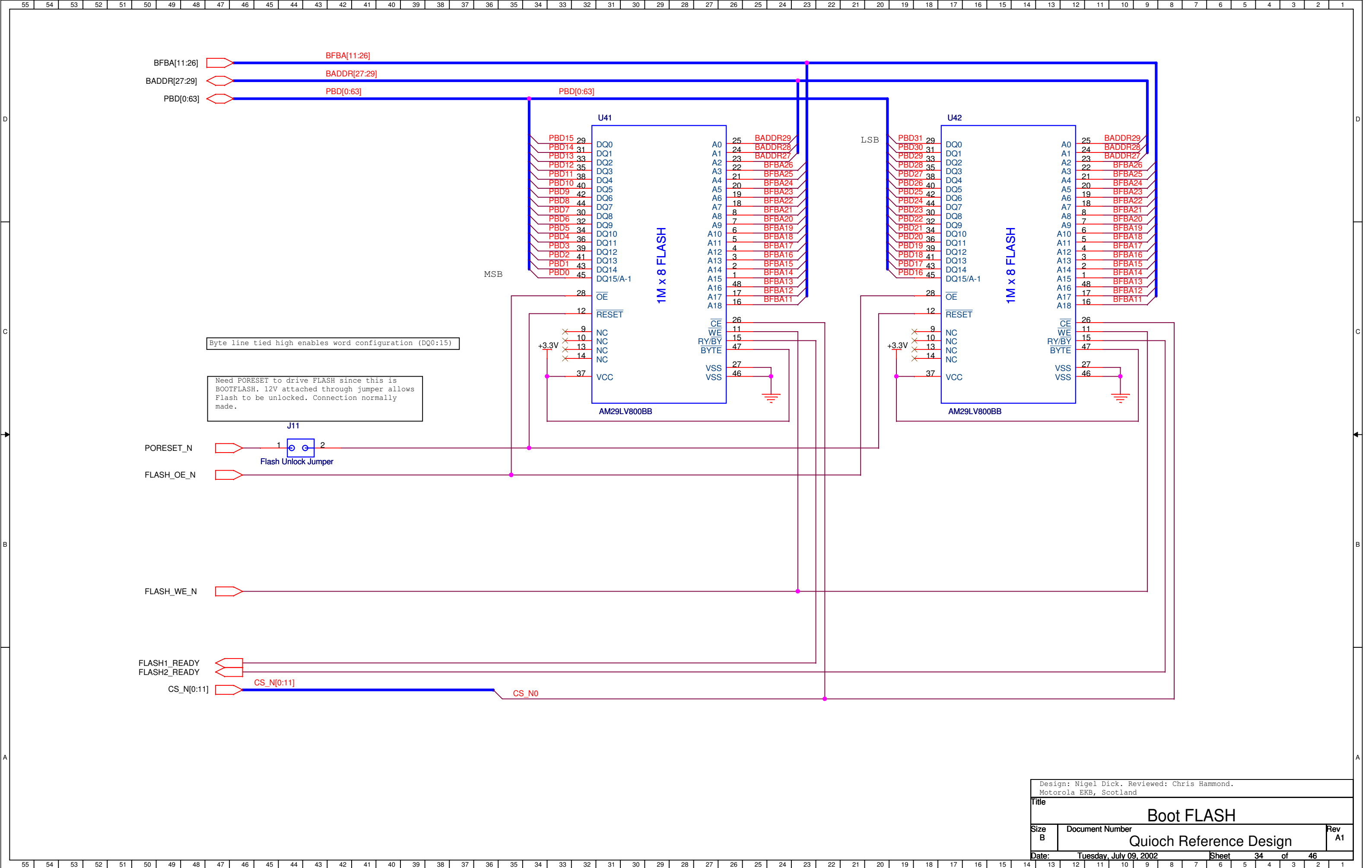


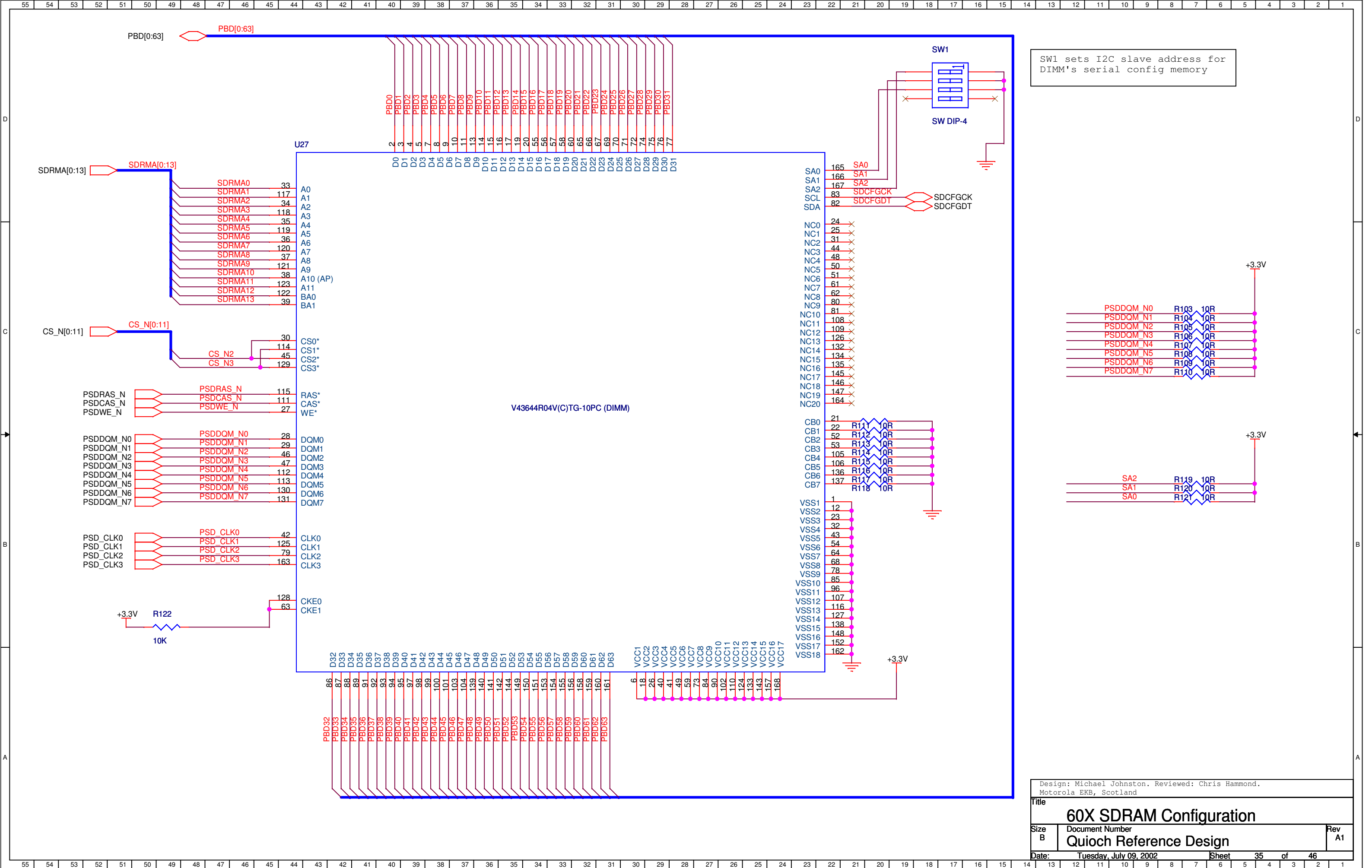
Design: Nigel Dick. Reviewed: Chris Hammond. Motorola EKB, Scotland		
Title MPC185 COP Configuration		
Size B	Document Number Quioch Reference Design	Rev A1
Date: Tuesday, July 09, 2002	Sheet 31	of 46

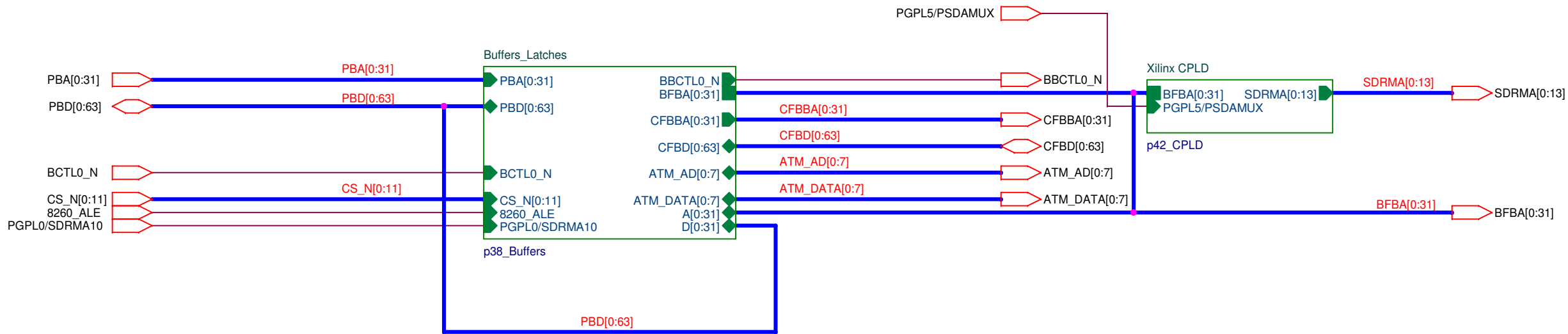


Design: Nigel Dick. Reviewed: Michael Johnston. Motorola EKB, Scotland													
Title MPC185 Power													
Size B		Document Number Quioch Reference Design											Rev A1
Date: Tuesday, July 09, 2002													
Sheet 32 of 46													
14	13	12	11	10	9	8	7	6	5	4	3	2	1

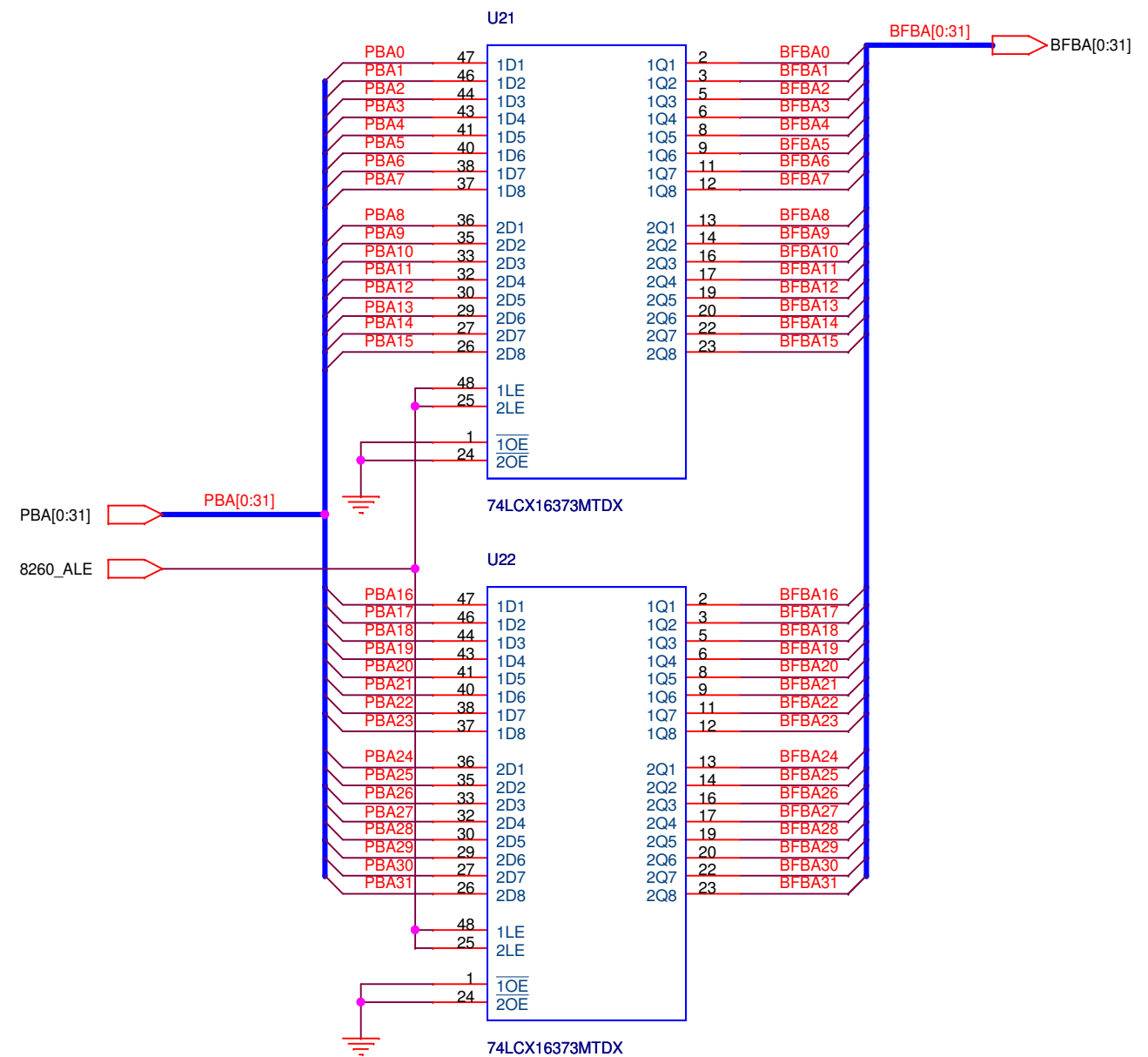




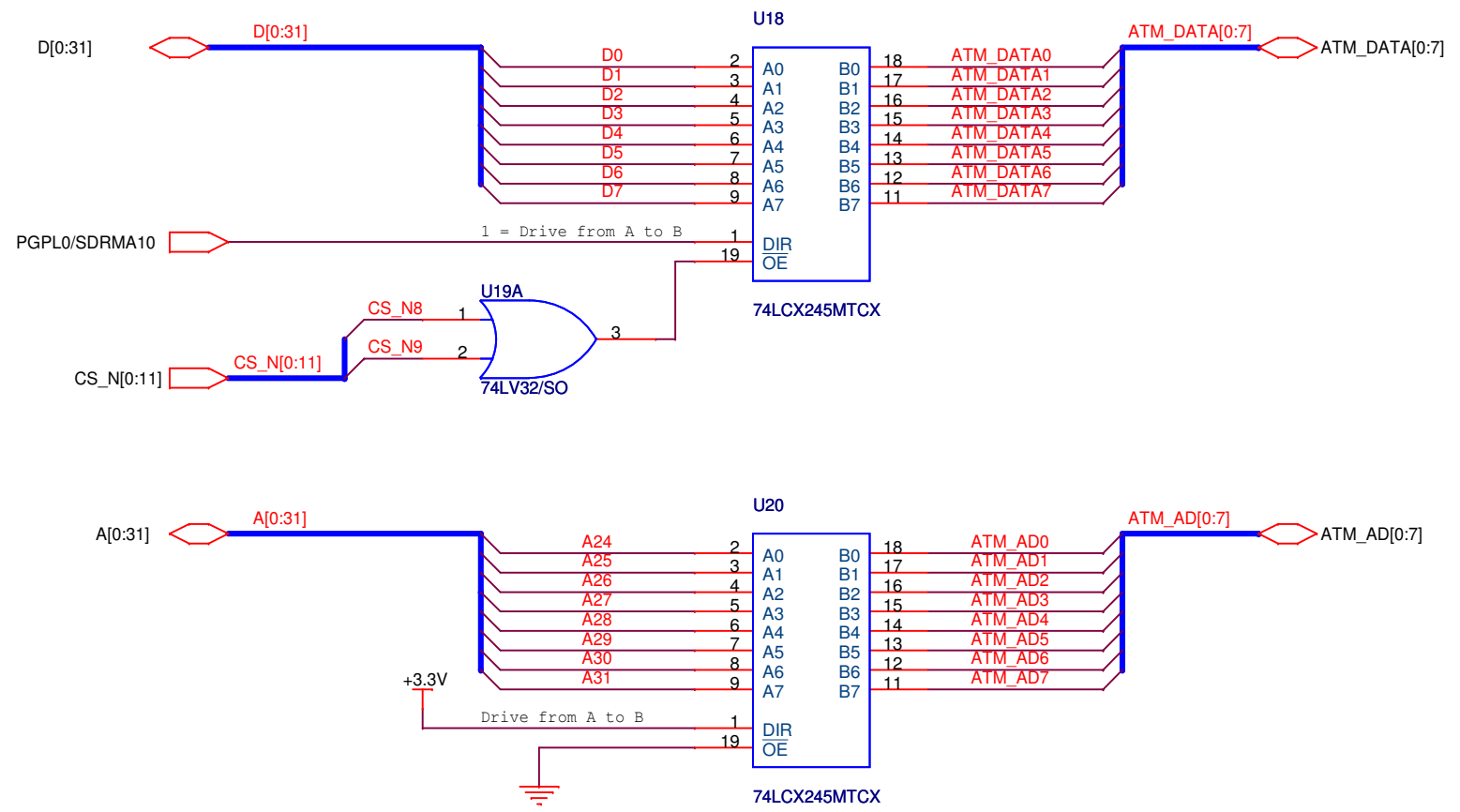


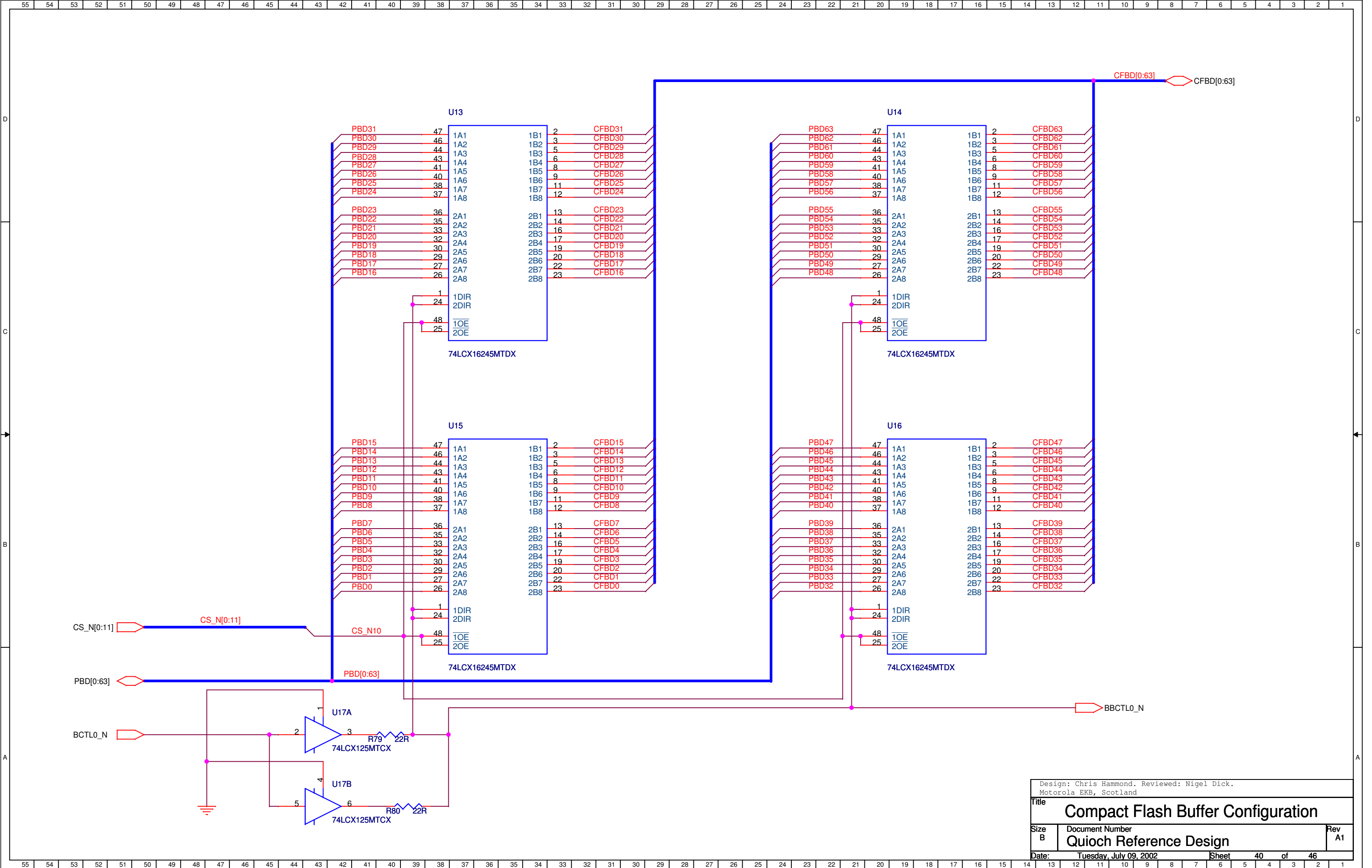


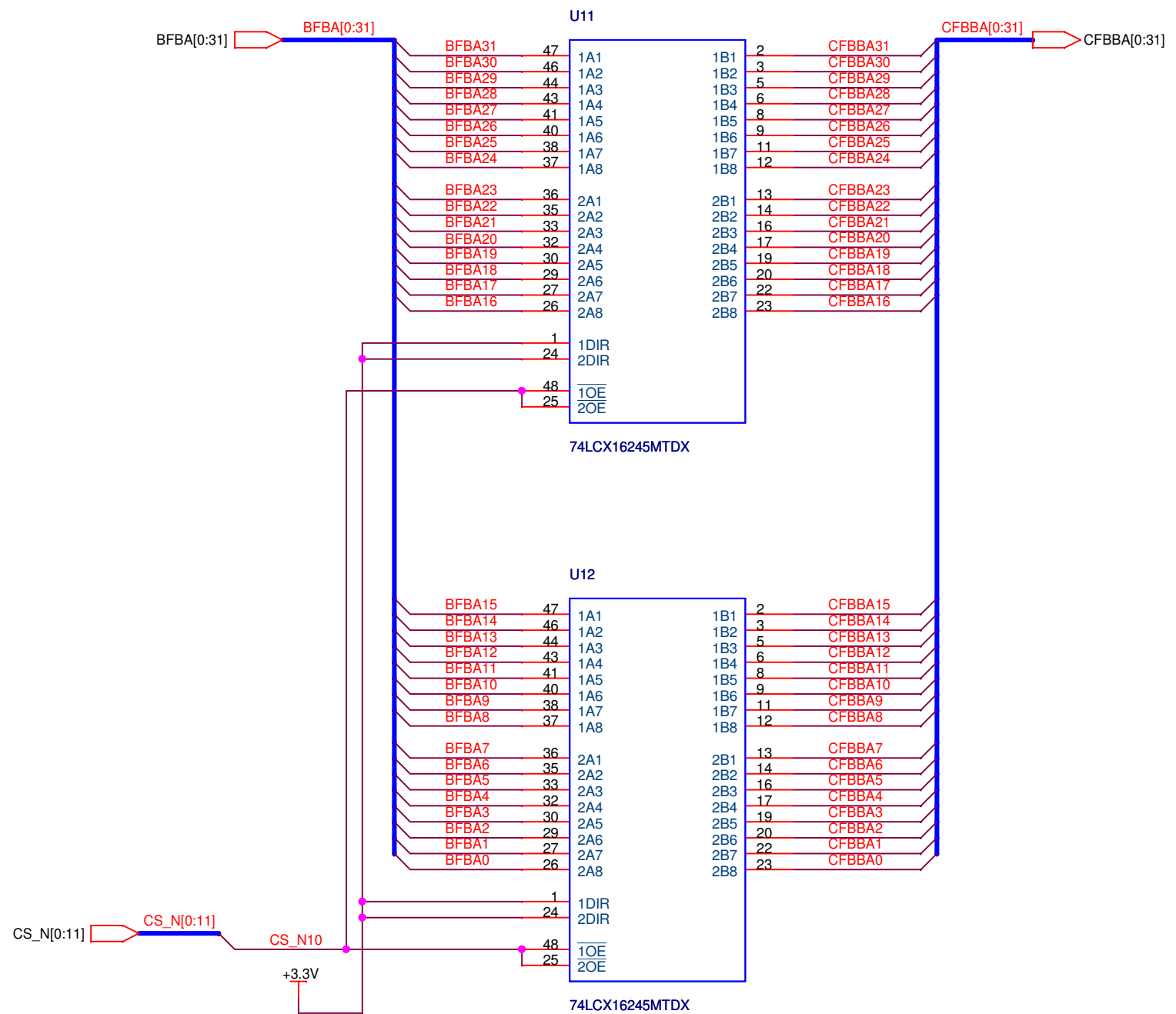
Design: Chris Hammond. Reviewed: Nigel Dick. Motorola EKB, Scotland									
Title CPLD Top Level									
Size B	Document Number Quioch Reference Design								Rev A1
Date:	Tuesday, July 09, 2002				Sheet	37	of	46	

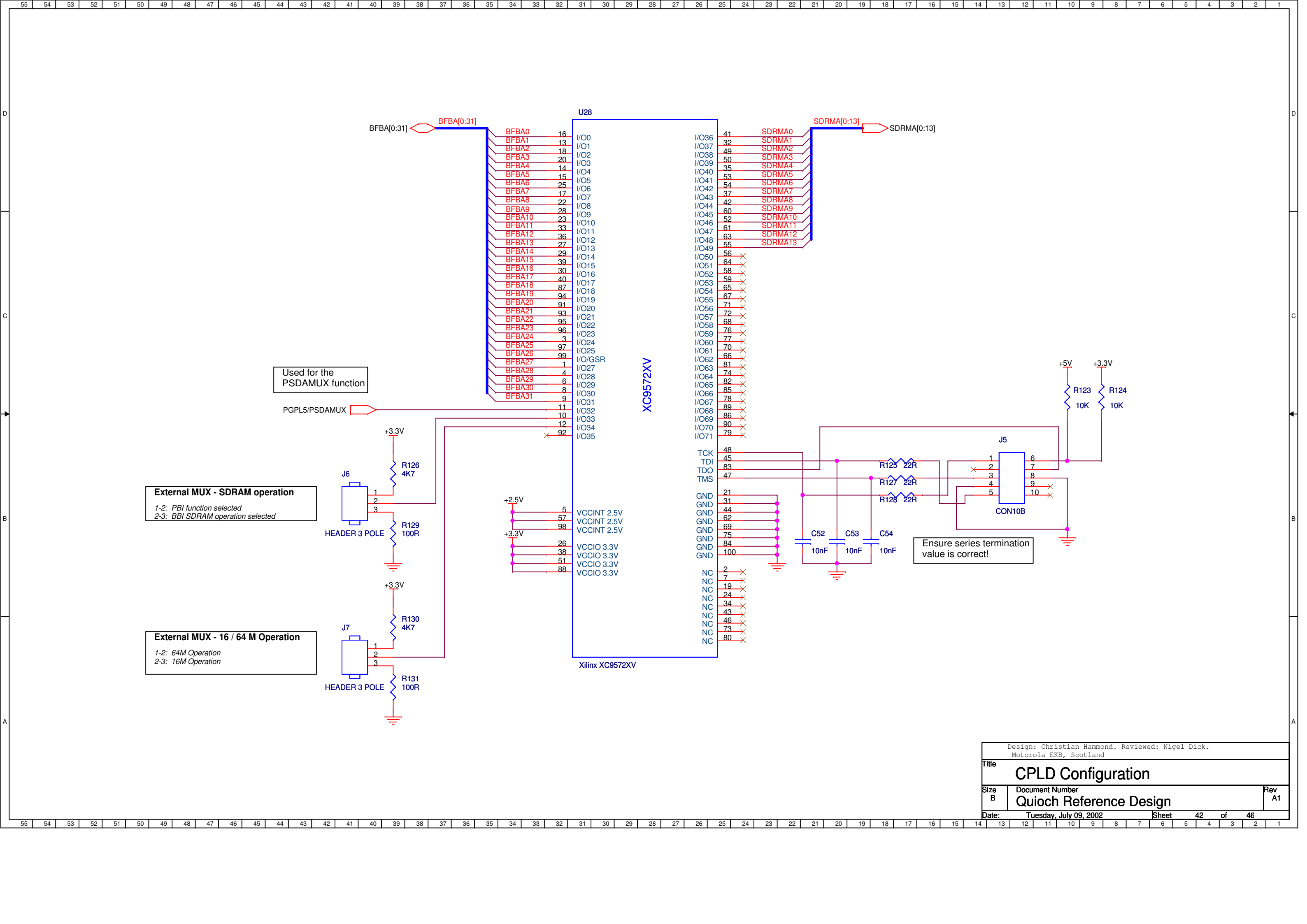


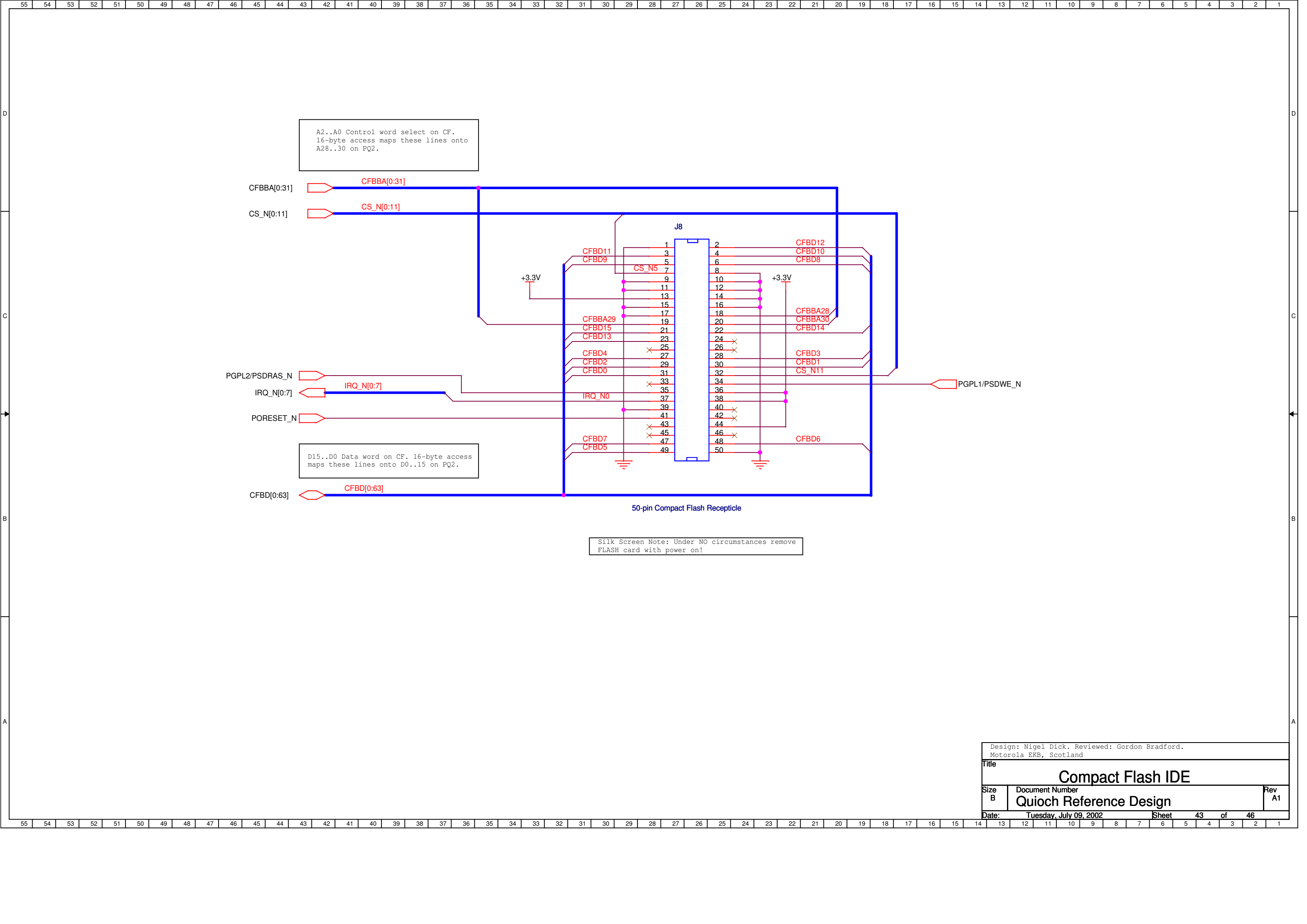
Design: Chris Hammond. Reviewed: Nigel Dick. Motorola EKB, Scotland											
Title 60x Latch Configuration											
Size B	Document Number Quioch Reference Design									Rev A1	
Date:	Tuesday, July 09, 2002			Sheet		38	of		46		

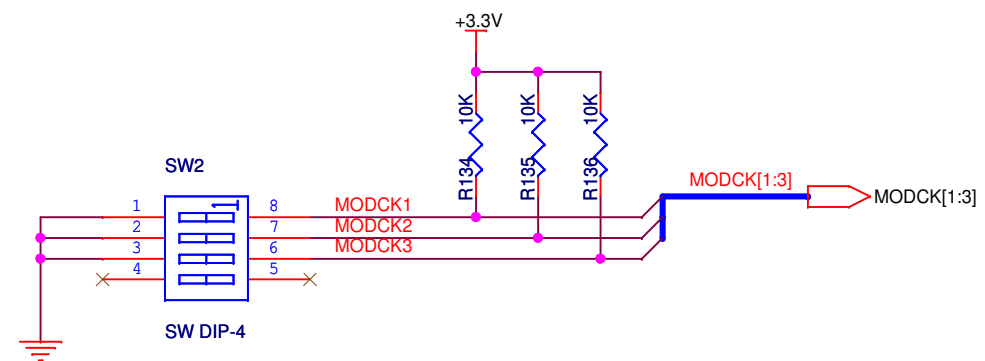
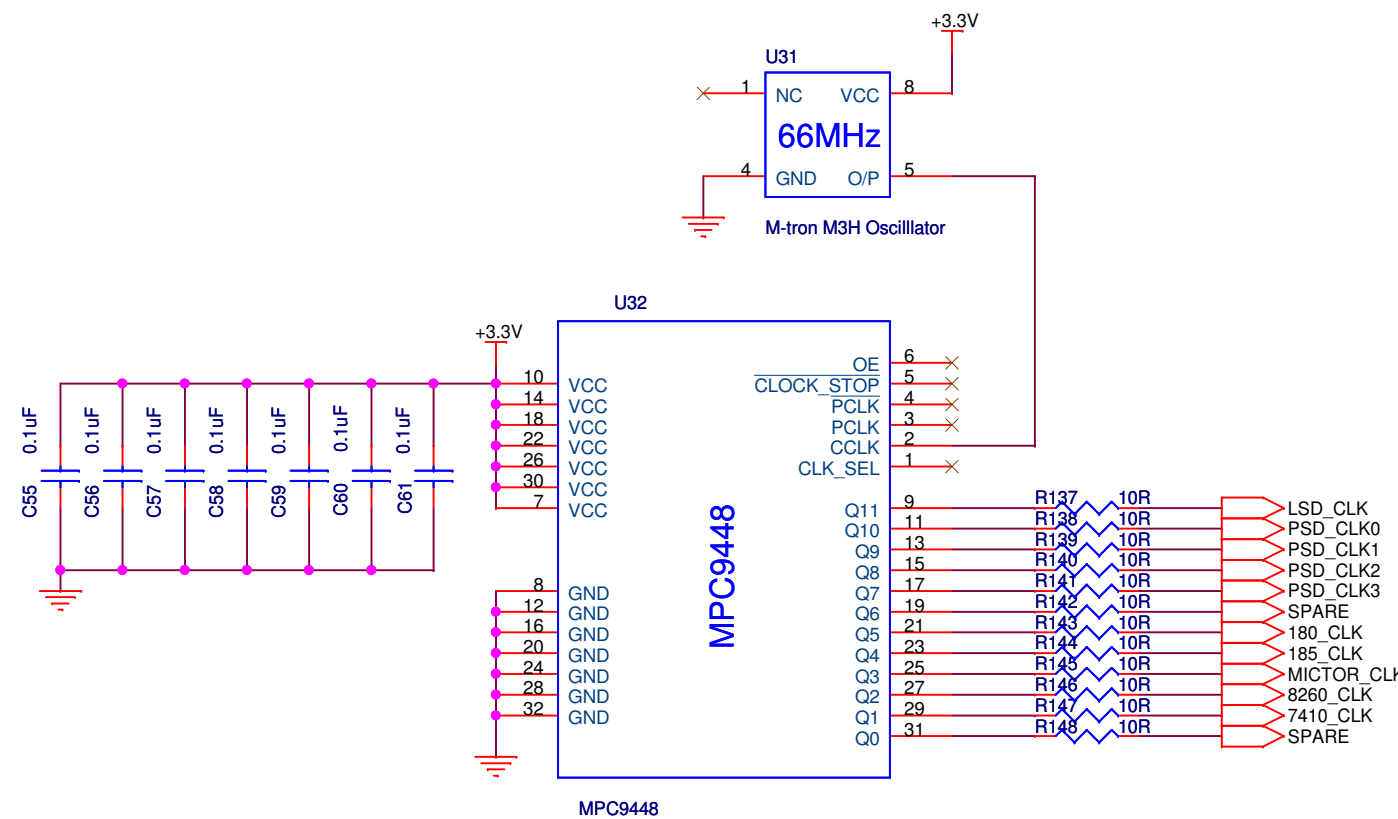


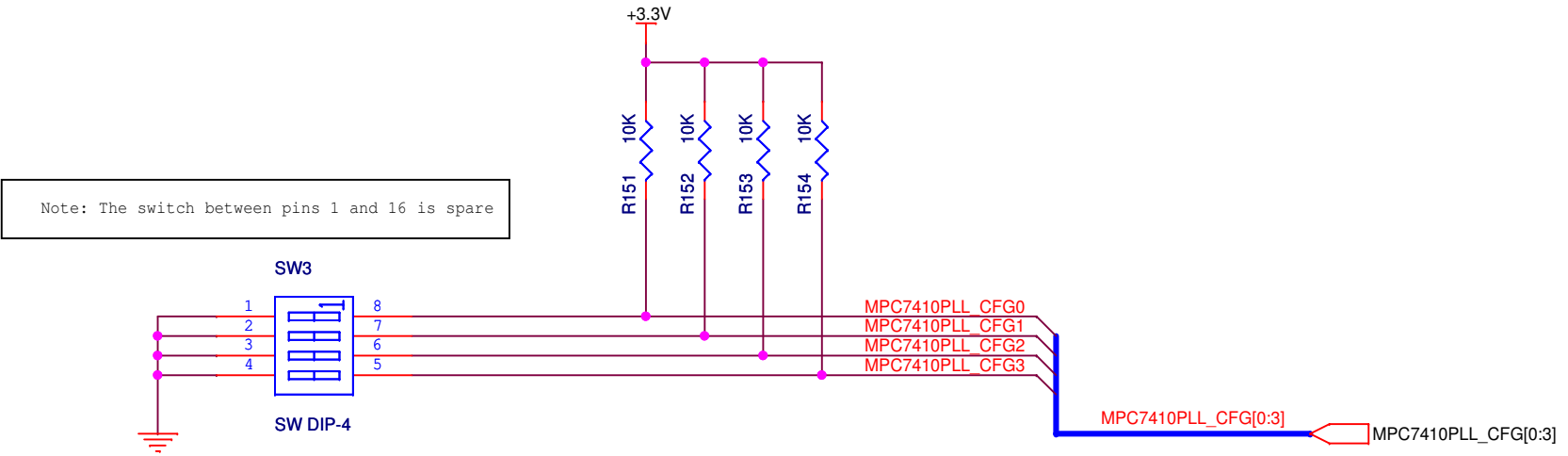
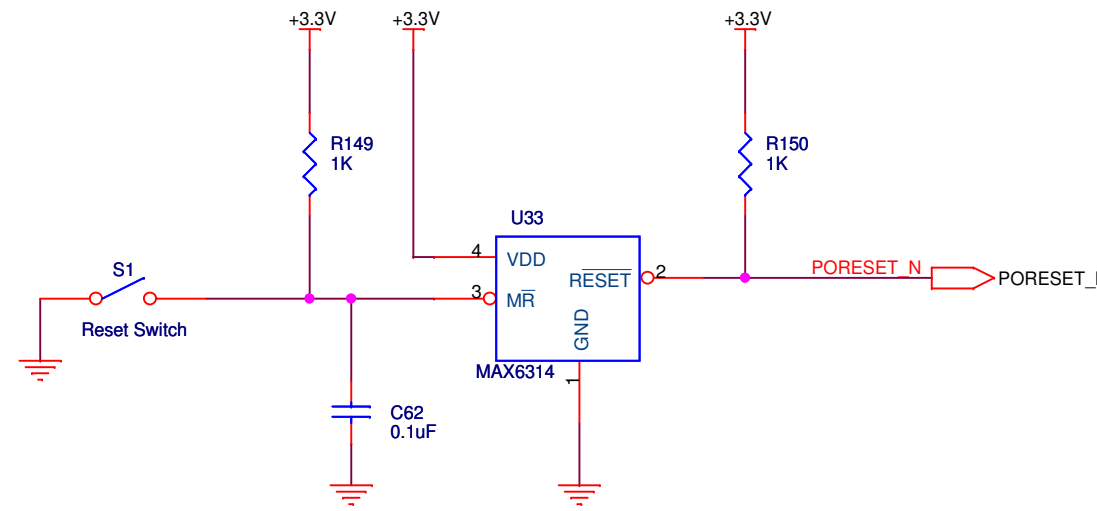












Key:
P1 = +12V
P2 = +5V
P3 = +5V
P4 = GND

Vertical Cable Mount
Terminals 5.08mm Pitch, 2
part PCB Connectors (12A
rating or greater)

Header for FAN
(2.54mm Pitch 7mm)

Sense resistor:
Outside Copper Trace: 0.21" X 1.87"
taps at 1.53", 1.70", 1.87"
(.009 / .010 / .011 Ohm)

Kelvin connections to be routed parallel and directly to ends of sense resistor

Keep gate resistors close to FET's. FET needs heatsink copper area of 0.5 sq in.
Route sense resistor trace on inner layer under FET for temp tracking

Locate away from other circuitry on BOTTOM SIDE.
The MBRS340 will fail if the 3.3V rail is shorted to ground.

Decoupling Capacitors

Power Indicators