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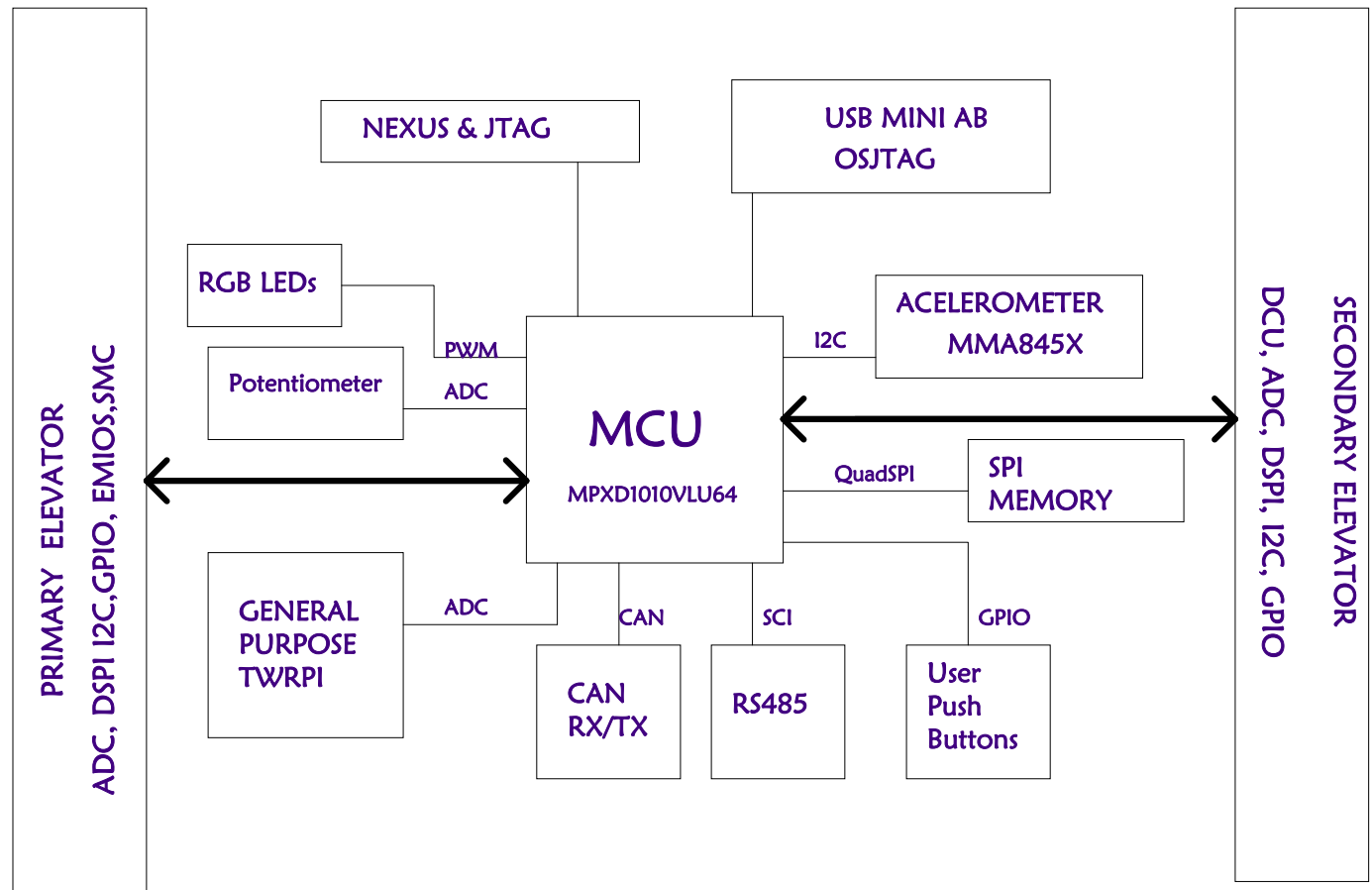
Revisions

Rev	Description	Date	Approved
X1	Initial Draft	11/08/11	JR
X2	Change RS485 from full duplex to a Half duplex MCU_PF1 ->IRQ_I and IRQ_J on secondary elevator MCU_PF2 ->IRQ_K and IRQ_L on secondary board MCU_PG12 ->IRQ_M and IRQ_N on secondary board MCU_PK10 ->IRQ_A and IRQ_B on Primary board J7 and J10 change to a single jumper selection(simple enable or disable accelerometer) Test Pads connected to GND J23 Removed. Third connection to ground on RS485 and CAN headers added	15/08/11	JR
X3	CAN Termination circuit modified, BAM HDRs added	16/08/11	JR
X4	Adjust RBD LED resistor values	16/08/11	JR
X5	HDRs in I2C lines were removed. PE[3..0] were reassigned to GPIO [17..15]. +5V HDR selection removed, 5 volts will be supplied by the USB switch. HDR added to isolate 120 ohms termination resistor at CAN transiever. PG12 reassigned to Primariy IRQ C and D	17/08/11	JR
X6	Adding UART lines to TWRPI connector	22/08/11	JR
X7	Assign DE & RE RS485 transceiver pin to GPIOs	23/08/11	JR
A	Release for Production	24/08/11	JR
AX1	OSJTAG DM and DP lines swapped Change RS485 transceiver to SP3483 Change microcontroller part number to MPXD1010VLU64 Give more space to NEXUS connector TWRPI connectors swapped Add 4.7Kohm pull-up resistors on the I2C lines: I2C2_SCL and I2C2_SDA LCD lines re-assigned.	18/11/11	JR
B	Release for Production	19/12/11	JR

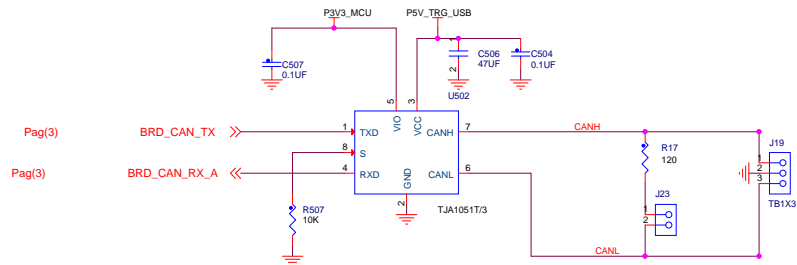
		Microcontroller Solutions Group	
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ICAP Classification: FCP:		FLUQ: X PUB:	
Designer: Dafne Sanchez	Drawing Title: TWR-PXD10XX		
Drawn by: Dafne Sanchez	Page Title: TITLE PAGE		
Approved: Jose Ruiz	Size C	Document Number SCH-27279 PDF: SPF-27279	Rev B
Date: Tuesday, December 20, 2011		Sheet 1 of 7	

All polarized capacitors are aluminum electrolytic

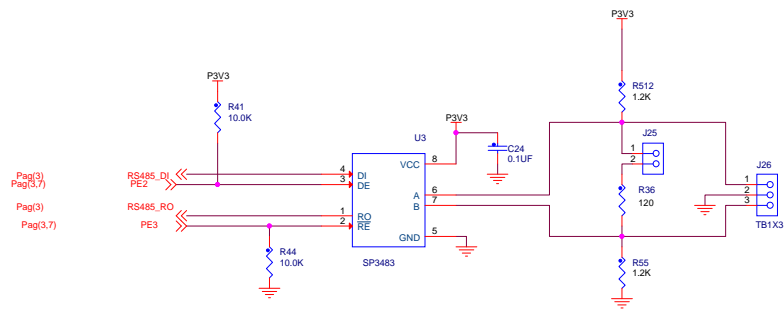
2. Interrupted lines coded with the same letter or letter combinations are electrically connected.
3. Device type number is for reference only. The number varies with the manufacturer.
4. Special signal usage:
 _B Denotes - Active-Low Signal
 <> or [] Denotes - Vectored Signals
5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



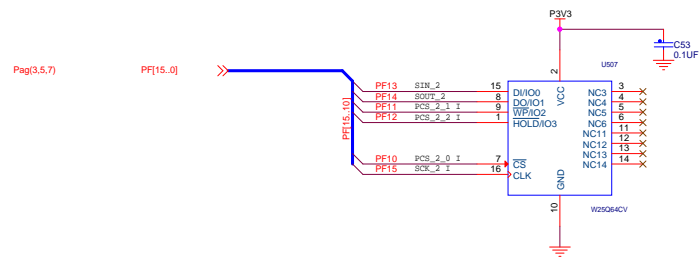
NXP CAN Transceiver

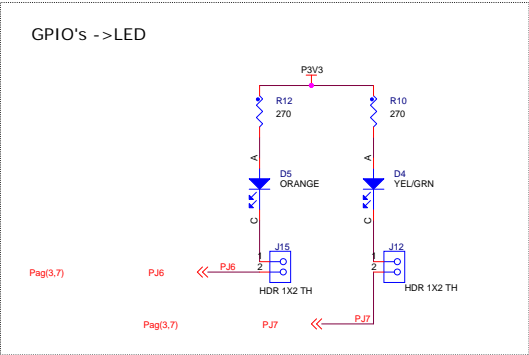
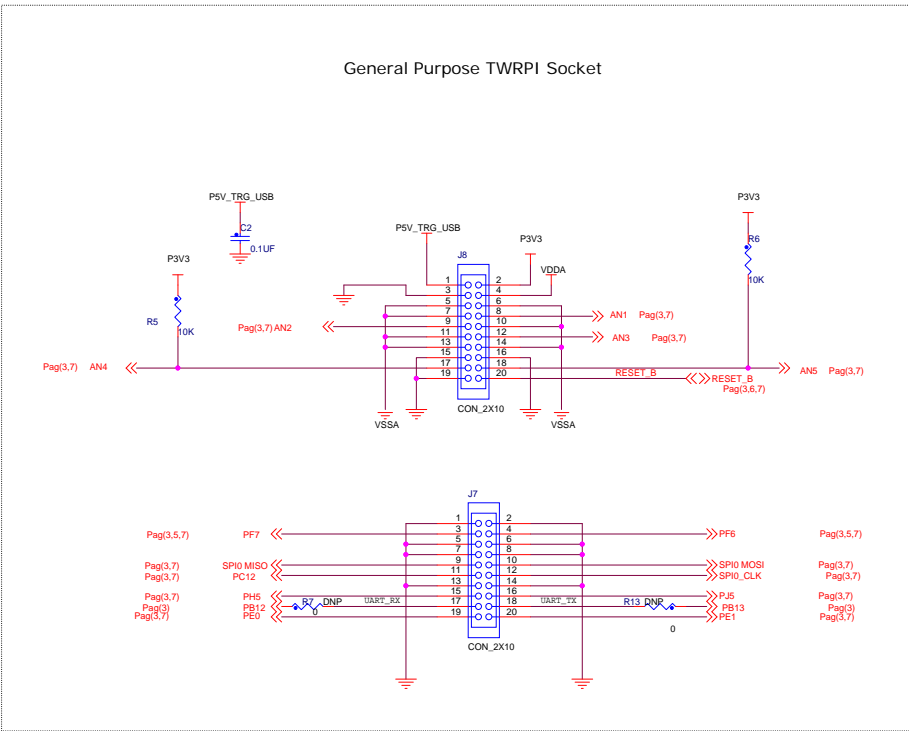
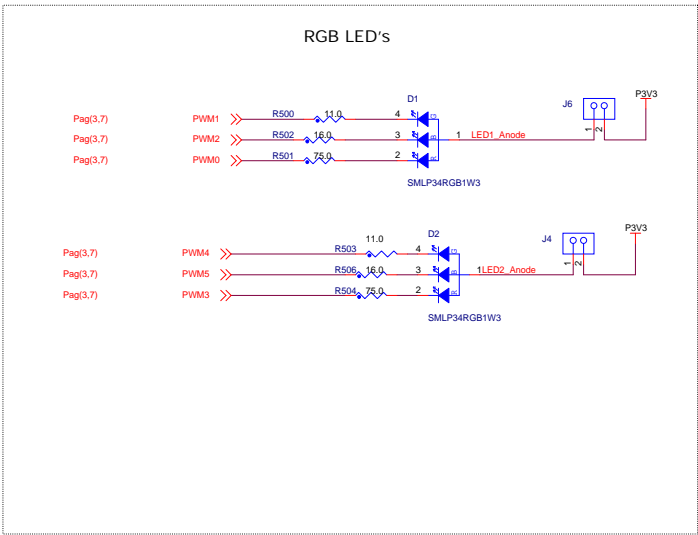
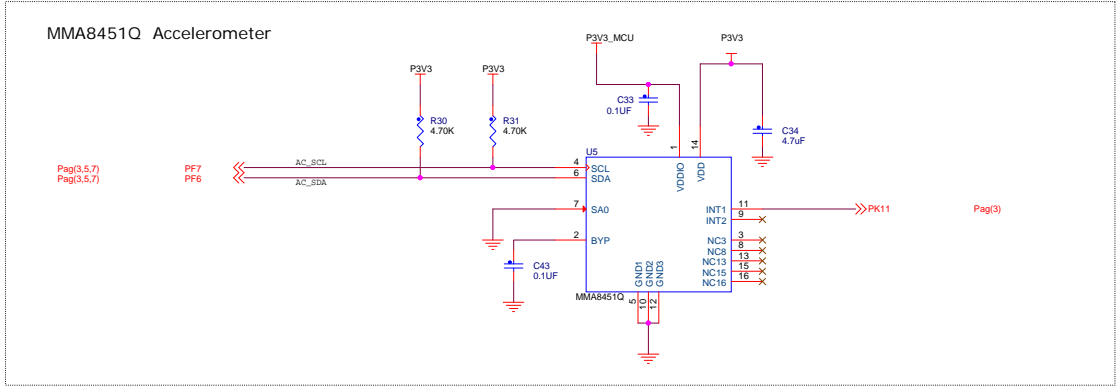


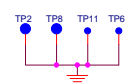
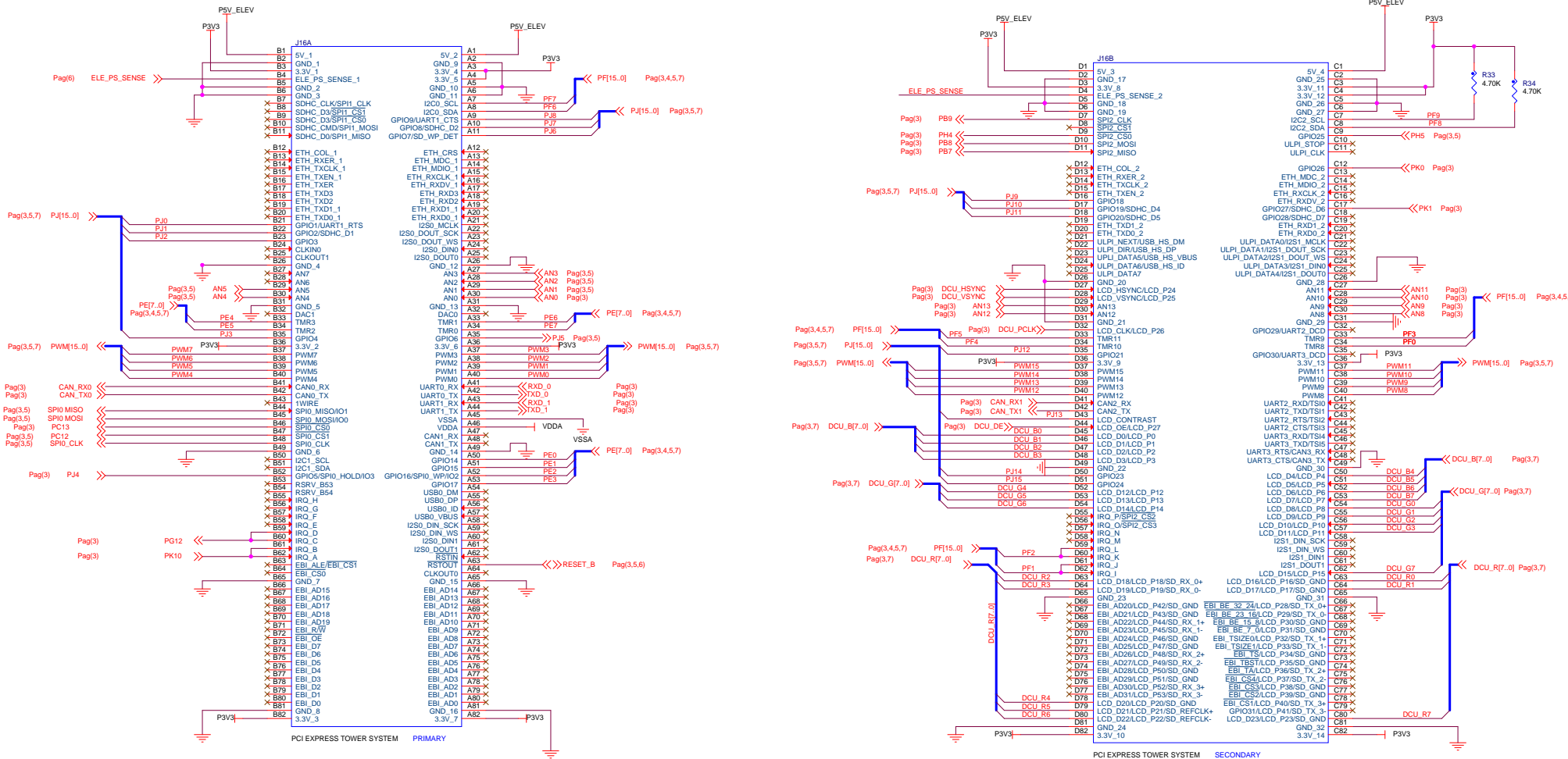
RS-485 HALF DUPLEX TRANSCEIVER



SPI MEMORY







freescale
semiconductor

ICAP Classification: FCP: FIUC: X PUBL: _____
Drawing Title: **TWR-PXD10XX**

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