PTN3356 Evaluation and Applicaiton Board Rev. 0.10

REVISION HISTORY :

0.1 June 10, 2014
- Base on PTN3355_ONLY_REV14.DSN

0.2 July 16, 2014
- BOM changes due to long lead time items, LEDs

0.3 July 17, 2014
- Change USB J12

0.4 July 17, 2014
- Change U1 to Johnstech ROL 100A Series
- Change U4 to TI part

0.5 July 21, 2014
- Change D10, D13, D14 singal names
- Swap U2, D6 to un-twist H/V sync
- change U2 to SSOP
- Add TP23, TP24

0.6 July 22, 2014
- Remove D12

0.7 July 22, 2014
- Remove U3 and caps around it.

0.8 July 23, 2014
- Add AC caps for DP lanes

0.9 July 24, 2014
- Correct DP signal name

0.10 Aug. 04, 2014
- U4 library is wrong
- Re-work U4 connection

Page#	Page Title
1	Index
2	PTN3356
3	VGA
4	DP & Power
5	JTAG & CONFIG

NXP Semiconductors

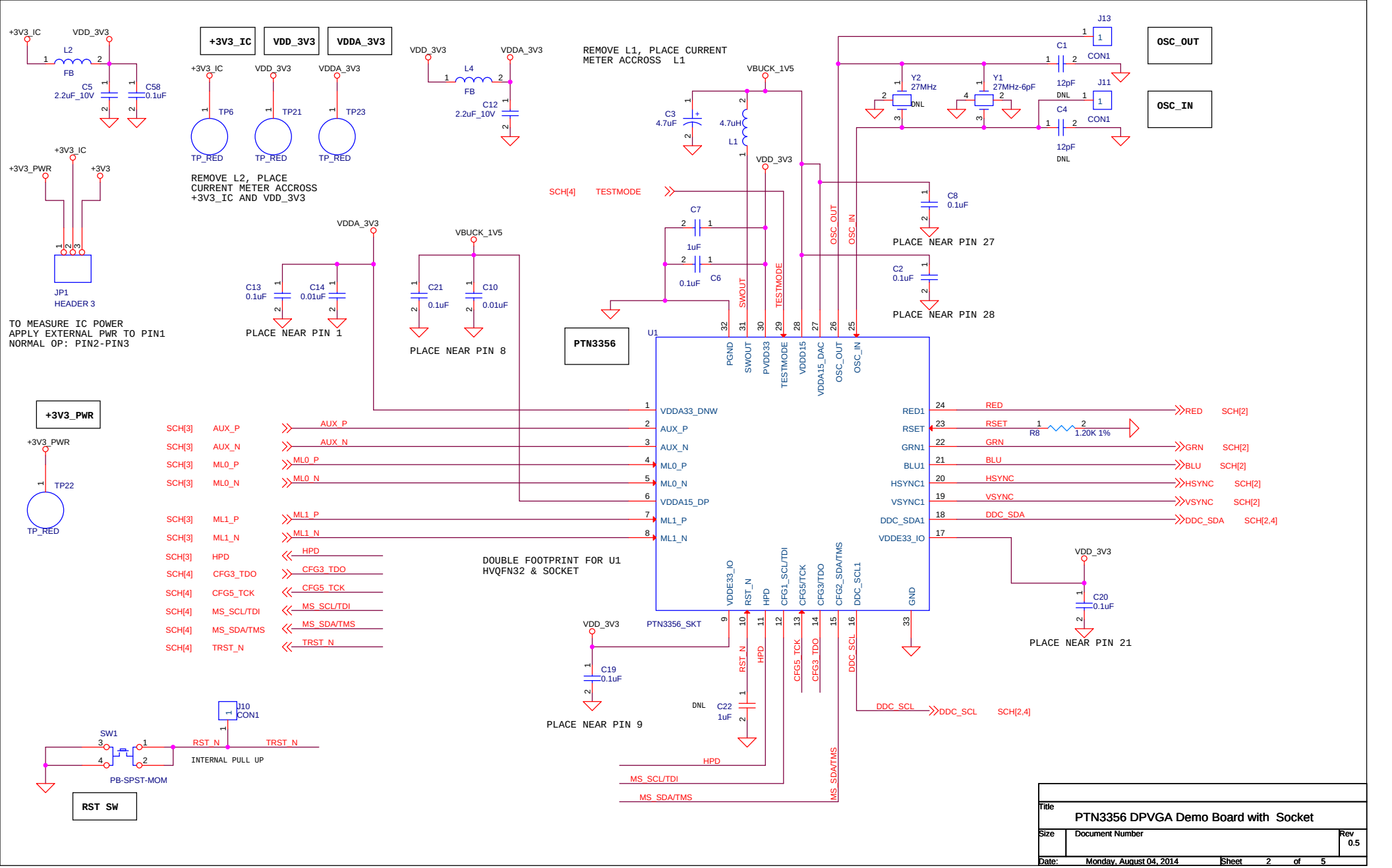
411 E. Plumeria Drive, San Jose, CA 95134

Title: **INDEX**

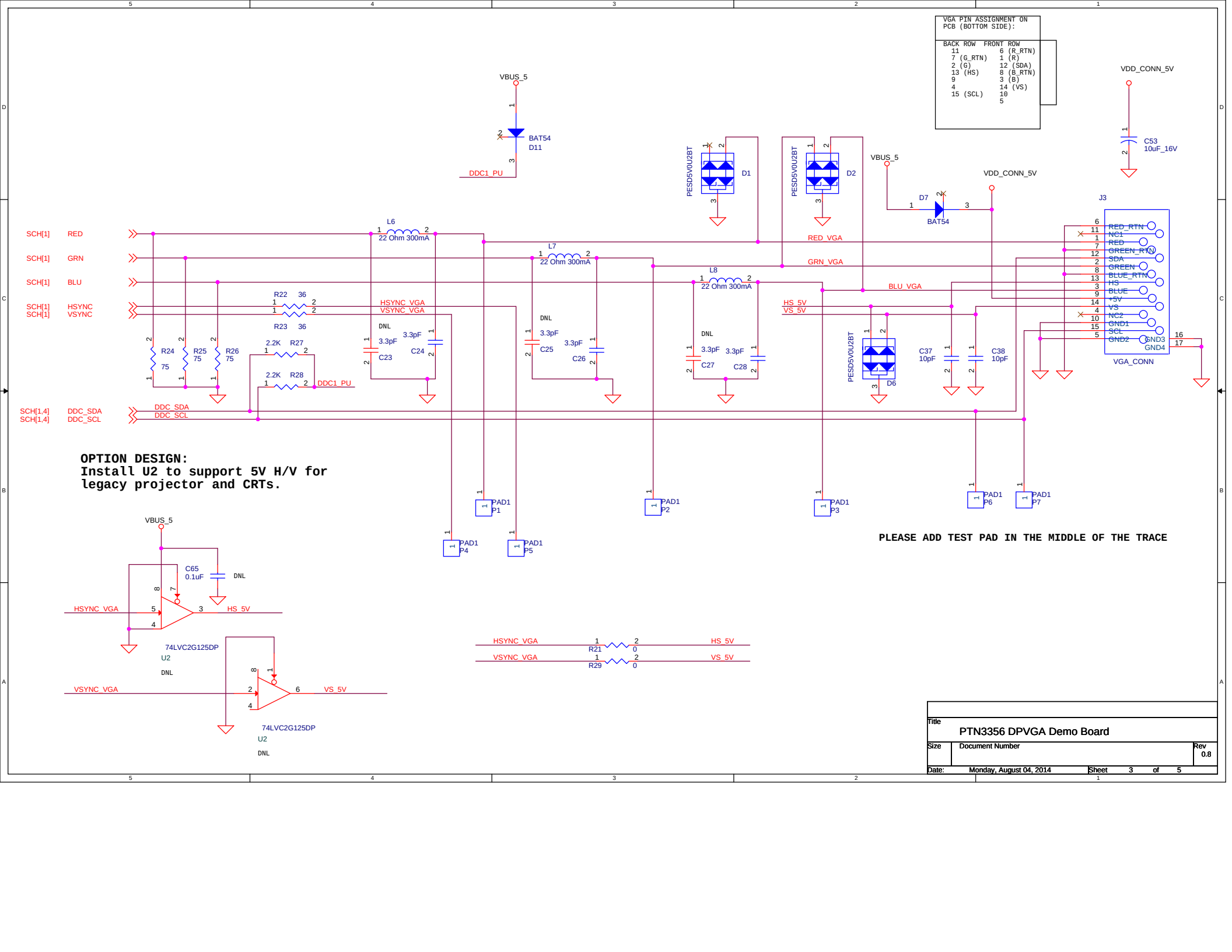
Document Name: **PTN3356 DPVGA**

Size	Document Number	Rev
B		0.10

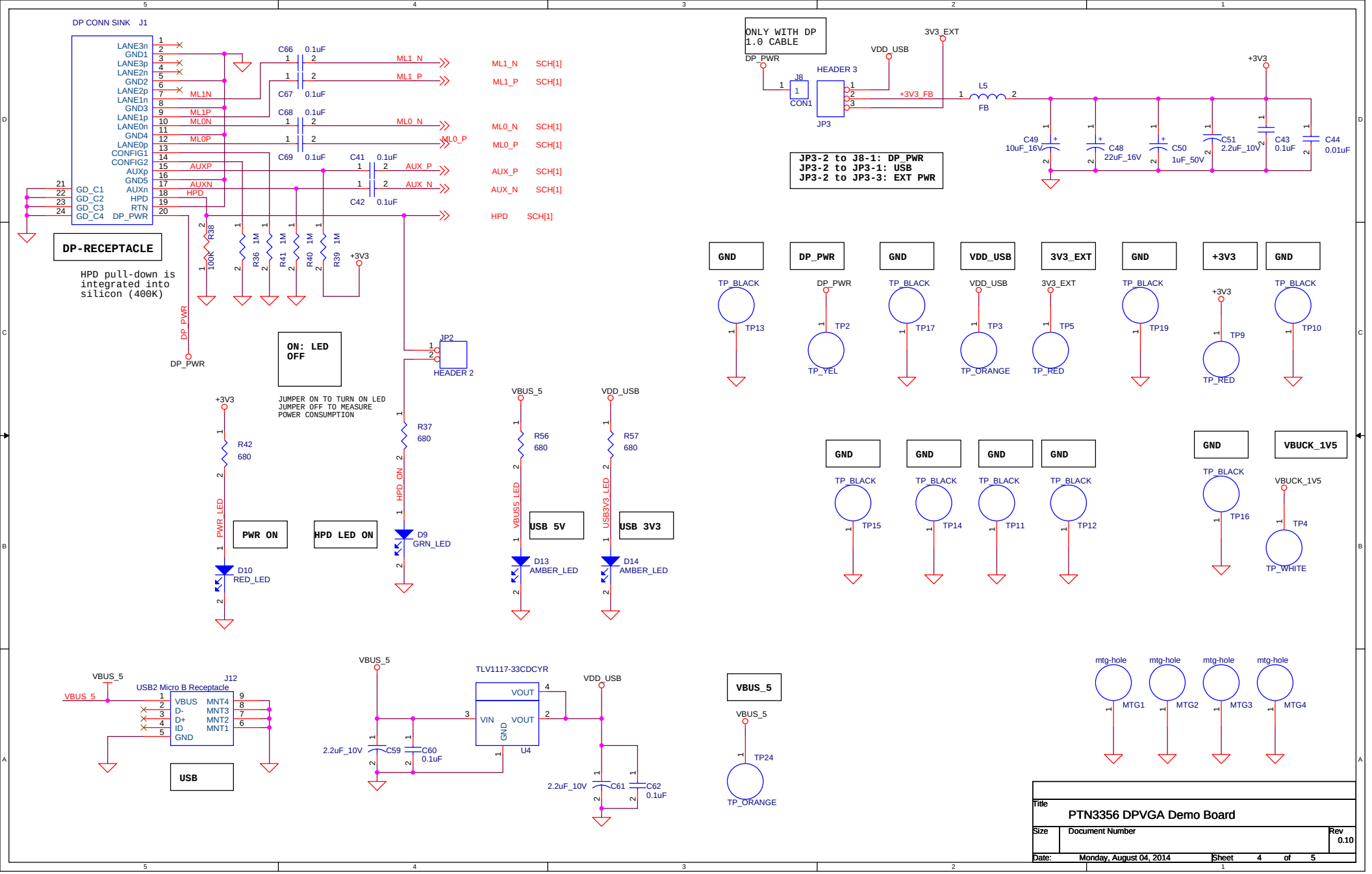
Date: Monday, August 04, 2014 Sheet 1 of 5



Title	PTN3356 DPVGA Demo Board with Socket	
Size	Document Number	Rev 0.5
Date: Monday, August 04, 2014	Sheet 2 of 5	



Title	PTN3356 DPVGA Demo Board	
Size	Document Number	Rev 0.8
Date: Monday, August 04, 2014	Sheet 3 of 5	



Title: PTN3356 DPVGA Demo Board

Size | Document Number | Rev 0.10

Date: Monday, August 04, 2014 | Sheet 4 of 5

HI
CFG5/TCK
LO

HEADER 3
JP5
R49 10K
R50 10K
CFG5_TCK
+3V3
CFG5_TCK SCH[1]

JUMPER 1-2, HIGH, 24 MHZ XTAL IS USED
OPEN: 27 MHZ XTAL IS USED
JUMPER 2-3, LOW, 25 MHZ XTAL IS USED

HI
TESTMODE
LO

HI
CFG1-MS_SCL/TDI
LO

HI
CFG2-MS_SDA/TMS
LO

HI
CFG3-SPARE
LO

+3V3
R44 10K
R45 10K
R46 10K
R48 10K
HEADER 3
JP4
TESTMODE
TESTMODE SCH[1]

HI = PIN 1-2, CFG[5:1] = JTAG PINS
LO = PIN 2-3, CFG[5:1] = CONFIG PINS, I2C ADDRESS = 40h
OPEN: CFG[5:1] = CONFIG PINS, I2C ADDRESS = C0h

HEADER 3
JP7
MS_SCL/TDI
MS_SCL/TDI SCH[1,4]

CFG1 CFG2:
11: COMPLIANT HPD BEHAVIOR, MS BUS IS USED
10: NON-COMPLIANT HPD BEHAVIOR
01: NON-COMPLIANT HPD BEHAVIOR
00: COMPLIANT HPD BEHAVIOR

HEADER 3
JP9
MS_SDA/TMS
MS_SDA/TMS SCH[1,4]

HEADER 3
JP10
CFG3_TDO
CFG3_TDO SCH[1]

R52 10K
R53 10K
R51 10K
R55 10K

SCH[1] TRST_N
TRST_N

FOR PTN3356 WITH FLASH ONLY

SCH[1,4] MS_SCL/TDI
SCH[1,4] MS_SDA/TMS
MS_SCL/TDI
MS_SDA/TMS
J5
HEADER 4
MS_I2C
I2C BIRD PIN OUT

SCH[1,2] DDC_SCL
SCH[1,2] DDC_SDA
DDC_SCL
DDC_SDA
J7
HEADER 4
DDC_I2C
I2C BIRD PIN OUT

CFG5_TCK
CFG3_TDO
MS_SDA/TMS
MS_SCL/TDI
JTAG
DNL C35 100pF
J6
HEADER 2x5
+3V3
R43 1K
DNL
TRST_N

MOUNT J4 ON THE
TOP SIDE WITH
RIGHT ANGLE
CONNECTOR

Title	PTN33356 CONFIG AND JTAG	
Size	Document Number	Rev 0.1
Date: Monday, August 04, 2014	Sheet 5 of 5	