

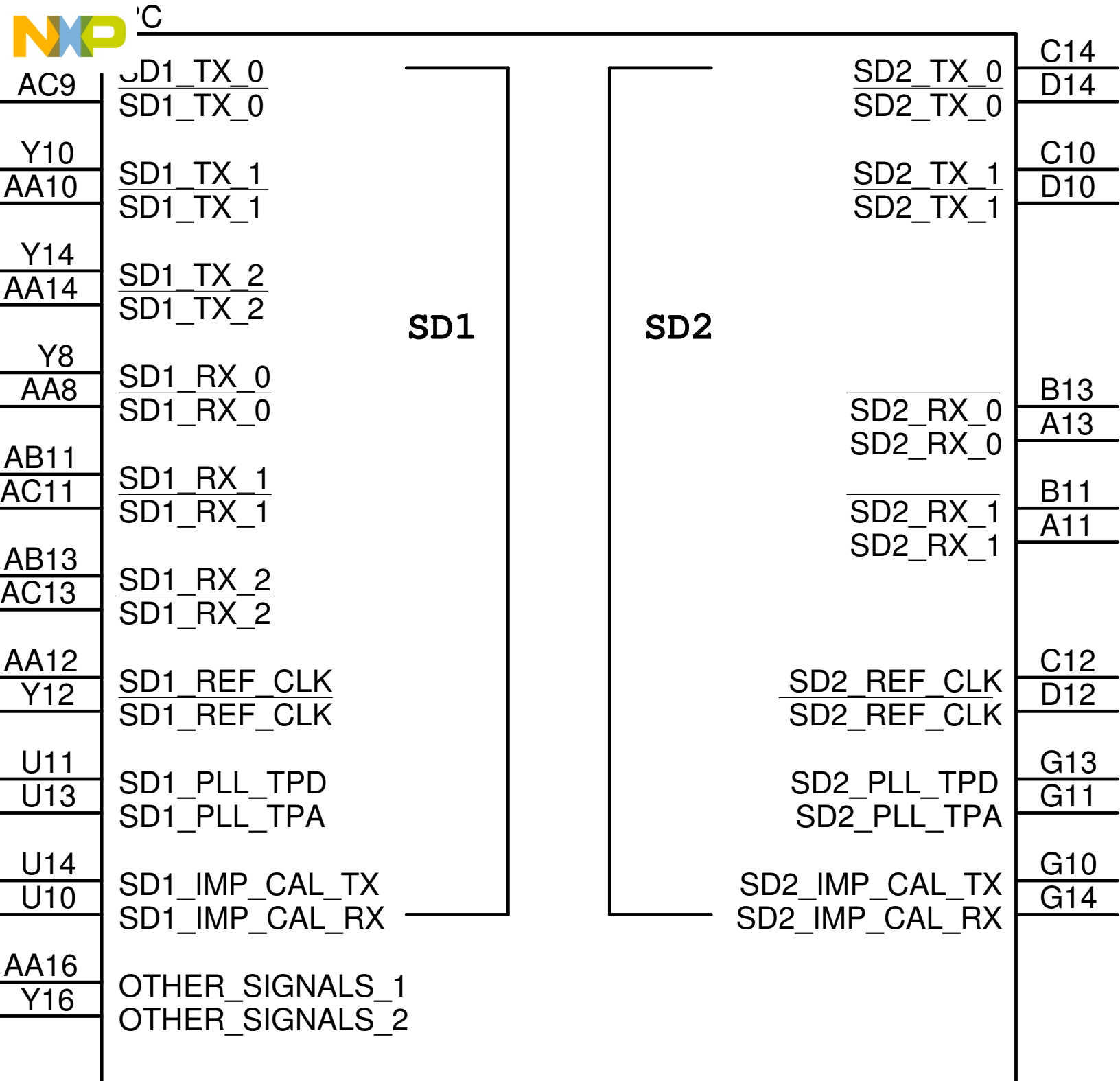
DDR3/DDR3L CONTROLLER			
	MDQ_00	MA_00	D3
M3	MDQ_01	MA_01	D7
J4	MDQ_02	MA_02	B6
N4	MDQ_03	MA_03	B3
K3	MDQ_04	MA_04	A2
N3	MDQ_05	MA_05	C7
G3	MDQ_06	MA_06	A5
L3	MDQ_07	MA_07	A3
H3	MDQS_0	MA_08	C6
J3	MDQS_0	MA_09	B5
M4	MDM_0	MA_10	D1
		MA_11	A4
H2	MDQ_08	MA_12	D5
L1	MDQ_09	MA_13	A6
G1	MDQ_10	MA_14	C3
M2	MDQ_11	MA_15	A7
H1	MDQ_12		
N1	MDQ_13	MBA_0	C4
J2	MDQ_14	MBA_1	C5
M1	MDQ_15	MBA_2	D4
J1	MDQS_1		
K1	MDQS_1	MODT_0	E2
L2	MDM_1	MODT_1	E1
R4	MECC_0		
V4	MECC_1	MCKE_0	E3
R3	MECC_2	MCKE_1	C1
W4	MECC_3		
T4	MECC_4	MCS_0	B1
Y2	MECC_5	MCS_1	C2
P3	MECC_6	MCS_2	A8
V3	MECC_7	MCS_3	B8
T3	MDQS_2		
U3	MDQS_2	MWE	F4
W3	MDM_2	MRAS	F1
		MCAS	F2
		MCK	G4
		MCK	F3
		MDIC_0	D8
		MDIC_1	C8
		MVREF	J7

<Value>



	AD_00/CFG_SYS_PLL_0	IFC_ADDR_16/SDHC_CLK/USB_CLK/IFC_CS_2	W23
T23	IFC_AD_01/CFG_SYS_PLL_1	IFC_ADDR_17/SDHC_CMD/USB_D_0/DMA_DREQ_1	W21
T22	IFC_AD_02/CFG_SYS_PLL_2	IFC_ADDR_18/SDHC_DATA_0/USB_D_1/DMA_DACK_1	Y23
U23	IFC_AD_03/CFG_CORE_PLL_0	IFC_ADDR_19/SDHC_DATA_1/USB_D_2/DMA_DDONE_1	Y22
U22	IFC_AD_04/CFG_CORE_PLL_1	IFC_ADDR_20/SDHC_DATA_2/USB_D_3	AA23
V23	IFC_AD_05/CFG_CORE_PLL_2	IFC_ADDR_21/SDHC_DATA_3/USB_D_4	Y21
V22	IFC_AD_06/CFG_CORE_SPEED	IFC_ADDR_22/SDHC_WP/USB_D_5	AB23
R21	IFC_AD_07/CFG_DDR_PLL_0	IFC_ADDR_23/SDHC_CD/USB_D_6	AA22
R20	IFC_AD_08/CFG_DDR_PLL_1	IFC_ADDR_24/USB_D_7	AC23
T21	IFC_AD_09/CFG_IFC_PB_0	IFC/eSDHC/ULPI	AA21
T20	IFC_AD_10/CFG_IFC_PB_1		AB21
U21	IFC_AD_11/CFG_IFC_PB_2		
V21	IFC_AD_12/CFG_SRDS_REFCLK		Y18
V20	IFC_AD_13/CFG_IO_PORTS_0	IFC_CLK_0	AC18
W20	IFC_AD_14/CFG_IO_PORTS_1	IFC_CLK_1/USB_NXT/IFC_CS_3	
	IFC_AD_15/CFG_IFC_ADM		AA19
AA18		IFC_BCTL/CFG_BOOT_SEQ_0	AC22
AB18	IFC_PERR/USB_DIR	IFC_AVD/CFG_DRAM_TYPE	AA20
AC19	IFC_PAR_1/CFG_PLAT_SPEED	IFC_CLE/CFG_HOST_AGT_0	AB20
	IFC_PAR_0/USB_STP	IFC_OE/CFG_HOST_AGT_1	AC20
		IFC_WP	AC21
		IFC_WE/CFG_IFC_FLASH_MODE	Y19
		IFC_RB	

<Value>



<Value>

TSEC1_TXD_0/1588_ALARM_OUT1/CFG_ROM_LOC[0]
 TSEC1_TXD_1/1588_ALARM_OUT2/CFG_ROM_LOC[1]
 TSEC1_TXD_2/1588_PULSE_OUT1/CFG_ROM_LOC[2]
 TSEC1_TXD_3/1588_PULSE_OUT2/CFG_ROM_LOC[3]
 TSEC1_TX_EN/CFG_SVR
 TSEC1_GTX_CLK/DMA_DDONE_0

 TSEC1_RXD_0/1588_TRIG_IN1
 TSEC1_RXD_1/1588_TRIG_IN2/GPIO_12
 TSEC1_RXD_2/1588_CLK_IN
 TSEC1_RXD_3/1588_CLK_OUT
 TSEC1_RX_DV/DMA_DREQ_0/GPIO_13
 TSEC1_RX_CLK/DMA_DACK_0/GPIO_14
 TSEC1_GTX_CLK125/GPIO_15

 EC_MDIO
 EC_MDC/CFG_CPU_BOOT

AC5

AC1

AA5

AA4

AC6

AA3

AC4

AB4

AB3

AC3

AB6

Y6

Y5

AC2

AA6

<Value>



<Value>



	J1	AVDD_DDR	N17
U16	BVDD2		
U17	BVDD3	AVDD_PLAT	P17
U20	BVDD4		
	BVDD5	AVDD_CORE	H9
G17			
H17	BVDD_VSEL_0	SD1_AVDD	U12
	BVDD_VSEL_1		
G7		SD2_AVDD	G12
G8	GVDD1		
G9	GVDD2	VDD1	G15
H7	GVDD3	VDD2	G16
K7	GVDD4	VDD3	H10
L7	GVDD5	VDD4	H11
M7	GVDD6	VDD5	H14
N7	GVDD7	VDD6	H15
P7	GVDD8	VDD7	H16
R7	GVDD9	VDD8	H8
T7	GVDD10	VDD9	J16
	GVDD11	VDD10	J17
U7		VDD11	J8
U8	LVDD1	VDD12	K16
AB5	LVDD2	VDD13	K17
	LVDD3	VDD14	K8
C17		VDD15	L16
C22	OVDD1	VDD16	L8
D20	OVDD2	VDD17	M16
G20	OVDD3	VDD18	M8
J20	OVDD4	VDD19	N16
	OVDD5	VDD20	N8
AA11		VDD21	P16
AA17	S1VDD1	VDD22	P8
AB10	S1VDD2	VDD23	R16
AB12	S1VDD3	VDD24	R17
AB14	S1VDD4	VDD25	R8
AB7	S1VDD5	VDD26	T10
T13	S1VDD6	VDD27	T14
Y13	S1VDD7	VDD28	T15
Y7	S1VDD8	VDD29	T16
	S1VDD9	VDD30	T8
A10		VDD31	T9
A12	S2VDD1	VDD32	U15
C11	S2VDD2	VDD33	U9
C15	S2VDD3		
H13	S2VDD4	USBVDD1_0_1	L17
	S2VDD5	USBVDD1_0_2	M17
AB16			
AB8	X1VDD1	USBVDD1_8_1	J21
T11	X1VDD2	USBVDD1_8_2	K21
Y15	X1VDD3		
Y9	X1VDD4	USBVDD3_3_1	K20
	X1VDD5	USBVDD3_3_2	L20
A14			
B9	X2VDD1		
C13	X2VDD2		
C9	X2VDD3		
	X2VDD4		

POWER1

<Value>

			VSS81	Y4
			VSS80	Y20
AB17	S1VSS2		VSS79	W22
AC10	S1VSS3		VSS78	W2
AC12	S1VSS4		VSS77	U4
AC14	S1VSS5		VSS76	T2
Y11	S1VSS6		VSS75	R9
Y17	S1VSS7		VSS74	R23
	S1VSS8		VSS73	R15
B10			VSS72	R14
B12	S2VSS1		VSS71	R13
D11	S2VSS2		VSS70	R12
D15	S2VSS3		VSS69	R11
	S2VSS4		VSS68	R10
T12			VSS67	P9
H12	SD1_AVSS		VSS66	P4
	SD2_AVSS		VSS65	P22
J23			VSS64	P20
K22	USBVSS1		VSS63	P15
L22	USBVSS2		VSS62	P14
M21	USBVSS3		VSS61	P13
M23	USBVSS4		VSS60	P12
	USBVSS5		VSS59	P11
AA15			VSS58	P10
AA9	X1VSS1		VSS57	N9
AC16	X1VSS2		VSS56	N20
AC8	X1VSS3		VSS55	N2
	X1VSS4		VSS54	N15
B14			VSS53	N14
B15	X2VSS1		VSS52	N13
D13	X2VSS2		VSS51	N12
D9	X2VSS3		VSS50	N11
	X2VSS4		VSS49	N10
AA2			VSS48	M9
	SENSEVDD		VSS47	M15
Y3			VSS46	M14
	SENSEVSS		VSS45	M13
N21	FA_VDD	POWER2	VSS44	M12
AA1			VSS43	M11
AB1	NC_AA1		VSS42	M10
AB15	NC_AB1		VSS41	L9
AC15	NC_AB15		VSS40	L4
B2	NC_AC15		VSS39	L15
N22	NC_B2		VSS38	L14
N23	NC_N22		VSS37	L13
P1	NC_N23		VSS36	L12
P2	NC_P1		VSS35	L11
R1	NC_P2		VSS34	L10
R2	NC_R1		VSS33	K9
T1	NC_R2		VSS32	K2
U1	NC_T1		VSS31	K15
U2	NC_U1		VSS30	K14
V1	NC_U2		VSS29	K13
V2	NC_V1		VSS28	K12
W1	NC_V2		VSS27	K11
Y1	NC_W1		VSS26	K10
	NC_Y1		VSS25	J9
A1			VSS24	J15
A15	VSS1		VSS23	J14
A9	VSS2		VSS22	J13
AB2	VSS3		VSS21	J12
AB22	VSS4		VSS20	J11
AC17	VSS5		VSS19	J10
AC7	VSS6		VSS18	H4
B17	VSS7		VSS17	G22
B19	VSS8		VSS16	G2
B22	VSS9		VSS15	E4
B4	VSS10		VSS14	D6
B7	VSS11		VSS13	D2
	VSS12			